An Embedded Multi-Core Real-Time Simulation Platform of Basal Ganglia for Deep Brain Stimulation

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***Abstract*— Closed-loop deep brain stimulation (DBS) paradigm is gaining tremendous favor due to its potential capability of further and more efficient improvements in neurological diseases. Preclinical validation of closed-loop controller is quite necessary in order to minimize injury risks of clinical trials to patients, which can greatly benefit from real-time computational models and thus potentially reduce research and development costs and time. Here we developed an embedded multi-core real-time simulation platform (EMC-RTP) for a biological-faithful computational network model of basal ganglia (BG). The single neuron model is implemented in a highly real-time manner using a reasonable simplification. A modular mapping architecture with hierarchical routing organization was constructed to mimic the pathological neural activities of BG observed in parkinsonian conditions. A closed-loop simulation testbed for DBS validation was then set up using a host computer as the DBS controller. The availability of EMC-RTP and the testbed system was validated by comparing the performance of open-loop and proportional-integral (PI) controllers. Our experimental results showed that the proposed EMC-RTP reproduces abnormal beta bursts of BG in parkinsonian conditions while meets requirements of both real-time and computational accuracy as well. Closed-loop DBS experiments using the EMC-RTP suggested that the platform could perform reasonable output under different kinds of DBS strategies, indicating the usability of the platform.**

***Index Terms*— Basal ganglia, deep brain stimulation, real-time simulation, multi-core calculation.**

I. Introduction

PARKINSON'S disease (PD) is a neurodegenerative disorder with progressive motor and non-motor symptoms [1], [2], which is commonly seen in the middle-aged and elderly population [3]. Apart from static tremor, myotonia, and some non-motor symptoms [4], abnormal brain oscillatory activities are a typical clinical manifestation of PD [5]. As an alternative of medical [6]–[8] and surgical treatments [9], [10], deep brain stimulation (DBS) is a device-based therapy that has high efficiencies and fewer side-effects in clinical treatment for PD [11]. This therapy uses a stereotactic technique to implant microelectrodes into the Basal Ganglia (BG) [12], [15], the focal area of PD, and to emit continuous high-frequency electrical pulses to stimulate targets including the subthalamic nucleus (STN) or the globus pallidus interna (GPi) with the aim of diminishing abnormal brain rhythms to alleviate disease symptoms [13]–[16].

Parameters such as amplitude, frequency and pulse width of the DBS waveform directly determine the effectiveness of the treatment [17]–[19]. Therefore, failure to optimize stimulation waveform may account for suboptimal clinical outcomes. Traditional approach to optimize stimulation mostly relies on the clinician's experience or on the use of the traversal method which is artificially adjusted based on observed clinical effects [20]–[22]. This approach not only requires tremendous number of resources and time but also still may fail to identify personalized strategies owing to individual variabilities of different patients. Moreover, because subject's response to simulation can and does vary from time to time [23]–[26], continuous long-duration stimulation with fixed mode i.e., open loop DBS (op-DBS) can induce excess or shortage of stimulation which may cause a low success rate of the pre-optimized strategy [11], [27]. In response to overcome these drawbacks, closed-loop DBS (cl-DBS) approaches were gradually developed [18], [22], [28]. It is essentially a controller that receives the neural signal from the patient and automatically determines the stimulation parameters in conjunction with the normal state of the neural signal as a reference signal [29]–[31]. Different physiological signals such as action potentials (APs) [28], [32], local field potential (LFP) [33]–[35] and electrocorticogram (ECoG) [36], [37] have been used as feedback in the cl-DBS systems. It has been proven that abnormal oscillations of the LFP in the beta frequency band in cortical-BG circuits is correlated with normal movement suppression and motor impairment in PD,

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and became the most used biometric for assessment and treatment thusly [33]–[35].

Closed-loop experiments for improving the reliability and validity of control strategy are the necessary step of clinical DBS treatment for a patient. However, considering factors such as ethics, huge experimental risks and costs, it is not allowed to do a large number of reproducible experiments directly on humans. Therefore, the use of computational models to simulate the properties of relevant physiological structures, characterize the relationship between DBS and neural responses, and generate alternative data thus replacing the specific brain circuits as the controlled object, provides an effective solution to cross the gap between the theoretical design and clinical application of cl-DBS [36], [37]. Different models of BG network have been constructed to participate in this procedure. The conductance-based network model of basal ganglia and thalamus proposed by Rubin and Terman laid the ground work on the theoretical analysis of DBS effects [38].

Nevertheless, many computational methods were only validated using non-real time numerical stimulation tools. To ensure the effectiveness of the control strategy and make it easier to interface with the DBS stimulation device, it is essential and feasible to build a hardware real-time testbed for pre-clinical trials, which is important to promote the clinical application of cl-DBS in PD treatment. Many researchers have done a lot of work on hardware implementation of biological neural networks for closed-loop experiments. Park *et al.* presented a 128-channel field-programmable gate array (FPGA)-based real-time closed-loop bidirectional neural interface system [39]. Piri *et al.* constructed a complete digital circuit of the close loop system that is the bio-inspired stimulator and the cortical population model are implemented in hardware based on the dynamic model of astrocyte [40]. Hardware implementations such as FPGA and large-scale integrated circuits could be difficult and costly to develop. We want a hardware platform with high computing capability, low power consumption, and scalability to be designed and built. For a large number of nonlinear operations, this platform needs to draw on the advantages of the above work to achieve multi-core parallel computing and schedulability through a specific architecture to accomplish the aforementioned real-time simulation of neural networks. It also overcomes the deficiencies of hardware means such as FPGAs for floating-point multiplication. The ARM architecture series of microcontrollers (MCU) has received a lot of attention in the industrial sector in recent years due to its good working characteristics and low cost and easy development. However, such MCUs are less used in hardware neuron implementation.

In this context, we developed an embedded multi-core real-time simulation platform (EMC-RTP) using STM32 MCU. Based on the physiological structure of BG, the mapping scheme between neural network and hardware structure is designed. The implementation of BG is completed in EMC-RTP and used as a testbed to construct a complete cl-DBS real-time optimization system with host computer included. After verifying the implementation of EMC-RTP, the performance of different controller could be validated and compared using this closed-loop testbed. The innovations of this work include three aspects.

1) Based on the core requirement of real-time, a simplified approach to the selected original BG network model is proposed. The analysis of the simulation results proved that the modified model can substantially improve the computational speed during hardware implementation while ensuring accuracy.
2) An EMC-RTP for BG network hardware implementation was built using an STM32 MCU. Single neuron optimization model building was completed. Based on the mapping of the BG network to the hardware architecture topology, the hierarchical architectural design and construction of the EMC-RTP is completed. Point-to-point delivery of discharge information is accomplished through a customized data frame format and routing propagation mechanism.
3) A real-time closed-loop testbed system for DBS was built using the EMC-RTP as the control object to verify its usability, and the performance of DBS modulated with different approaches including open-loop controller (op-C) and proportional-integral controller (PI-C) was validated and compared from the view of both control effect and stimulation energy consumption.

The rest parts of this paper are organized as follow. The BG network computational model used for hardware implementation is introduced in Section II. Section III briefly describes the optimization process of the model and verifies the feasibility of this approach. Section IV describes the EMC-RTP building process and the way it was applied to build the closed-loop simulation testbed for confirmatory DBS experiment. Section V shows the results of the platform runs, including the dynamical activity of the hardware BG network within EMC-RTP and the effect of a simple validated DBS optimization experiment, and analyzes the operating performance metrics of the platform. Finally, Section VI concludes this article.

II. Computational Model of the BG Network

We used the BG network model developed by Rosa *et al.* [41] to build the platform. The network consists of STN, GPe, GPi and TH. There are several, 16 in this paper, neurons in each nucleus. The network and connectivity patterns of individual neurons were illustrated in Fig. 1, in which the number of excitatory/inhibitory inputs received by each neuron is indicated by the number of arrows. For thalamic cell, apart from the inhibitory input from a single GPi neuron, it receives the input signal from the motor cortex of the brain. The model can simulate the discharge activities of the nuclei in BG network in normal state, PD state and under DBS. The expressions for the neurons are shown below:

$$C_m \frac{dv_{STN}}{dt} = -I_L - I_K - I_{Na} - I_T - I_{Ca} - I_{AHP} - I_{GPe\rightarrow STN} + I_{\text{app\_STN}} + I_{DBS} \quad (1)$$

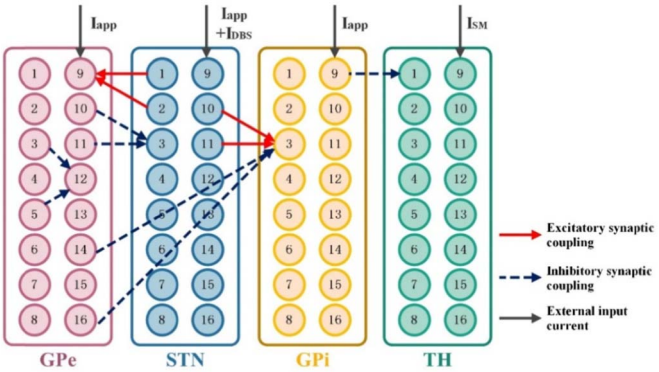

Fig. 1. BG network connection schematic.

$$C_m\frac{dv_{GPe}}{dt} = -I_L - I_K - I_{Na} - I_T - I_{Ca} - I_{AHP} + I_{GPe\to GPe} - I_{\mathrm{STN}\to\mathrm{GPe}} + I_{\mathrm{app\_}GPe} \quad (2)$$

$$C_m\frac{dv_{GPi}}{dt} = -I_L - I_K - I_{Na} - I_T - I_{Ca} - I_{AHP} - I_{GPe\to GPi} - I_{STN\to GPi} + I_{\mathrm{app\_}GPi} \quad (3)$$

$$C_m\frac{dv_{TH}}{dt} = -I_L - I_K - I_{Na} - I_T - I_{GPi\to\mathrm{TH}} + I_{SMC}. \quad (4)$$

Here v_{cell} are the membrane potentials of neurons, $C_m = 1\mu F/cm^2$ is the membrane capacitance, I_L, I_K, I_{Na}, I_T, I_{Ca}, I_{AHP} and I_{app} are the leak current, the sodium current, the potassium current, the low-threshold calcium current, the high-threshold calcium current, the after hyper polarization potassium current and the bias current, separately. $I_{\alpha\to\beta}=g_{\alpha\to\beta}(v_\beta - E_{\alpha\to\beta})\sum_j S_\alpha^j$ describes the sum of all synaptic currents from the presynaptic membrane cell α to the postsynaptic membrane cell β, where $\sum_j S_\alpha^j$ refers to the sum of the conductance of all presynaptic membrane cells α, positive for excitatory signals and negative for inhibitory signals. I_{SMC} in the thalamic neuron model is a single pulse with an amplitude of $3.5\mu A/cm^2$, a pulse width of 5ms, and a frequency of 14Hz, representing the stimulation current from the motor cortex of the brain. In this model, TH neurons in the normal state will follow the I_{SMC} to produce firing, and the PD state will produce firing failure phenomenon, thus characterizing the different physiological states. Particularly, the LFP of GPi nucleus is used as the neural signature in the following experiments, of which the expression is

$$\mathrm{LFP} = I_{GPe\to GPi} - I_{STN\to GPi} + I_{\mathrm{app\_}GPi}. \quad (5)$$

The rest of the expressions in the above model and the values of the parameters involved are listed in the appendix.

III. Modified BG Network Model and Validation for Hardware Implementation

A. Model Simplification

The core requirement and advantage of the hardware BG network proposed in this work is the real-time performance. However, limited by the operating frequency and resources of the selected MCU, a simple attempt proved that it is difficult to meet this requirement with a direct implementation of the above model using standard library functions. We evaluated the time overhead of each step in the hardware porting process of the above model. It is proven that the calculation of the transmembrane ion current and its intermediate variables is the most time-consuming, thus indicated a reasonable simplification of the neuron model is necessary. Further software debugging illustrated that the excessive calculation of the exponential function in the above step led to this phenomenon. Therefore, we use the following formula instead of the standard exponential operation:

$$e^x = \lim_{n\to\infty}(1 + x/n)^n. \quad (6)$$

For example, the equation for the gating variable m_∞ in the original STN model is

$$m_\infty(v) = 1/(1 + \exp(-(v + 30)/15)). \quad (7)$$

This equation is then rewritten as

$$m_\infty(v) = 1/(1 + (1 + (-(v + 30)15n))^n). \quad (8)$$

The computational accuracy increases as n increases, but it is also more time consuming. Therefore, the feasibility of this simplified approach and the variation of error and time overhead with n are discussed next using software method.

B. Modified Model Evaluation

The accuracy of the modified model is described by the following two metrics. The first one is the root mean square error (RMSE), which is defined as:

$$RMSE = \frac{1}{N}\left(\sum \frac{(x_o(i) - x_m(i))^2}{x_o^2(i)}\right)^{1/2}, \quad (9)$$

where $x_o(i)$ and $x_m(i)$ represent the value of original function and modified function, respectively. N represents the amount of sampling points. Using the normalized RMSE, we further define the second accuracy metric as:

$$ACC = \left(1 - \frac{RMSE}{x_{\max} - x_{\min}}\right) \times 100\%. \quad (10)$$

To evaluate the performance of the simplified model in terms of time overhead, we define the computational efficiency as:

$$R_C = t_m/t_a, \quad (11)$$

where t_m and t_a represent the time overhead of the solving process of modified functions and original functions, respectively. The time consumption comparison process is performed in the MCU.

We selected the STN model as an example to validate the above metrics at four levels: gating variables, intermediate variables, transmembrane currents and membrane potentials. The selected variables are $h_\infty(v)$, h, I_{Na}, and v_{STN}. The variation of the above metrics at different values of n was tested first. The reason for choosing n as an exponential power of 2 is to replace the standard function with repeated

TABLE I
MODIFIED STN MODEL PARAMETERS CALCULATION ERROR ($N = 2^{10}$)

Parameters	RMSE	ACC (%)
I_L	0.0034	99.9986
I_{Na}	0.0085	99.9993
I_K	0.0070	99.9970
I_T	0.0015	95.0920
I_{Ca}	0.0014	99.9912
I_{AHP}	0.0016	99.9966
h	0.000679	99.9321
n	0.000480	99.9075
r	0.000668	99.9119
c	0.000426	99.7911
$[Ca]$	0.000013	99.9963
v_{STN}	0.0070	99.9140

multiplications, further optimizing the time overhead. This procedure can be described in detail as

$$\left.\begin{array}{l} x := 1 + x/2^k \\ x := x^*x \\ \vdots \\ x := x^*x \end{array}\right\} (ktimes). \tag{12}$$

It avoids the need to use a circular structure for a specific number of multiplications, and can make full use of the powerful floating-point computing power of the FPU to ensure the real-time performance of the simulation.

The validation of $h_\infty(v)$ expression was performed in the range of values containing the membrane potential of the STN neuron. The chosen range is $[-80,50]$ with a step size of 0.01mV. The validation of h , I_{Na}, and v_{STN} were then performed for the complete simulation of the STN neuron with a simulation time of 2000 ms and a step size of 0.02 ms. The variation of ACC and R_C with n is shown in Fig.2. It can be seen that the accuracy of the simplified model gradually increases as n increases, and at the same time brings about a decrease in the computational speed. However, the computational efficiency is still greatly improved. Eventually, n was chosen to be 2^{10} to achieve a good compromise between real-time performance and accuracy of the hardware implementation of the neuron model.

Table I shows the error of each ion current versus membrane potential in the optimized model. In this way, the modified model can improve the computational speed to about 11 times of the original model the calculation error of the membrane potential is less than 0.1%, providing the possibility of real time implementation of the BG network. The modified models of the remaining three nuclei are verified to meet the accuracy and real-time requirements as well. The above experimental and analytical results demonstrate that this approach can be applied to the hardware implementation of the BG network model.

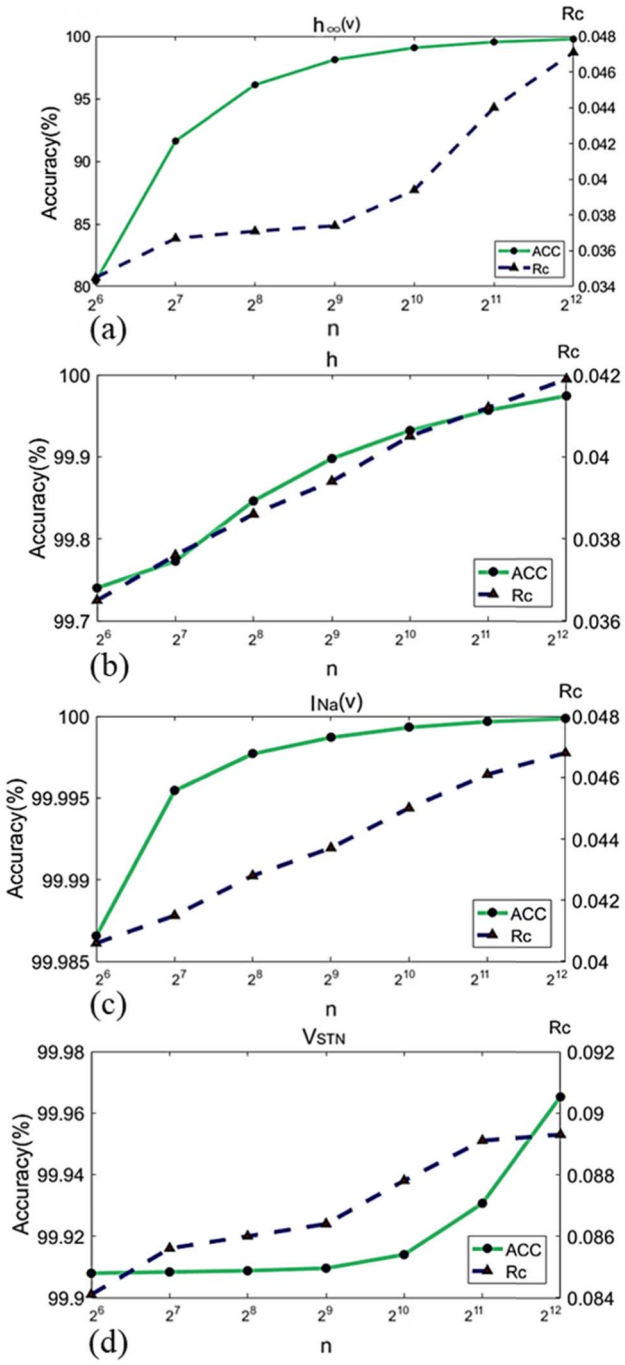

Fig. 2. The relationship between the computational accuracy and real-time performance of the simplified model and the parameter n.

IV. EMC-RTP CONSTRUCTION AND BG NETWORK IMPLEMENTATION

A. BG Network Model Mapping and Chip Selection

Before the concrete implementation of the multi-core platform, the first task is the structural correspondence of these chips to the BG network model, i.e., the mapping process. Corresponding to the structure of the model mentioned above, we divided the system design into two parts by function. From this perspective, the platform needs to implement two

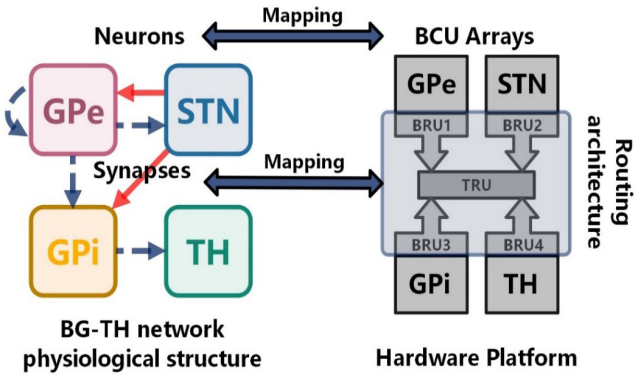

Fig. 3. Mapping mechanism between BG network and the hardware platform.

major functions, including model multi-core parallel solving and routing communication scheduling. For each individual neuron in the BG network, the first part is assigned to complete the solution of the model of them. We name the chip that accomplishes this task the basic computing unit (BCU). Corresponding to the synaptic connections among neurons, the other part is responsible for passing the discharging information between BCUs and coordinating the parallel computing process of them. On this basis, a 2-layer hierarchical routing organization structure consisting of 5 chips is built to organize them. There are 4 bottom routing units (BRUs) and one top routing unit (TRU). Each of the 4 BRUs corresponds to the 4 nuclei separately, while TRU is connected to them at a higher level, forming a hierarchical routing structure. This mapping mechanism between the neural network and the platform structure is shown in Fig.3.

The core requirement for EMC-RTP is to fulfill the requirements of real-time performance. Besides, low power consumption and scalability under the guarantee of a certain neural network scale are preferred. Consequently, it is necessary to choose a universal and high-performance embedded processor equipped with abundant peripherals and energy-efficient. After comparison, we selected the STM32F407 model MCU based on ARM 32-bit Cortex-M4 architecture as the core CPU. It integrates floating-point unit (FPU) and supports for the DSP instruction set, which make it particularly suitable for scenarios requiring a large number of floating-point operations. It is completely free from the multiplier resource limitation of FPGA, providing a guarantee for real-time neural network simulation.

B. Single Neuron Hardware Implementation

Following the aforementioned mapping mechanism, the first task to be completed was the implementation of the single neuron model in BCU. We discretized the neural model expressed as a system of differential equations as follow:

$$\begin{aligned} v_{STN}(k+1) = v_{STN}(k) + \frac{\Delta t}{C_m}(&-I_L - I_K - I_{Na} - I_T - I_{Ca} \\ &- I_{AHP} - I_{GPe\to STN} + I_{\text{app\_STN}} \\ &+ I_{DBS}) \end{aligned} \tag{13}$$

$$\begin{aligned} v_{\text{GPe}}(k+1) = v_{\text{GPe}}(k) + \frac{\Delta t}{C_m}(&-I_L - I_K - I_{Na} - I_T - I_{Ca} \\ &- I_{AHP} + I_{GPe\to GPe} - I_{STN\to GPe} \\ &+ I_{\text{app\_}GPe}) \end{aligned} \tag{14}$$

$$\begin{aligned} v_{\text{GPi}}(k+1) = v_{\text{GPi}}(k) + \frac{\Delta t}{C_m}(&-I_L - I_K - I_{Na} - I_T - I_{Ca} \\ &- I_{AHP} - I_{GPe\to GPi} - I_{STN\to GPi} \\ &+ I_{\text{app\_}GPi}) \end{aligned} \tag{15}$$

$$\begin{aligned} v_{TH}(k+1) = v_{TH}(k) + \frac{\Delta t}{C_m}(&-I_L - I_K - I_{Na} - I_T \\ &- I_{GPi\to \text{TH}} + I_{SMC}). \end{aligned} \tag{16}$$

These equations were solved using the forward Euler method. Here the k in the above equation represents the number of iterative steps. Δt represents the time step, which means the time that the neuron corresponding to each computational cycle passes in the real environment. Shorter a step time will bring higher simulation accuracy, but it is hard to achieve real-time simulation. Too long a step time can lead to distorted simulation results. The appropriate step time should be chosen to achieve a compromise between simulation real time and accuracy. Here we choose $\Delta t = 0.02ms$ after experimental verification. Within the platform, the operation time step is controlled by the timer interrupt provided by the MCU.

The experimental process of the single neuron model is roughly divided into intermediate variable calculation, transmembrane current calculation, state variable update, discharge state and other information output, and historical data storage. The specific flow of the above implementation is briefly illustrated in Fig.4, which depicts the two interrupt function processes for state equation solving and synaptic variable updating. Although in principle the number of neurons within a BCU can be chosen arbitrarily, we implement only one neuron model in each BCU under the premise of ensuring real-time performance. The core process of the neuron model hardware implementation is the model computation within the timer interrupt. This process uses the simplified approach presented in Section III, while using the float point unit (FPU) integrated within the MCU, which greatly reduces the computation time and thus ensures that the time scale of this process is consistent with the real process.

C. Hierarchical Routing Architecture Design

After completing the implementation of each neuron in the BCU, these 64 chips were set as the bottom layer of the whole platform. Next, the hierarchical routing organization architecture is constructed. The design requirements of this part are to complete the point-to-point propagation of discharge time among the underlying BCUs, to achieve reasonable scheduling of multi-core parallelism, and to build a hardware neuron network. Specialized routing units are used to obtain and integrate the discharge information. To better explain the design inspiration of this segment, we first discuss the synaptic current in the model, i.e., $I_{\alpha\to\beta}$, in a more detailed manner. As introduced in Section II, the expression for the synaptic current is $I_{\alpha\to\beta}$=$g_{\alpha\to\beta}(v_\beta - E_{\alpha\to\beta})\sum_j S_\alpha^j$, where both g and E are constants for the determined neuron.

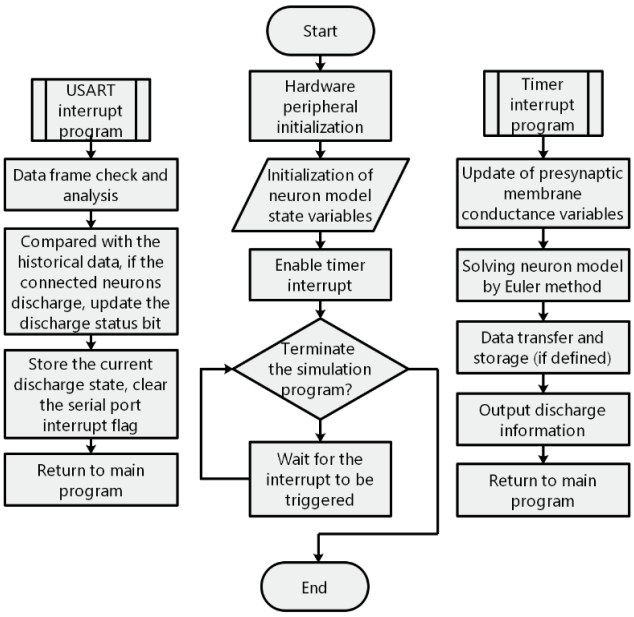

Fig. 4. Flow chart of single neuron implementation in BCU.

And the conductance S of a single presynaptic membrane cell is determined by the following set of second-order differential equations:

$$\begin{cases} dS/dt = z \\ dz/dt = 0.234u(t) - 0.4z - 0.04S. \end{cases} \tag{17}$$

During the computation, u(t) = 1 if the membrane potential of the presynaptic cell crosses the threshold of −10 mV at the moment t, which means that the presynaptic cell has generated an action potential. Otherwise, u(t) = 0. For synaptic connection like this, the postsynaptic membrane cell only needs to obtain information about whether the presynaptic membrane cell has generated an action potential or not. Such a mechanism is very suitable to be implemented in our platform. Fig.5 depicts the generation of discharge information and the mechanism of data frame generation and delivery. We select one general-purpose I/O(GPIO) port in each BCU to be multiplexed into normal output mode. It is set high when action potential is generated, otherwise it is set low, which representing the status of the presynaptic cell. In this way, the discharge information can be obtained simply by reading the state of this pin. The synaptic model is integrated into the BCU and solved together with the neural model, which greatly reduces the time and resource cost of information transfer.

On this basis, each BRU is connected to 16 GPIO ports, ones are used as the membrane potential state output of the 16 BCUs within the group. By continuously polling the BCUs connected to it, a data frame indicating the current discharge status is generated. The data frame is 8 bytes in length and consists of three sets of discharge information and tail validation, with each of the four parts occupying 2 bytes. During the reading procedure, if a GPIO port is in the high level, the corresponding bit in the data frame is set to 1 by the BRU, otherwise it is set to 0. After completing the acquisition, it is transferred to TRU. When data frames are received from the BRUs, the TRU consolidates them by analyzing the sources. Finally, a data frame describing the current state of all neural potentials is generated uniformly and down streamed to all BRUs. To prevent redundant processing, the BRU upload process is performed only when the underlying neural discharging state changes. Similarly, the BRUs perform a comparison when they receive the downstream data frame. Only when the discharging information of the connected nuclei changes, it is transferred uniformly to the underlying BCUs. By combining the tail and length checks of the data frame, this process allows for simple, efficient, accurate and complete information processing and transfer.

To implement the connectivity patterns described in Section II and determine the presence or absence of connections between two specific neurons, we number the BCUs in each nucleus. After receiving the data frame, the BCU reads the discharge information of neurons that have connections within itself and performs the update of presynaptic membrane conductance variables. For example, without loss of generality, GPe neuron #1 receives the inhibitory input from GPe neurons #2 and #3. Thus, in a loop, this BCU gets the GPe input by reading only bits 2 and 3 of the GPe part of the data frame and calculating the synaptic current. This connection can also be changed arbitrarily by programming.

The above communication processes are implemented by the chip-integrated universal synchronous/asynchronous receiver/transmitter (USART). It is important to select as high a transmission speed as possible in the work to ensure that a sufficiently high data throughput rate is provided. It can be seen that each BRU and the 16 BCUs it controls form a well-connected network of modular basic operator groups. This group can be easily replicated and scaled up as chip resources allow. It is also possible to change the number of BCUs within an operator group.

Based on the above mechanism, a total of 69 STM32 chips are used to build the EMC-RTP. Through reasonable allocation and organization, the scaled parallel operation is completed. This organization allows for a good hardware implementation of the BG network model in real time. At the same time, the platform equips the BCU with a large enough storage facility to store the required historical data and leaves enough peripheral resources for expansion.

D. Closed-Loop Simulation Testbed Construction for DBS Experiments

After the completion of construction and BG network porting, the EMC-RTP can be considered as an independent system with external interfaces. We next use this platform as the controlled object to build a closed-loop system to verify its usability in the DBS optimization process and to compare the effects of different DBS control strategies. Fig.6(a) shows the structure of the testbed for DBS optimization experiments. The EMC-RTP is used to stimulate neural dynamic activities and can be regarded as a virtual BG which can switch between normal and PD state to generate surrogate data. The switching between the normal and PD states is achieved by changing

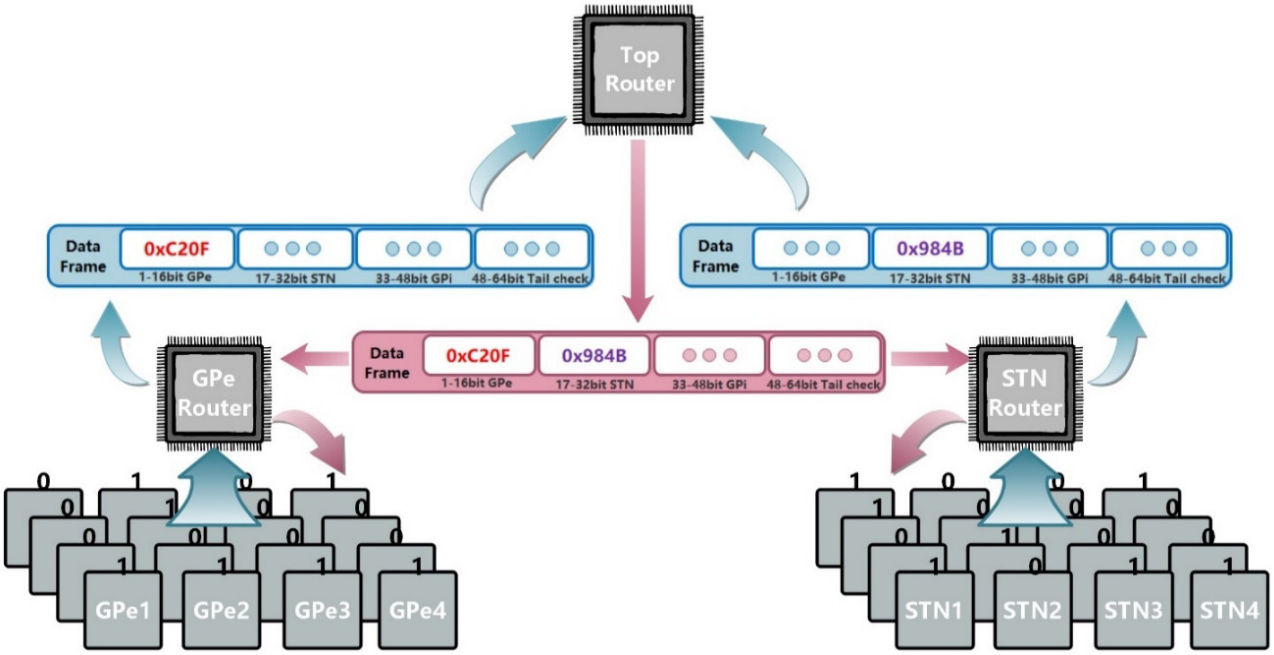

Fig. 5. Discharge information data frame format and routing delivery mechanism.

the bias current I_{app} of the three nuclei groups, STN, GPe and GPi (see Table VIII in Appendix). We thus define a Boolean type flag within each BCU. When the model state needs to be switched, a command to change the flag bit is issued to all BCUs via the TRU, which changes the value of I_{app} to achieve the switch between normal and PD states.

The storage of operational data can be adjusted according to requirements. Generally speaking, a small amount of data can be stored in integrated RAM, of which the maximum capacity is about 700-800ms of historical data when storing only one variable such as membrane potential with a simulation step time of 0.02ms. For long time data storage, such as the experiments carried out afterwards, the BCU supports SD card as extended memory. In this way, the data storage capacity is greatly enhanced. A 32GB SD card, for example, can store about 47 hours of simulation data.

In this work, the controller part is implemented in the host computer by software means. The process of closed-loop experiments requires the implementation of several processes: feedback signal sampling, controller calculation and control variable transfer. The sampling and output parts involve data transfer between the host computer and EMC-RTP. We use the reserved USART to connect these two modules to achieve this function, thus closing the loop. During the experiment, the data to be collected which is generated by the hardware BG network is transmitted to the host computer according to the set sampling frequency. We designed a variable as a counter for the iterative loop during the operation. A data transfer is initiated when the count value reaches the set amount of data. The DBS waveform generation is implemented in the platform based on the received parameters. Fig.6(b) is the physical diagram of the testbed. An oscilloscope is used to visualize the Digital/Analog (D/A) converted output of the hardware BG network. The construction of this system laid the foundation for the DBS validation experiments carried out next.

V. Results

A. Hardware Modified Single Neuron Model Dynamic Activities

Single neuron models of the four nuclei were first implemented independently in the BCU to verify the ability of the transplantation method. This process is done in the STM32 MCU using the modified model described in Section III. The first verification performed is the accuracy of each variable in the hardware implementation. We selected the intermediate variables H, the ionic current I_{Na} and the membrane potential v_{STN} in a single STN neuron for comparison with the MATLAB simulation results of the original model. The results are shown in Fig.7. It can be seen that the implementation of the optimized model in hardware only introduces a certain error near the peak of the action potential and is completely controlled within acceptable limits.

On this basis, since the DBS used in the subsequent experiments was applied to the STN nuclei, we tried to apply different amplitudes of DBS to the STN neurons using a controller implemented in the host computer to ensure that they could produce timely and accurate responses to the control output. The results are shown in Fig.8(a). It can be seen that the STN neurons gradually increase the frequency of firing with the increase of DBS intensity. Moreover, since only the transmission of DBS parameters is performed during the output of the control volume, the control delay is greatly reduced and the STN can produce a response in a very short time.

The implementation of synaptic current $I_{\alpha\to\beta}$, which has a similar mechanism to the I_{DBS} was also experimentally

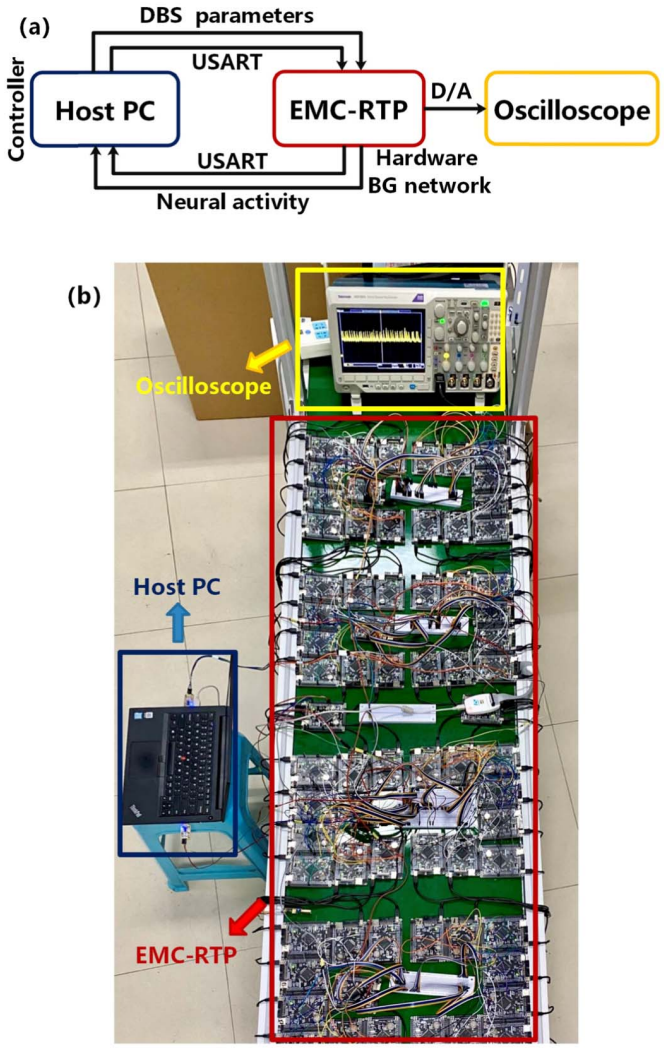

Fig. 6. (a) Schematic of the closed-loop simulation testbed for DBS experiment. (b) Physical diagram of the DBS simulation experiment testbed.

verified. We selected a GPe neuron and transmitted a data frame to it to simulate the action potential received from the presynaptic neuron under a certain moment. The results of the implementation of the synaptic current model are shown in Fig.8(b). The GPe neuron also produced a rapid response. The above experimental results demonstrate the accuracy of our proposed single-neuron implementation mechanism, while the information processing process integrated within the BCU ensures the feasibility of the establishment of a real-time network.

B. Simulation Results of BG Network in EMC-RTP

In this section, we ran the EMC-RTP individually to verify that the designed hardware implementation can accurately reproduce the oscillatory activity characteristics of the BG network in healthy and PD states. Regarding the characteristics of PD, two mainstream views were selected for assessment. One is the diminished or even loss of thalamic response to sensorimotor cortex (SMC) input, i.e., thalamic relay capacity, and the other is the enhancement of Beta band (13-30Hz)

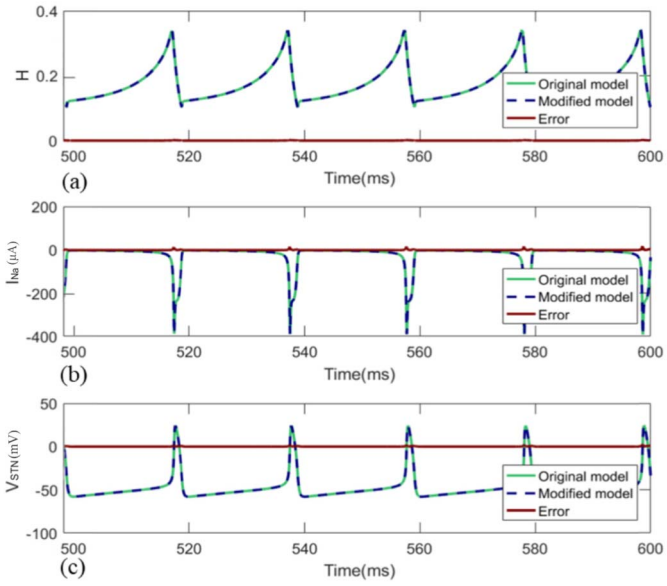

Fig. 7. Comparison of simulation results between the hardware modified model and the original model.

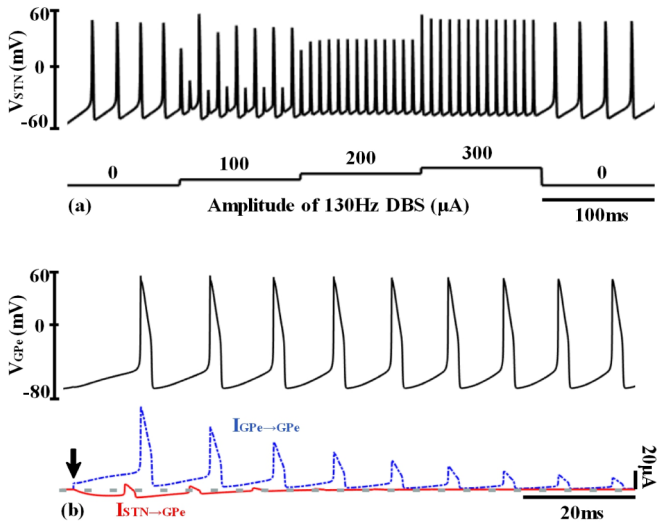

Fig. 8. (a) Response of single STN neuron under different amplitude DBS stimulation. (b) Results of the synaptic current model implementation in hardware single GPe neuron. The black arrow represents the moment when the data frame is received. The blue and red lines represent the input from GPe and STN neurons, respectively.

oscillatory energy in electrophysiological signals. We first ran the hardware BG network in normal and PD state, and the results are visualized by an oscilloscope, while the source data are collected via USART to a host computer for further analysis and processing. Due to the operating characteristics of the MCU, the output here is uniformly set between 0 and 3.3V, which is linearly proportional to the true amplitude. The model of the oscilloscope is Tektronix MDO3024.

The membrane potentials of the 4 nuclei are shown in Fig.9. From the time-domain characteristics, the GPe and GPi neurons in the PD state showed a significant burst discharge compared to the normal state, i.e., the synchronous discharge phenomenon. In addition, to show the response of the TH

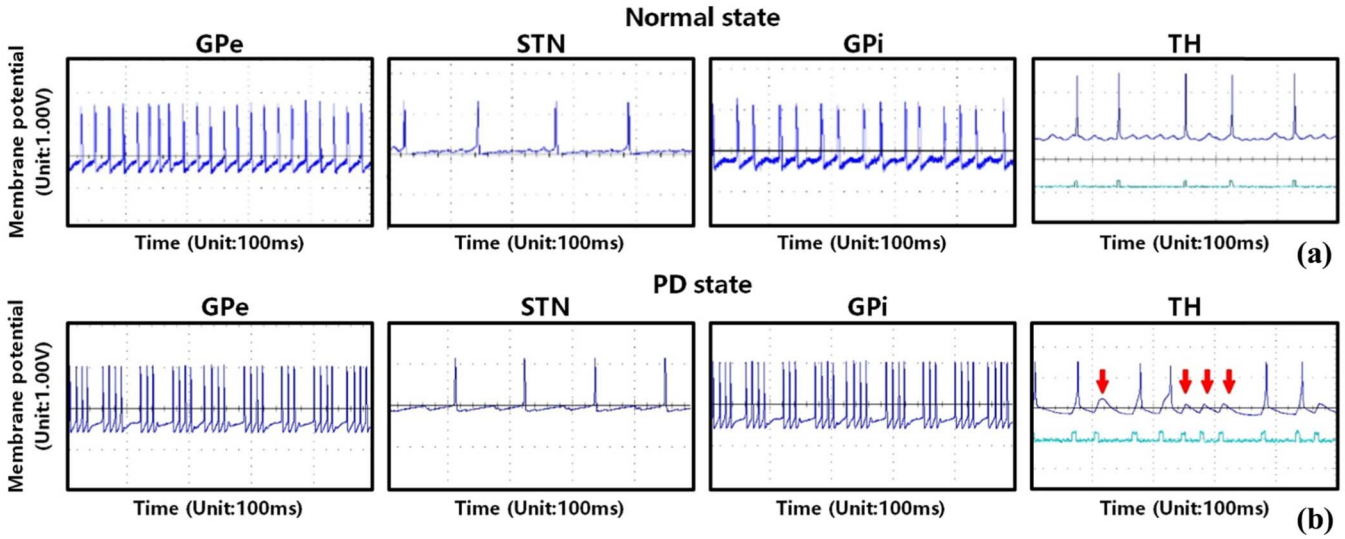

Fig. 9. Firing patterns of the 4 nuclei in hardware BG network in (a) healthy and (b) PD state.

neuron to the I_{SMC} input, we used a dual-channel display and acquired both the membrane potential of TH and the input simultaneously. It can be seen that the TH neurons in the PD state showed a response deficit, which are marked with red arrows. This phenomenon is consistent with the first view of measuring PD status.

We next collected the LFP of the GPi nucleus and performed a power spectrum analysis of this sequence to further illustrate the anomalous Beta oscillations of BG network in PD state. As shown in Fig.10 (a) and (b), the energy of the LFP in the PD state is significantly higher in the Beta band than in the normal state, which is found to be correlated with the PD symptoms. These results demonstrate the ability of EMC-RTP to reproduce the characteristics of the BG network in both states.

C. Confirmatory Experiment Results Under Op-DBS and CI-DBS

To verify that EMC-RTP can be applied to cl-DBS experiments and to observe the response of hardware BG networks under the application of DBS, we next perform the DBS parameter optimization experiments within the built simulation testbed system. The DBS used in the experiments

was a bipolar rectangular wave, and the parameters controlled included stimulus amplitude and frequency. To ensure the clinical safety and usefulness of the DBS parameters, the amplitude u_A as limited to 200-400μA

and the frequency u_f was limited to 100-200Hz. The pulse width was not used as a control parameter and was fixed at 0.3ms [41].

Op-C and PI-C are implemented separately in the host computer. For Op-C, of which the control output is a set of fixed parameters, the experiment procedure is rather simple. The DBS is exerted to STN nucleus directly from the host PC with the hardware BG network running in the PD state. The ODBS in the following experiment is a square wave with a frequency of 130Hz, an amplitude of 3mA and a pulse width

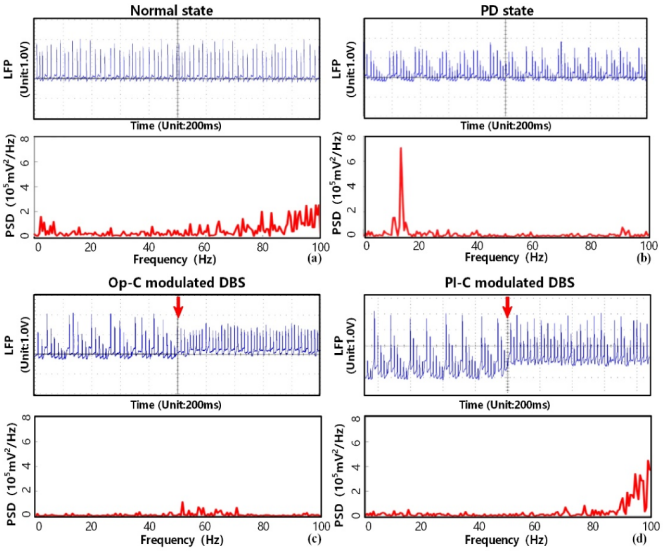

Fig. 10. LFP of GPi and its power spectrum in normal, PD and different kinds of DBS stimulated state.

of 0.3ms. The purpose of DBS stimulation is to eliminate abnormal oscillations, and we therefore chose the Beta band energy of the LFP of GPi nucleus as a feedback and control indicator. We first run the hardware BG network in normal state independently and collect LFP data with the sampling frequency as 1kHz to get the reference input. These data are divided into equal length time windows, i.e., control periods. In each time window, the LFP is band-pass filtered, then the oscillation activity power is calculated using Welch method of power spectral density estimation. We accumulate the energy in the Beta band to obtain the biometric

Z_k used for control, where k represents the number of the time window. The length of the time window in the experiment was set to 0.5s. The PI-C algorithm is described as

$$u_k^* = k_p \cdot e_k + k_i \cdot \sum_{i=0}^{n} e_k, \tag{18}$$

where u_k^* represents the control output, e_k represents the error, n represents the total of time windows, k_p and k_i are the controller parameters and the adjustment process of which is carried out empirically. We set $k_p = 5$ and $k_i = 0.5$ in the experiments.

The experiment results of the EMC-RTP working under different type of DBS are shown in Fig.10 and Fig.11. In the experiments of TH on SMC input relay capability, both of them were able to bring this indicator back to normal from the PD state. However, as can be seen in Fig.10 (c) and (d), although the op-C modulated DBS can be useful in the suppression of anomalous oscillations, the energy of all bands is reduced. This demonstrates that op-DBS may cause adverse effects on the patient or even new diseases may be induced due to the brain overstimulation. Besides, the energy consumption of a DBS stimulus W_I is defined as the root-mean-square (RMS) of its stimulus current value per unit time, which is described as

$$W_I = \sqrt{\frac{\sum_{i=1}^{t} I_{DBS_i}^2}{t}}, \tag{19}$$

where I_{DBS_i} represents the value of DBS current at the time i. Reducing the power consumption of DBS stimulation can prolong the life of the battery for the DBS stimulation device, thus can decrease the frequency of invasive surgeries [42], [43]. This metric was calculated to be $3.3 \times 10^4 \mu A/s^{1/2}$ and $2.0 \times 10^4 \mu A/s^{1/2}$ for op-C and PI-C, respectively. The above experimental results demonstrate the usability of the constructed EMC-RTP for closed-loop DBS experiments on the one hand, and reveal the advantages of cl-DBS over op-DBS in terms of more personalization and lower energy consumption on the other hand.

D. EMC-RTP Performance Evaluation

In this section we measure the working performance of the platform to discuss its strengths and weaknesses. First, we compared the difference in real-time performance between EMC-RTP and software simulation in CPU, and also analyzed the scalability of the platform in terms of the number of neurons implemented. We implemented different number of neurons in a BCU separately while performing simulations of the same scale within the software environment to observe the change in real-time performance. We define the model solving efficiency (MSE) as

$$MSE = t_s / t_a, \tag{20}$$

where t_s and t_a represent the time overhead of solving the neural network model and the real time of the same size model, respectively. In this experiment each iteration of EMC-RTP was shortened as much as possible in order to analyze its scalability at maximum working capacity. The clock speed of the MCU and the CPU used for comparison is 168MHz and 3.0GHz, separately. The software tool is MATLAB2020b. The experimental results are shown in Fig.12(a). It can be seen that as the number of neurons increases, the real-time performance of both is affected. However, EMC-RTP still has a significant advantage over the CPU by virtue of its multi-core parallel computing mechanism. The results also show that the working performance of the platform suffers when the number of neurons within a single core rises, limited by the complexity of the model. This is an issue that needs to be further explored in future work.

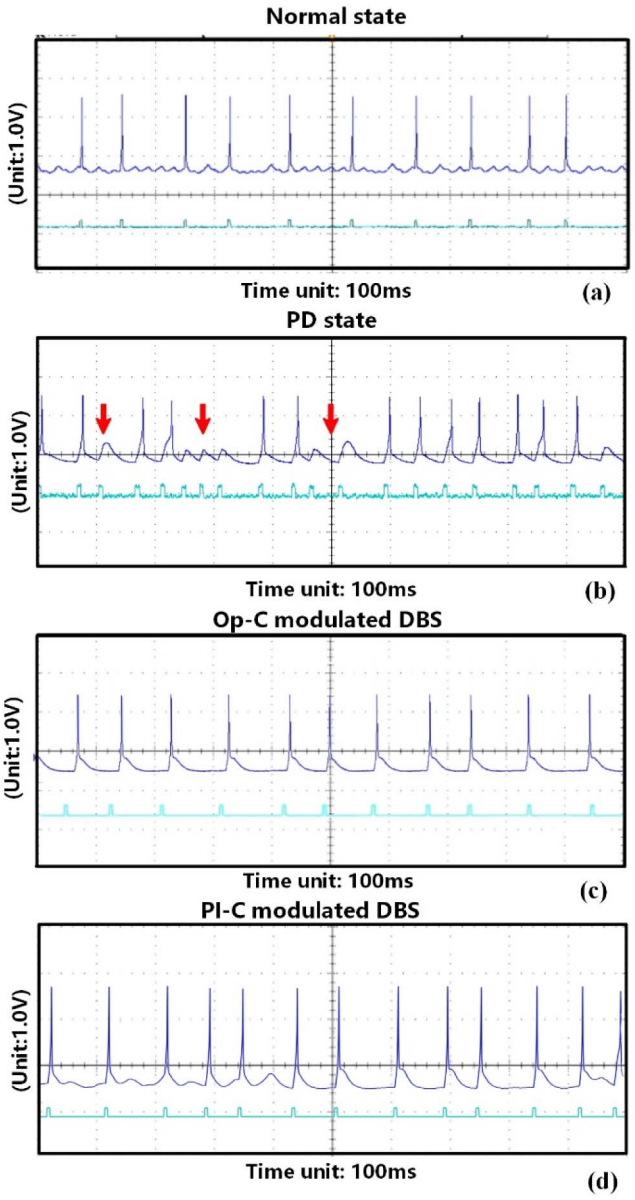

Fig. 11. Relaying of SMC input by TH neurons in different states.

Another noteworthy issue is that the delivery of data frames in the routing architecture built in this work is implemented using the serial interrupt, whose priority is higher than timer interrupts, the process of neuron model solving. It implies that if the platform size grows with the number of implemented neurons, too frequent discharge information transfer process could affect the real-time performance of the model computation. To analyze this operating performance of the platform, we selected a BCU and applied simulated data frame inputs of different frequencies to it with different chosen baud rate to observe the change in MSE.

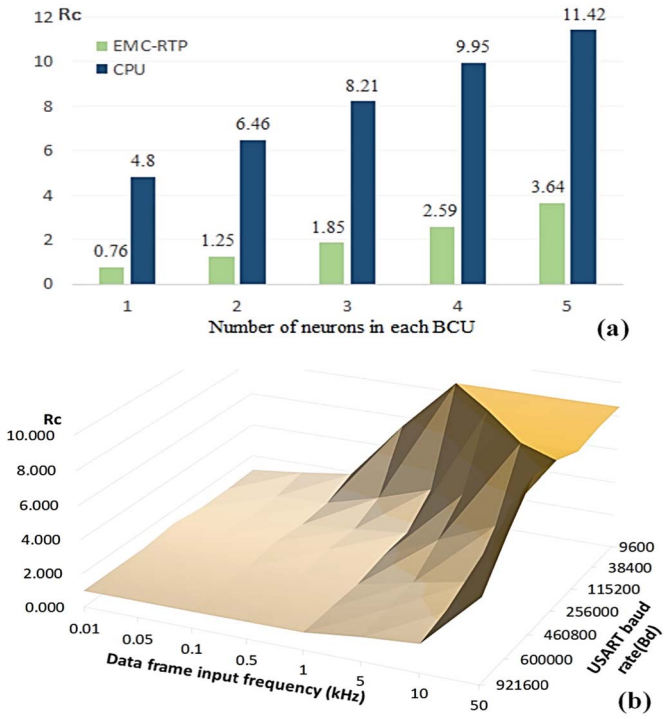

Fig. 12. (a) Comparison of hardware platform and CPU model solving efficiency. (b) The effect of data frame input frequency on the real-time performance of BCU computation at different baud rates.

TABLE II
POWER CONSUMPTION OF HARDWARE PLATFORM

MCU function	Nuclear type	Working current	Single chip power consumption
BCU	GPe	57.8 mA	0.191W
	STN	60.1 mA	0.198W
	GPi	61.0 mA	0.201W
	TH	56.4 mA	0.186W
BRU	-	41.4 mA	0.136W
TRU	-	42.8 mA	0.141W

TABLE III
RESOURCE COST OF HARDWARE PLATFORM

MCU function	Nuclear type	Single chip SRAM consumption	Single chip FLASH consumption
BCU	GPe	27.476KB (14.3%)	93.625KB (9.1%)
	STN	26.246KB (13.7%)	92.547KB (9.1%)
	GPi	24.832KB (12.9%)	92.320KB (9.0%)
	TH	22.004KB (11.5%)	91.633KB (8.9%)
BRU	-	10.738KB (5.6%)	25.680KB (2.5%)
TRU	-	10.262KB (5.3%)	26.195KB (2.6%)

Fig.12(b) shows the experimental results of the effect of data frame transmission on MSE. At the scale of the network implemented in this work, the average data frame transmission frequency is around 1 kHz, and the baud rate is chosen as 600000. The MSE of EMC-RTP won't be affected under this condition. However, even if at higher baud rates, the real-time performance of the platform will be compromised when the transmission frequency of the discharge information reaches around 10 kHz. At smaller orders of magnitude, this problem can be compensated by optimizing the computational efficiency of the BCU. However, as the number of chips and network size continue to increase, further exploration is required. For example, more optimized topologies or more efficient data frame delivery methods may be adopted to resolve the conflict between parallel computing network size and information delivery efficiency.

TABLE IV
TH MODEL EQUATIONS

Current Equation	Intermediate variables	Gating variables
$I_L=0.05(v+70)$		
$I_{Na}=3m_\infty^3(v)h*(v-50)$	$h'=\frac{h_\infty(v)-h}{\tau_h(v)}$	$h_\infty(v)=1/(1+e^{\frac{v+41}{4}})$ $\tau_h(v)=1/[0.128e^{\frac{-(v+46)}{18}}+4/(1+e^{\frac{-(v+23)}{5}})]$
$I_K=5[0.75(1-h)]*(v+75)$	$r'=\frac{r_\infty(v)-r}{\tau_r(v)}$	$r_\infty(v)=1/(1+e^{\frac{v+84}{4}})$ $\tau_r(v)=4.2+0.15e^{\frac{-(v+25)}{10.5}}$
$I_T=5p_\infty^2(v)rv$		

The hardware resource and power consumption of each part in the platform are listed in Table II and Table III. We measured the power consumption of the CPU for the same computing task in software, and the average value is about 17.32W. The EMC-RTP accomplishes the desired task with low hardware resource usage and power density.

VI. CONCLUSION

In this paper, the EMC-RTP for real-time BG network simulation is built. A simplified approach for the physiological model is chosen and validated, laying the foundation for large-scale real-time hardware implementations. A two-part system of basic computing units and hierarchical routing organization architecture is designed. Through the custom data frame structure and routing information processing mechanism, the multi-processor structured parallel operation is realized. The reasonably simplified hardware BG network was implemented using 69 STM32 MCUs. The closed-loop simulation testbed system was constructed on this basis, in which different DBS control strategies are validated and compared in real-time. The running results show that EMC-RTP can accurately reproduce the dynamical activity of the BG network with low power and resource consumption. The validated closed-loop experiments demonstrate the usability of the platform for future DBS optimization experiments.

As an exploratory design for cl-DBS, this work has the following limitations. Firstly, in terms of modeling, richer physiological properties were not introduced. Also, the use

TABLE V
STN MODEL EQUATIONS

Current Equation	Intermediate variables	Gating variables
$I_L=2.25(v+60)$		
$I_{Na}=37\mathrm{m}_\infty^3(v)h$ $*(v-55)$	$\mathrm{h}'=\frac{3[\mathrm{h}_\infty(\mathrm{v})-\mathrm{h}]}{4\tau_h(v)}$	$\mathrm{m}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+30}{15}})$ $\mathrm{h}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+39}{3.1}})$ $\tau_\mathrm{h}(\mathrm{v})=1+500/(1+e^{\frac{v+57}{3}})$
$I_K=45\mathrm{n}^4(v+80)$	$\mathrm{n}'=\frac{3[\mathrm{n}_\infty(\mathrm{v})-\mathrm{n}]}{4\tau_n(v)}$	$\mathrm{n}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+32}{8}})$ $\tau_n(\mathrm{v})=1+100/(1+e^{\frac{v+80}{26}})$
$I_T=0.5a_\infty^3(v)*\mathrm{b}_\infty^3(v)rv$	$\mathrm{r}'=\frac{\mathrm{r}_\infty(\mathrm{v})-\mathrm{r}}{5\tau_r(v)}$	$a_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+63}{7.8}})$ $b_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{0.4-r}{0.1}})$ $-1/(1+e^4)$ $\mathrm{r}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+67}{2}})$
$I_{Ca}=2\mathrm{c}^2(v-140)$	$\mathrm{c}'=\frac{2[\mathrm{c}_\infty(\mathrm{v})-\mathrm{c}]}{25\tau_c(v)}$	$\mathrm{c}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+20}{8}})$ $\tau_\mathrm{c}(\mathrm{v})=1+10/(1+\mathrm{e}^{\frac{v+80}{26}})$
$I_{AHP}=20(v+80)$ $*\mathrm{CA}/(CA+15)$	$\mathrm{CA}'=3.75*10^{-5}$ $(-I_{Ca}-I_T-22.5CA)$	

TABLE VI
GP MODEL EQUATIONS

Current Equation	Intermediate variables	Gating variables
$I_L=0.1(v+65)$		
$I_{Na}=120\mathrm{m}_\infty^3(v)h$ $*(v-55)$	$\mathrm{h}'=\frac{\mathrm{h}_\infty(\mathrm{v})-\mathrm{h}}{\tau_h(v)}$	$\mathrm{h}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+58}{12}})$ $\tau_\mathrm{h}(\mathrm{v})=0.05+0.27/(1+e^{\frac{v+40}{12}})$
$I_K=30\mathrm{n}^4(v+80)$	$\mathrm{n}'=\frac{3[\mathrm{n}_\infty(\mathrm{v})-\mathrm{n}]}{4\tau_n(v)}$	$\mathrm{n}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+50}{14}})$ $\tau_n(\mathrm{v})=0.05+0.27/[1+e^{\frac{v+40}{12}}]$
$I_T=0.5\alpha_\infty^3(v)rv$	$\mathrm{r}'=\frac{\mathrm{r}_\infty(\mathrm{v})-\mathrm{r}}{150}$	$\alpha_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+57}{2}})$ $\mathrm{r}_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+70}{2}})$
$I_{Ca}=0.15s_\infty^3(v)*(v-120)$		$s_\infty(\mathrm{v})=1/(1+\mathrm{e}^{\frac{v+35}{2}})$
$I_{AHP}=10(v+80)$ $*\mathrm{CA}/(CA+10)$	$\mathrm{CA}'=10^{-4}(-I_{Ca}$ $-I_T-15CA)$	

of patient physiological data to achieve individual variability at the model level is lacking. In terms of control laws only two algorithms, op-C and PI-C, were validated. At the hardware level, the platforms implemented so far are not very large. Hardware facilities with higher integration should be designed and manufactured to achieve better flexibility and scalability under the current architectural design architecture. In addition, the current tree topology is rather homogeneous.

TABLE VII
PARAMETERS FOR SYNAPSES CURRENT

Synapses	$g_{\alpha\to\beta}$ (μS/cm^2)	$E_{\alpha\to\beta}$ (mV)
$I_{STN\to GPe}$	0.15	0
$I_{STN\to GPi}$	0.15	0
$I_{GPe\to STN}$	0.5	-85
$I_{GPe\to GPe}$	0.5	-85
$I_{GPe\to GPi}$	0.5	-85
$I_{GPi\to TH}$	0.17	-85

TABLE VIII
APPLIED CURRENTS IN HEALTHY AND PD CONDITIONS

Conditions	I_{app} for STN	I_{app} for GPe	I_{app} for GPi
Healthy	33	20	21
PD	23	7	15

The unit of potential, conductance and current are mV, μA/cm^2 and μS/cm^2, and time constants have unit of msec.

In future work, we will improve the integration of the circuit structure in the hardware design, and establish a modular architecture makes it easier to scale up. The computational power and adaptability of the platform could be enhanced at the same or lower power consumption level. Besides, the working capability of the platform can be further extended by adding other peripheral resources to make it compatible with more types of models to get more application scenarios. More diverse topologies could be attempted in the routing structure to solve the possible conflict between network size and information delivery. More importantly, other pathological features can be implemented by the platform. The model can be optimized. For example, local axon collaterals inside the STN and the hyperdirect pathway (cortex to STN) are discussed in some works [44]–[46]. Richer model details can improve the accuracy of the description. More accurate and high-performance control algorithms should be designed and implemented to the online optimization of cl-DBS to advance its clinical application. The patient's physiological data can be used to enable the platform to implement cl-DBS hardware-in-loop simulation with individual variability.

APPENDIX A
DETAILS OF THE BG NETWORK MODEL

See Tables IV–VIII.

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