APPLICATIONS OF VEDIC MULTIPLIER DESIGNS - A REVIEW

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***Abstract*— Rapidly growing technology has raised demands for fast and efficient real time digital signal processing applications. Multiplication is one of the primary arithmetic operations every application demands. A large number of multiplier designs have been developed to enhance their speed. Active research over decades has lead to the emergence of Vedic Multipliers as one of the fastest and low power multiplier over traditional array and booth multipliers. Vedic Multiplier deals with a total of sixteen sutras or algorithms for predominantly logical operations. A large number of them have been proposed using Urdhava Tiryakbhyam sutra rendering them most efficient in terms of speed. The objective of this paper is to encapsulate an array of applications of Vedic Multiplier in the vast domain of Image processing and Digital signal processing, particularly the different modifications of existing Vedic Multiplier architectures enhancing their speed and performance parameters.**

Keywords-Vedic Multiplier, Image Processing, Digital Signal processing, Urdhava Tiryakbhyam sutra.

I. INTRODUCTION

The term 'Veda' means storehouse of knowledge. Vedic Mathematics is an ancient form of mathematics reconstructed from ancient Indian scriptures referred to as Vedas. It is based on 16 sutras which transact different branches of mathematics like algebra, geometry, arithmetic. [1] Urdhva Tiryagbhyam is the most generalised sutra for implementation of Vedic Multiplier designs because with increase in number of bits both area and delay increase slowly [2]. The beauty of Vedic Multiplier lies in the fact that they can be used to solve cumbersome mathematical operations orally thereby improving speed [3]. Fig.1 shows multiplication of 23 and 52 using Urdhva Tiryagbhyam.

[4] Multipliers being the key components of Arithmetic and logic units, Digital signal processing blocks and Multiplier and accumulate units, determine the performance and throughput of the applications. Vedic Multiplier has become highly popular as a faster method for computation and analysis.

[5] They have found immense use in applications of image processing to save time and area. Image processing is the application of certain operations on images such as image sharpening, pattern recognition, edge detection etc, to extract some useful information from them or to enhance a particular feature in it. Hence it is essential in fields of mapping, holography, x-ray imaging, medical image processing and robotics.

Similarly Digital Signal Processing is another area where high speed and low area Vedic Multipliers, are replacing commonly used conventional multipliers. Their importance couldn't have been more significant in the Semiconductor market demanding Digital Signal Processors for areas of wireless communication, audio and video processing, industrial control and portable electronics. The applications are as follows:

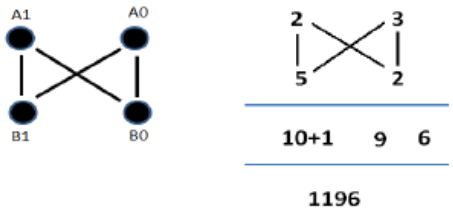

Fig.1 Two digit Multiplication using UT sutra

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II. APPLICATIONS OF HIGH SPEED VEDIC MULTIPLIER

A. A High Speed and Low Area Vedic Multiplier for Efficient Implementation of Faster Real Time Hardware Image Processing

Convolution being a fundamental concept is widely used in various image processing techniques, particularly spatial filtering techniques like smoothing, image sharpening etc. The idea behind [5] is to make these operations on images faster so as to enable more complex processing in real time, through the proposed Vedic Multiplier.

When 2-dimensional convolution is carried out on images, represented using 8 bit binary representation, the image intensity values are multiplied by the convolution kernel coefficients. Fig.2 shows how image is stored in Block RAM as a column vector, accessed and convoluted using 3*3 kernel coefficients. Position by position, convolution of each pixel is carried out in a Multiplier and Accumulate (MAC) unit, where multiplication was performed using Vedic Multiplier, till the end of image is reached. The processed image is finally displayed on a Video Graphics Array (VGA) screen.

While Vedic Multipliers developed so far are prone to inaccuracy at higher bit levels. The proposed Vedic Multiplier is highly accurate at both lower bit and higher bit level multiplications due to simple and regular design layout. Fig.3 shows implementation of a 4 bit Vedic Multiplier implemented using 2 bit multiplier and 4 bit adders. An 8 bit Vedic Multiplier can be built using four 4 bit multipliers and three four bit adders, enabling multiplication of larger bits using smaller bit multipliers.

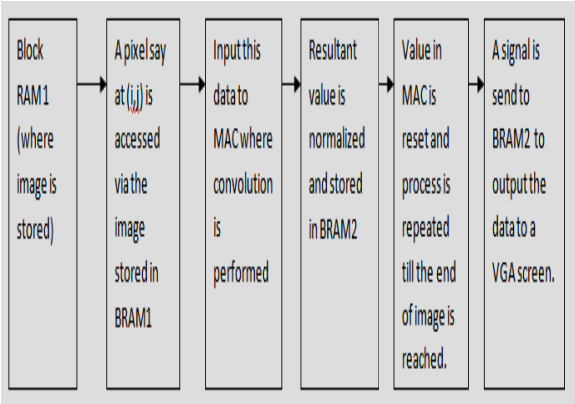

Fig.2 Image Processing Using Vedic Multiplier

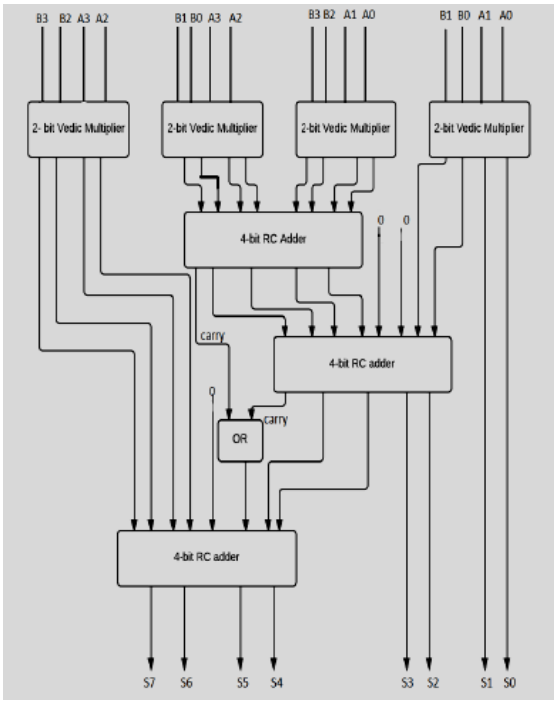

Fig.3 Hardware Architecture of 4 bit Vedic Multiplier

Table1 shows that the combinational delay of proposed 8 bit Vedic Multiplier is 12.429 ns and the total number of slices used in building it is merely 25. A comparison between proposed Vedic Multiplier architecture and the other existing implementations based on delay and total hardware utilization of FPGA clearly indicates that the Vedic Multiplier developed is faster and uses less area than others.

TABLE 1.COMPARISON RESULTS OF EXISTING AND PROPOSED VEDIC MULTIPLIER

TYPE	D:LAY(ns)	TOTAL NO. OF SLICES USED
1. Proposed Vedic Multiplier	12.429	25
2.Traditional Array Multiplier	25.527	133
3.Traditional Booth Multiplier	59.252	451
4.Overlay Array Multiplier	20.269	186
5.Overlay Booth Multiplier	37.583	580

B. Implementation of Vedic Multiplier in Image Compression, using Discrete Cosine Transform (DCT) Algorithm

[6] has proposed another application of Vedic Multiplier in Image Compression by improving

computational speed of matrix multiplication in Discrete Cosine Transform(DCT). The objective of Image Compression is to efficiently store or transmit an image by reducing the redundancy of image data.

Joint Photography Experts Group (JPEG) process is a widely used international standard lossy image compression algorithm, centred around DCT. Fig.4 shows the block diagram of proposed Image compression system where the image is first decomposed into 8x8 blocks of pixels, followed by which DCT algorithm is applied from left to right and top to bottom. Each block being compressed through quantization, enable the storage of an image in reduced amount of space.

The image can be reconstructed through the array of compressed blocks using Inverse Discrete Cosine Transform (IDCT) algorithm.

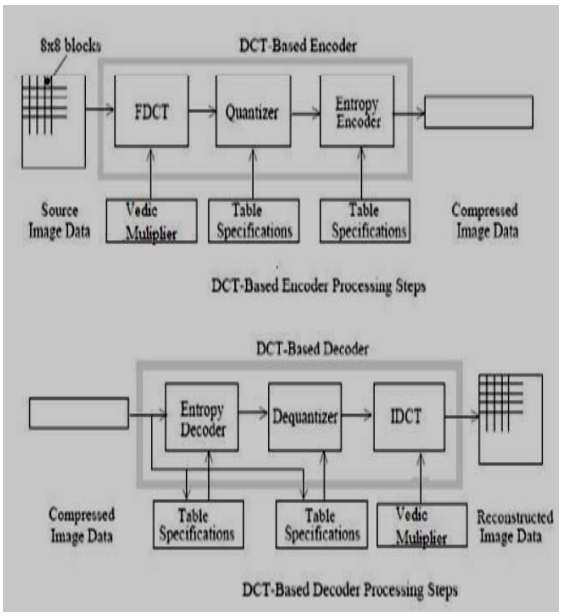

Fig.4 Block diagram of proposed Image compression system

Vedic Multiplier based on Urdhava Tiryakbhyam sutra is used for matrix computation of DCT. Fig.5 shows the hardware architecture of Vedic Multiplier. Thus by applying Vedic Multiplier in Image processing in DCT, computational time has reduced significantly in comparison to other conventional multipliers.

Fig.6(a) shows the input image to be transmitted, Fig.6(b) shows the compressed output image after applying DCT to the input image and Fig.6(c) is the output image obtained after decompressing using IDCT.

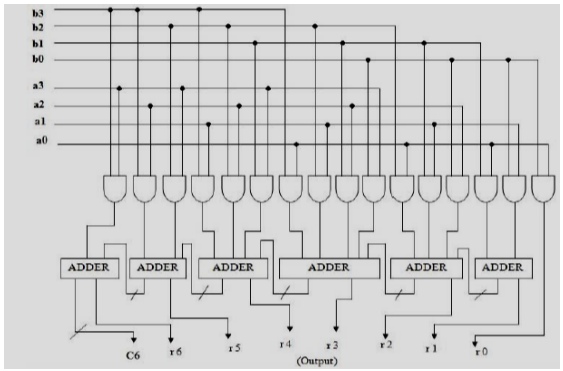

Fig. 5 shows the hardware architecture of Vedic Multiplier

Figure 6(a): Input Image

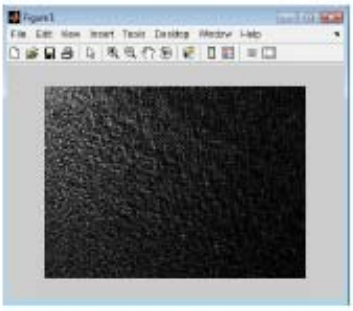

Figure 6(b) : Image after applying DCT to input image.

Figure 6(c) : Image after applying IDCT to compressed image

C. Application of Modified Vedic Multiplier in Multi-level 2-D Discrete Wavelet Transform (DWT) for Image Processing

Discrete Wavelet Transform is any wavelet transform in which wavelets are discretely sampled. It holds key advantage over traditional

transforms like Fast Fourier Transform (FFT) and Discrete Cosine Transform by the fact that it contains both frequency and time information due to which the quality of images reconstructed after same compression is much improved. In 2 dimensional DWT, FIR filter is used to increase the image resolution and remove unwanted noise present in the image by decomposing the input into different sub bands of low frequency and high frequency components. A high compression ratio is achieved followed by which inverse DWT is used to retrieve the original signal. This is referred to as Lifting based DWT computation, widely used for Image decomposition.

The modified Vedic Multiplier uses 8 half adders and 1 full adder as compared to 32 half adders in regular Vedic Multiplier, thereby offering reduction in area and power by 20% and 10% respectively. Thus in [7] a modified Vedic Multiplier emerged as an efficient architecture to implement multi level 2D DWT to increase image resolution than the conventional 3 level 2D DWT. Fig.7 shows the block diagram of Modified Vedic Multiplier for FIR filter of 2D DWT.

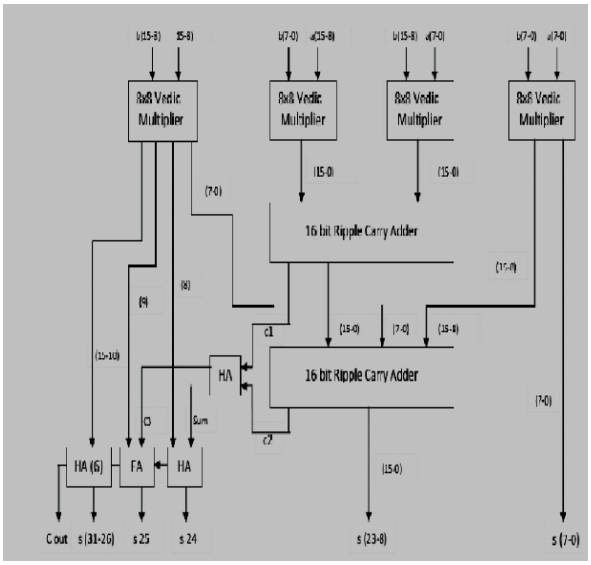

Fig.7 Block Diagram of Modified Vedic Multiplier for FIR filter of 2D DWT

D. Design of Novel Vedic Asynchronous Digital Signal Processor Core Using Vedic Multiplier And Divider:

[8] has implemented another application of Vedic Multiplier and Divider in the design of low power asynchronous Vedic DSP processor core. Fig.8 shows the architecture of Vedic DSP which is broadly divided into 2 sections: The Vedic core and asynchronous communication between modules.

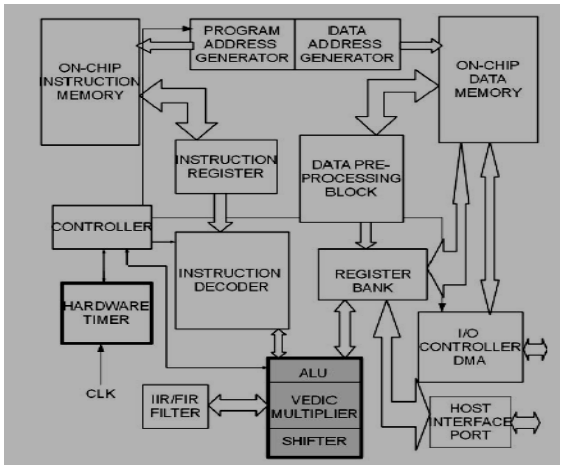

Fig.8 Vedic DSP Architecture

ALU along with Vedic Multiplier and Divider, forms the Vedic core, which makes the architecture efficient in terms of speed and area in comparison to conventional counterparts. Asynchronous design eliminates clocking issues and power consumption. Mousetrap pipelining [8] has been used to increase parallelism and hence the throughput of the system. Digital Signal Processor is rendered efficient because of usage of sutras , namely- Urdhva - tiryagbhyam, Nikhilam Navatashcaramam Dastaha, Ekadhikena and Ekanyunena Purvena, Anurupyena, Antyayor Dasakepi for Vedic Multiplier and Nikhilam, Paravartya Yojayet, Urdhva Tiryakbhyam and Dhvijanka for Vedic Divider. The proposed Vedic Multiplier is found to be 4 times faster than a conventional array multiplier. Synthesis reports show decrease in latency and a power advantage of 40%.

E. Application of High Speed Vedic Multiplier Using CSLA in Parallel FIR Architecture:

[9] shows implementation of high speed Vedic Multiplier in parallel FIR filter. The proposed Vedic Multiplier designed using high speed Carry Select Adder lead to reduced delay. Fig.9 shows the architecture of proposed 16x16 Vedic Multiplier structured further using four 8x8 Vedic Multiplier and two Carry select adders. Urdhva Tiryagbhyam algorithm has been implemented right from 2x2 Vedic Multiplier up to 16x16 bit Vedic module. Carry Select adders increases the speed of addition of partial products. The parallel FIR architecture using proposed 16 bit Vedic Multiplier has a gate

delay of 58.924 ns and device utilization of 3517 out of 3584. While existing Vedic Multiplier has a gate delay of 73.682 ns and device utilization of 3582 out of 3584. Thus Vedic Multiplier designed using CSLA has improved the speed of FIR filters and area utilization over traditional Vedic Multipliers.

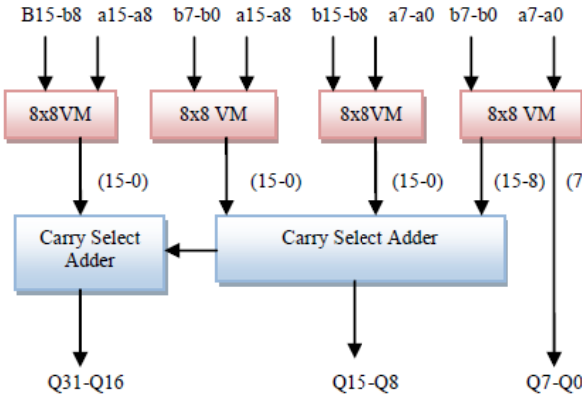

Fig.9 Proposed Architecture of 16x 16 bit Vedic Multiplier

F.Application of Vedic Mathematics in the design of High Speed ASIC Design of Complex Multiplier:

[10] has proved another application of Vedic Mathematics in the design of a novel complex Multiplier, which is of immense importance for high speed complex arithmetic circuits with wide applications in fields of image and signal processing. Till now the above approaches have mainly used Urdhva Tiryagbhyam algorithm for design of Vedic Multiplier which is efficient for smaller length multiplication. But this approach has concentrated on Nikhilam sutra, which is extremely efficient for multiplication of two larger numbers, involving a large amount of carry propagation delays. The partial products and sums are generated in one step, reducing the delay of carry propagation from LSB to MSB.

The implementation is done in Spice spectre and application of Vedic Mathematics has ensured 25% improvement in speed in comparison to commonly used complex multipliers based on parallel adder and distributed arithmetic based architectures. The propagation delay of 16 bit complex multiplier is only 4ns and consumes 6.5mW power ensuring substantial reduction in propagation delay and dynamic power consumption. Fig.10 shows the hardware implementation of 'Nikhilam Sutra' divided into 3 parts namely: 1) Radix Selection Unit (RSU), 2) Exponent Determinant(ED), 3) Array Multiplier. RSU is used to select proper radices corresponding to the input numbers, exponent determinant is used to extract the power of the radix and array multiplier is used to calculate the product.

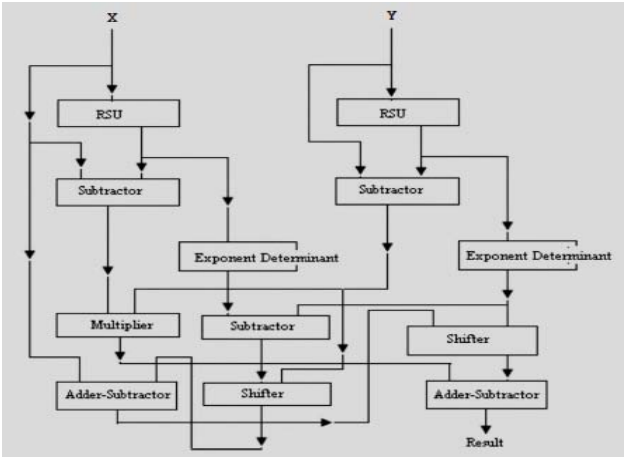

Fig.10 Hardware implementation of 'Nikhilam Sutra'

III. CONCLUSION

Thus presented the applications of different designs of Vedic Multiplier in numerous operations that can be used for storage, transmission or processing of large amount of data in the form of signal or an image required daily in a digital world. The enhancement of each application in the form of improved results has reinforced the efficiency of Vedic Multiplier in terms of speed, area utilization and power with respect to other multipliers.

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