# Investigations on High-Power LEDs and Solder Interconnects in Automotive Application: Part I—Initial Characterization

Maximilian Schmid, Andreas Zippelius, Alexander Hanß, Stephan Böckhorst, and Gordon Elger

***Abstract*—Thermo-mechanical reliability is one major issue in solid-state lighting. Mismatches in the coefficients of thermal expansion (CTE) between high-power LED packages and substrates paired with temperature changes induce mechanical stress. This leads to a thermal degradation of LED modules by crack formation in the solder interconnect and/or delamination in the substrate, which in turn increases junction temperature and thus decreases light output and reduces lifetime. To investigate degradation and understand influence of LED package design and solder material, a reliability study with a total of 1800 samples – segmented in nine LED types and five solder pastes – is performed. First of all, in this paper a state-of-the-art review of high-power LED packages is performed by analyzing and categorizing the packaging technologies. Second, the quality inspection after assembly is realized by transient thermal analysis (TTA), scanning acoustic microscopy (SAM) and X-ray. For TTA, a new method is introduced to separate the thermal resistance of the LED package from solder interconnect and substrate by applying the transient dual interface method (TDI) on samples with different solder interconnect void ratios. Further measurement effort is not required. The datasheet values for thermal resistance are verified and the different LED package types are benchmarked. The void ratio of the solder interconnects is determined by X-ray inspection combined with an algorithm to suppress disruptive internal LED package structures. TTA and TDI revealed that initial thermal performance is independent of solder paste type and that voiding is more critical to smaller LED packages. In addition, lower silver proportion in the paste is found to increase voiding. SAM is less sensitive for initial void detection than X-ray, but it's applied to monitor crack propagation while aging in combination with TTA. The results of the reliability study, i.e., the crack growth under temperature shock test for the different SAC solders, will be presented in a second independent paper.**

***Index Terms*—LED, non-destructive testing, reliability, solder, scanning acoustic microscopy (SAM), thermal impedance (Zth), thermal resistant (Rth), transient thermal analysis (TTA), X-ray.**

Manuscript received December 22, 2021; accepted February 11, 2022. Date of publication February 18, 2022; date of current version June 7, 2022. This work was supported by the German Federal Ministry of Education and Reseach through the Project IQLED under Grant 13FH044PX8. *(Corresponding author: Maximilian Schmid.)*

Maximilian Schmid, Andreas Zippelius, and Gordon Elger are with the Institute of Innovative Mobility, Technische Hochschule Ingolstadt, 85049 Ingolstadt, Germany (e-mail: maximilian.schmid@thi.de; andreas.zippelius@thi.de; gordon.elger@thi.de).

Alexander Hanß was with the Institute of Innovative Mobility, Technische Hochschule Ingolstadt, 85049 Ingolstadt, Germany (e-mail: alexander.hanss@gmx.de).

Stephan Böckhorst is with L-LI-TCE, HELLA GmbH & Co. KGaA, 59552 Lippstadt, Germany (e-mail: stephan.boeckhorst@hella.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TDMR.2022.3152590.

Digital Object Identifier 10.1109/TDMR.2022.3152590

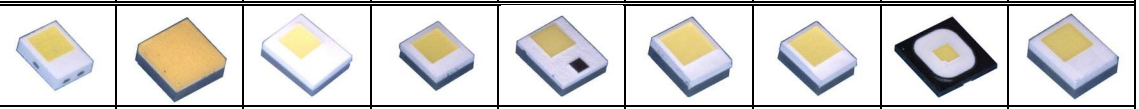
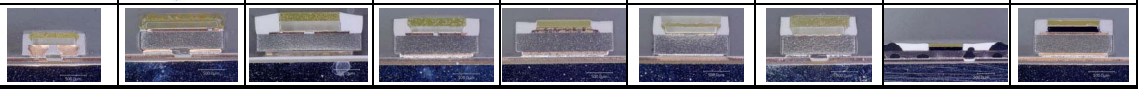
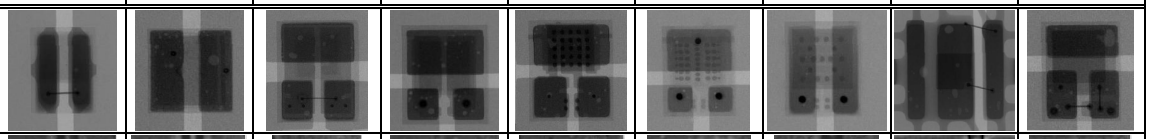
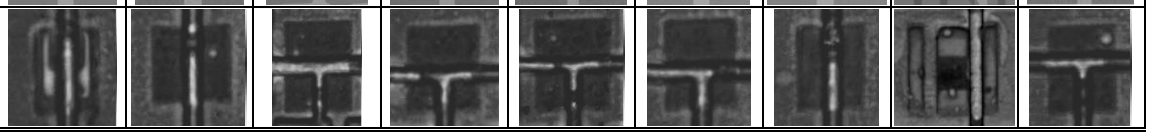
## I. Introduction

THE REPLACEMENT of conventional light sources, e.g., filament and discharge lamps, by LEDs in nearly all fields of lighting is driven by optical, mechanical and electrical advantages of LEDs [1] and restrictions like EU regulation on household lamps [2]. Based on their increased efficiency and nonhazardous materials, LEDs are eco-friendlier than their predecessor. Further, small form factors and distributed arrangements allow innovative optical designs [3].

LEDs can be manufactured in many different output colors. Most common in today's solid-state lighting industry are white LEDs based on a blue light emitting GaN die with phosphor light conversion. White light generation by RGB light mixing and non-white LEDs, e.g., red LEDs for automotive backlights or ultra violet LEDs for adhesive curing, are relevant as well [4]. However, the most critical parameter for all LED applications is the junction temperature $T_J$. An increase in $T_J$ results in a decrease in light output, i.e., reduction of efficiency, a shift in color and a reduction of lifetime [5]. To limit $T_J$ during operation to a non-critical range, the generated heat loss must be reliably conducted from the junction through the package and board to the heat sink (thermo-mechanical setup). The thermal and mechanical properties determine the initial performance of the design and the degradation according to environmental conditions [6].

Initial performance and degradation both depend strongly on the chosen components and materials for LED, solder interconnect and substrate. Finding the best combination is not trivial and valuable data is mostly not publicly accessible. To reveal influences, we performed a full factorial reliability study with nine LED types and five lead-free solder pastes, resulting in a total sample count of 1800 high-power LEDs, and evaluated initial performance and degradation under thermal shock cycling by different non-destructive test methods. X-ray is used to determine void ratio in the solder interconnect, scanning acoustic microscopy (SAM) is used to inspect crack growth in the solder interconnect and delamination in the substrate and transient thermal analysis (TTA) is used to evaluate initial and degraded thermal performance. The results are presented in two papers, where this first one covers the initial quality inspection, properties of the LEDs, solder pastes and substrate, and test methods for quality insurance. The second part will analyze the degradation over aging.

TABLE I
SUMMARY OF RELEVANT OPTICAL, MECHANICAL, ELECTRICAL AND THERMAL PARAMETERS OF THE LEDS WITH IMAGES, CROSS-SECTIONS, X-RAY IMAGES, SAM IMAGES. THE LEDS ARE NAMED ACCORDING TO THEIR INTERNAL DIE STRUCTURE

| **Name in this paper** | **FC-SP1** | **FC-SP2** | **FC-SP3** | **FC-SP4** | **FC-GB1** | **FC-GB2** | **FC-GB3** | **VTF1** | **VTF2** |
|---|---|---|---|---|---|---|---|---|---|
| Classification | Automotive | General | Automotive | Automotive | Automotive | Automotive | Automotive | Automotive | Automotive |
| Image |  | | | | | | | | |
| Cross-Section |  | | | | | | | | |
| Submount | Lead frame | Ceramic | Ceramic | Ceramic | Ceramic | Ceramic | Ceramic | Lead frame | Ceramic |
| Sapphire removed | No | No | No | No | Yes | No | No | Yes | Yes |
| Pad count | 2 | 2 | 3 | 3 | 3 | 3 | 2 | 3 | 3 |
| Die size [1] [$mm^2$] | 0.6 | 1.9 | 1.3 | 1.0 | 1.0 | 0.9 | 1.0 | 1.0 | 1.0 |
| Size [$mm^2$] | 1.92 | 2.56 | 5.0 | 3.03 | 4.37 | 2.61 | 2.61 | 14.06 | 2.85 |
| Pad-Size [$mm^2$] | 0.81 | 1.80 | 2.79 | 1.86 | 2.75 | 1.45 | 1.49 | 5.40 | 1.74 |
| $\lambda_{dom.}$ [nm] | 440 | 440 | 450 | 445 | 440 | 440 | 445 | 440 | 440 |
| Lumen [2] [lm] | 148 | 285 | 347.5 | 362.5 | 230 [3] | 362.5 | 325 | 330 | 377.5 |
| $I_{Nom}$ [A] | 0.35 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| $I_{Max}$ [A] | 0.7 | 2.0 | 1.5 | 1.5 | 1.5 | 1.2 | 1.2 | 1.5 | 1.5 |
| $V_f$ [2] [V] | 2.75 ... 3.00 | 2.9 [3] | 2.90 ... 3.50 | 2.8 ... 3.4 | 2.79 ... 3.03 [3] | 2.9 ... 3.5 | 2.9 ... 3.9 | 3.00 ... 3.25 | 3.00 ... 3.25 |
| $R_{th\text{-}JC\text{-}el.}$ [4] [K/W] | 4.75 | 6.0* | 3.0 | 3.5 | 4.2 | 3.3 | 3.0 | 3.0 | 3.3 |
| X-ray (not scaled) |  | | | | | | | | |
| SAM (not scaled) |  | | | | | | | | |

[1] Measured after mechanical phosphor removal

[2] Mean value of specified binning range at $I_{Nom}$ and 25 °C

[3] Defined at $I_{Nom}$ but at 85 °C instead of 25 °C

[4] $R_{th}$ from junction to case of the LED related to the electrical power. If the datasheet included no typical value, the mean value of the specified range is used

* Value from the datasheet doesn't correspond to measurement results with approx. 2 K/W and also to the LED design with a ceramic material (AlN) like the others. It is assumed that the value is in the datasheet is erroneous. However, the supplier didn't respond after contact and reporting the error.

## II. LEDs, SOLDER PASTES AND SUBSTRATE

For this reliability study, nine different LEDs and five different lead-free solders are investigated using a full factorial design of experiments. Aluminum insulated metal substrate printed circuit boards (Al-IMS-PCB) were designed for 10 LEDs per type. For every solder type four substrates were assembled with LEDs. Altogether the study contains 1800 LEDs on 20 substrates. LED types, solder pastes and substrate are described in following subsections.

### A. LEDs

All nine LED types from seven different manufactures are packaged white high-power LEDs in surface mounted technology (SMT). Light is generated by a GaN semiconductor die emitting blue light with a phosphor converter on top for light conversion. All LED types are named according to their internal die structure discussed later. Images, cross-sections together with relevant optical, electrical, thermal and mechanical parameters are summarized in Table I. Several characteristics are quite similar for all LEDs, like the dominant blue wavelength $\lambda_{dom}$ between 440 – 450 nm and the forward voltage $V_f$ of approx. 3 V at nominal current $I_{Nom}$. Others strongly differ like the mechanical dimensions, package type and the thermal properties.

Most relevant for thermal performance and reliability is the thermo-mechanical setup of the LED package and the internal die structure. For mechanical stability and heat spreading, the LED dies are attached to an AlN ceramic submount or copper-based lead frame with soldering pads at the bottom in all designs. The internal die structure can be classified into three groups for the inspected LED packages, schematically described in Fig. 1. All die structures follow modern design aspects for high power LEDs and are quite similar except for differences in internal current routing and lead out contacts for anode and cathode. The basic principle is an n-side-up

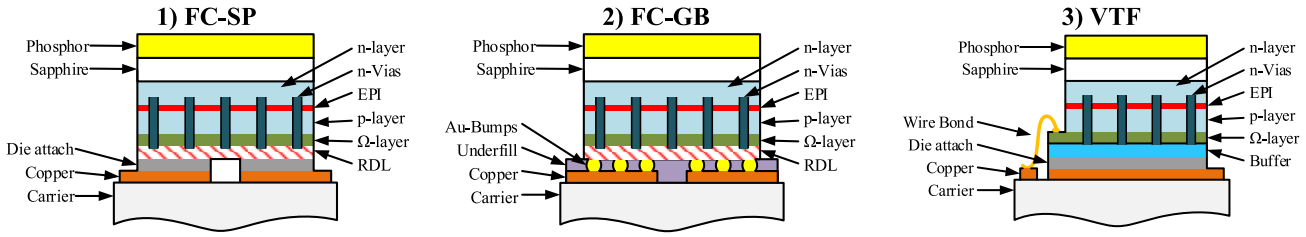



Fig. 1. Schematically description of the internal die structure with: 1) FC-SP: Flip Chip with solder pads used for FC-SP1 - FC-SP4, 2) FC-GB: Flip Chip with gold bumps used for FC-GB1 - FC-GB3 and 3) VTF: Vertical thin film used for VTF1 and VTF2. If the sapphire is removed by LLO, the phosphor is directly attached to the n-layer. Black lines represent electrical isolation between materials.

GaN die with vertical current flow. The electrical connection to the n-layer is realized by n-Vias through the light generating epitaxial layer (EPI) and p-layer. The relative thermally low conductive sapphire substrate, on which the GaN is grown, is for all die structures in the optical path above the n-layer. Therefore, the sapphire is not in the heat conduction path and doesn't influence the temperature of the EPI significantly, which is advantageous for thermal management [1]. In addition, for some LEDs the sapphire is removed by a laser lift off (LLO) process. The phosphor is therefore either attached to the sapphire or to the die in form of a ceramic based platelet or as silicon-based layer. The removal of the sapphire improves optical performance and reduces the phosphor temperature due to direct thermal connection to the die [7]. The roughly 100$\mu$m thick sapphire and the phosphor containing ceramic platelet act as additional stiffener for the die and can be beneficially for thermo-mechanical reliability. For all automotive LEDs a $TiO_2$ side coating is used to suppress sideway light emission out of the sapphire and the phosphor. The differences of the internal structures are now briefly described:

*1) Flip Chip With Solder PADS (FC-SP):* The anode and cathode contacts in form of two planar pads are at the bottom of the LED die, attached by soldering (often eutectic Gold/Tin) to the submount. Over a redistribution layer (RDL) anode is electrically routed to the p-layer over the Ω-Layer and cathode routed to the n-layer over the n-Vias. The light generating EPI is in-between n-layer and p-layer [8].

*2) Flip Chip With Gold Bumps (FC-GB):* This structure is nearly identical to FC-SP. The only difference is, that the backside connections for anode and cathode are realized by gold bumps to the submount instead of two solder interconnects. To improve mechanical stability, an underfill is applied between die and submount [9].

*3) Vertical Thin Film (VTF):* In this structure, anode connection is realized from the top of the Ω-Layer contact region by a wire bond to the submount. Therefore, this design is by definition not a flip chip. The planar die attach over the complete die surface is only used for the cathode connection and is connected to an electrically conductive buffer layer with access to the n-Vias. On top of the buffer is the Ω-Layer with an electrical isolation in-between. No RDL is required in this structure. Above the Ω-Layer the VTF is identical to FC-SP and FC-GB [10].

All LEDs are classified with $I_{Nom} = 1$ A, except for the FC-SP1 with only $I_{Nom} = 350$ mA. This is due to the smaller die size of the FC-SP1 with 0.6 mm$^2$ compared to the others with approx. 1 mm$^2$. Only the FC-SP2 and FC-SP3 have larger dies with 1.9 mm$^2$ resp. 1.3 mm$^2$. A copper lead-frame submount is used for VTF1 and FC-SP1 while all others use an AlN ceramic submount with top and bottom metallization and vias to connect both sides. For SMD soldering, the FC-SP1, FC-SP2 and FC-GB3 use a symmetrical two-pad design, with one pad for anode and one for cathode. The VTF1 has a three-pad design where two pads are electrical connected through the copper submount. All other LEDs use a three-pad design with one electrical isolated pad below the die (thermal pad) for improved heat management. The sapphire was removed by LLO for FC-GB1, VTF1 and VTF2.

TABLE II
COMPOSITION IN WEIGHT PERCENTAGE FOR THE DIFFERENT PASTES, SORTED BY AG PARTS. REMAINING PART IS SN

| Paste | Additives material | | | | | |
|---|---|---|---|---|---|---|
| | Ag | Cu | Sb | Bi | Ni | In |
| SAC105 | 1.0 | 0.5 | - | - | - | - |
| SAC+BiIn | 1.0 | 0.7 | - | 1.6 | - | 0.2 |
| SAC305 | 3.0 | 0.5 | - | - | - | - |
| SAC+Sb | 3.2 | 0.7 | 5.5 | - | - | - |
| SAC+SbBiNi | 3.8 | 0.7 | 1.5 | 3.0 | 0.15 | - |

### B. Solder Pastes

Five commercial Sn based lead-free solder pastes were selected for this study, with their composition listed in Table II. Two of them are pure SAC (Sn, Ag, Cu) alloys with different portions of silver. The others are SAC+ pastes with additives of Sb, Bi, Ni or In, developed for improved thermal performance and reliability [11].

All pastes were of type 4 (solder sphere diameter: 20 $\mu$m to 38 $\mu$m) and applied by a screen-printing process using a 75$\mu$m stencil. LEDs were placed with a semi-automatic pick-and-place machine. A batch oven was used to apply the same standardized reflow soldering profile [12] for all pastes with nitrogen protective atmosphere and vacuum by a membrane pump during liquidus time depicted in Fig. 2.

### C. Substrate

The LEDs were soldered on an insulated metal substrate printed circuit board (IMS-PCB) with 70 $\mu$m copper, a 50 $\mu$m

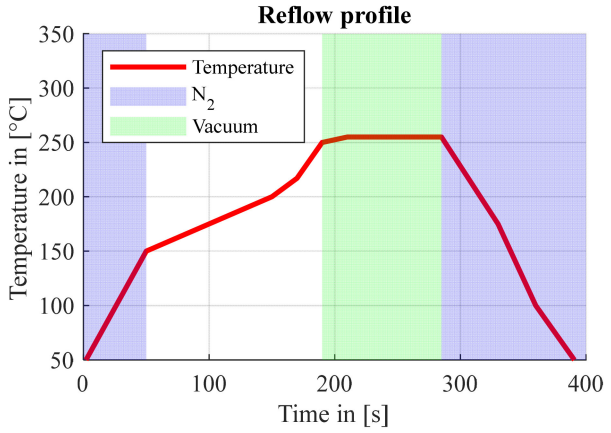



Fig. 2. Reflow profile with vacuum and nitrogen protective atmosphere.

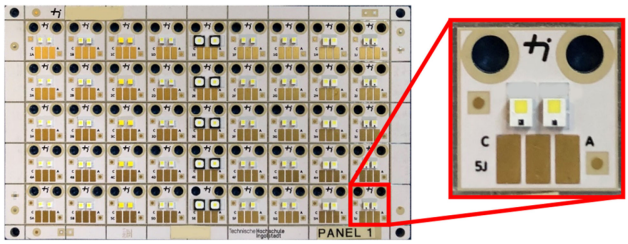



Fig. 3. (a) PCB with 90 LEDs soldered with one paste and (b) sub-PCB with two LEDs of one type.

thick dielectric with a thermal conductivity of 4.2 W/mK and a 1.6 mm aluminum core. Each IMS-PCB is assembled with 90 LEDs and can be separated into 45 sub-PCBs (each holding two LEDs of the same type), arranged in nine columns for the nine LED types and five rows. An image of an assembled IMS-PCB is shown in Fig. 3(a) with a closer look to one sub-PCB holding two LEDs in Fig. 3(b). Four IMS-PCBs were assembled per solder paste.

## III. Inspection Methods

### A. X-Ray

X-ray is the most popular inspection method nowadays in development and production of electronics. Continuous development of X-ray equipment has enabled fast inspection even at production speed, 3D inspections and resolutions down to $\mu$m range [13]. For X-ray inspection, the specimen is penetrated by a high energy electro-magnetic beam where the radiation is partly absorbed by the material depending on density and atomic number. The penetrating radiation is recorded on the backside of the specimen by an X-ray detector and summarized as a 2D image [14].

For electronics, X-ray is mostly used to detect voids (gas inclusions in the solder joint) and non-wetted solder areas (unsoldered regions due to residues or contamination on component or substrate). Both appear brighter in the X-ray image since more radiation can pass through the specimen due to missing metallic material. X-ray is not suited for crack detection in the solder joint, except if the crack propagation is parallel to the radiation, because cracks are minimal material separation without a volume change [15].

For this study, all LEDs were initial inspected with the same settings on standard 2D X-ray equipment and X-ray images from one sample LED of each type are included in Table I.

### B. Scanning Acoustic Microscopy

Focused acoustic waves in the range of 15 to 300 MHz are used for SAM inspections. The waves are emitted by a transducer towards the specimen, which is placed in water as couplant, requiring a subsequent drying process. While penetrating the specimen, parts of the acoustic wave are reflected back at any interface between two different materials according to their difference in acoustic impedance. These reflections are recorded time resolved by the transducer and the pattern and delay is analyzed. By raster scanning in x and y direction over the specimen, the information of single points is combined in a 2D image holding the surface and/or volume information of the specimen [16]–[18].

The resolution of the SAM images is worse compared to X-ray and depends on the used frequency. Higher frequencies increase the resolution but reduce the penetration depth and therefore also the analyzable depth [19]. However, besides voids and non-wetted areas, cracks are detectable with SAM. Small material separations represent interfaces from material to gas for the acoustic wave and cause a back reflection. Therefore, the SAM focus in especially of the detection of crack growth during the reliability investigation (second part of the study published separately) and has as initial inspection method a minor importance, i.e., in SMD reflow soldering typically solely X-Ray is used for the high-power LED packages.

For this study, all LEDs were initially inspected with a 50 MHz transducer from the backside to qualify the solder interconnect. An inspection from the topside was not possible, since the inhomogeneous internal material structure of the LED impeded an evaluation. Interferences by the woven fabric structure of the dielectric while measuring from the backside were only minimal for the used substrate and therefore this measurement direction was selected. Transducers with higher frequencies didn't reached the required penetration depth for solder joint inspection. SAM images of one sample LED per type (same samples as for X-ray images) are included in Table I, already mirrored vertically to compensate for the measurement from the backside for comparison to the X-ray.

### C. Transient Thermal Analysis

TTA is a widespread measurement method to qualify the thermal performance of semiconductors in a thermo-mechanical setup. The key parameter is the thermal impedance $Z_{th}(t)$, representing the time dependent temperature change $\Delta T(t)$ for a change in power loss $\Delta P$:

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P}. \tag{1}$$

The TTA measurement principle is applicable for all kinds of semiconductors and defined especially for LEDs in [20].

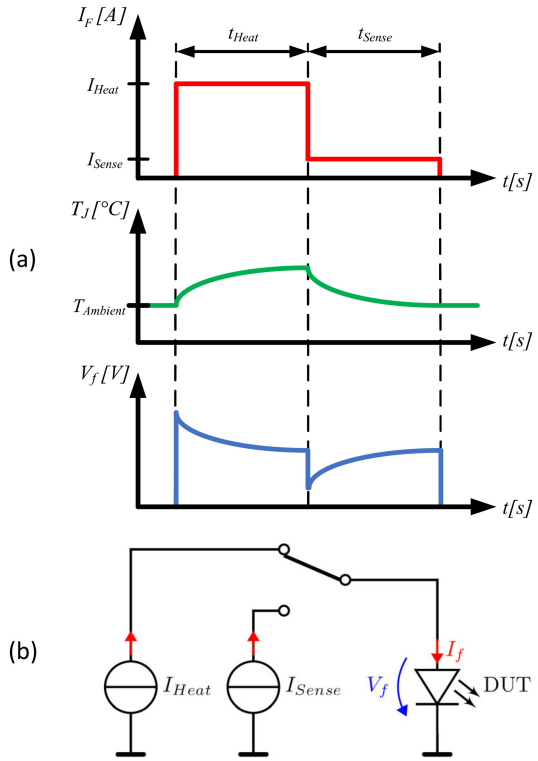



Fig. 4. (a) Measurement sequence of transient thermal analysis and (b) simplified schematic circuit diagram of measurement equipment.

The applied measurement sequence is depicted in Fig. 4(a) and the electrical measurement circuitry in Fig. 4(b). At first, the LED is driven by a constant heating current $I_{Heat}$ for the time $t_{Heat}$, resulting in an increase of the junction temperature $T_J$ of the LED through internal energy loss. $I_{Heat}$ should be chosen as high as possible without driving the LED in critical condition or with $I_{Nom}$ to achieve an adequate temperature increase. During $t_{Heat}$, thermal equilibrium should be reached to avoid incorrect results, which normally takes between 1 s to 10 s dependent on the thermo-mechanical setup. After $t_{Heat}$, the driving current is switched very fast from the heat current source to a second constant current source with a much lower constant sense current $I_{Sense}$ and the LED begins cooling down. During $t_{Sense}$, $T_J$ is continuously measured indirectly through the temperature sensitive forward voltage $V_f$ of the LED with a linear dependency *SEN* of approx. $-1$ to $-2$ mV/K at $I_{Sense}$:

$$\Delta T_J(t) = \frac{\Delta V_f(t)}{SEN} = k * \Delta V_f(t). \tag{2}$$

It should be mentioned that in some literature the $k$ factor is used instead of *SEN*, which is its reciprocal.

For LEDs, two different $Z_{th}(t)$ are defined in [20]. Both can be calculated with (1). First is the electrical thermal impedance $Z_{th\text{-}el.}(t)$, based on the change in electrical power between heating ($P_{Heat\text{-}el.} = I_{Heat} * V_{f\text{-}Heat}$) and sensing ($P_{Sense\text{-}el.} = I_{Sense} * V_{f\text{-}Sense}$):

$$Z_{th\text{-}el.}(t) = \frac{\Delta T(t)}{P_{Heat\text{-}el.} - P_{Sense\text{-}el.}}. \tag{3}$$

Second is the real thermal impedance $Z_{th\text{-}real}(t)$, based on the real change in thermal loss. For LEDs, part of the electrical power is converted into the optical power $P_{Opt}$ and don't have to be considered for the thermal behavior:

$$Z_{th\text{-}real}(t) = \frac{\Delta T(t)}{P_{Heat\text{-}el.} - P_{Sense\text{-}el.} - P_{Opt}}. \tag{4}$$

$Z_{th\text{-}real}(t)$ requires an additional complex measurement of $P_{Opt}$ with, e.g., an integrating sphere [21]. However, since lighting modules are in nearly all commercial application not regulated on their optical output but on their electrical input, $Z_{th\text{-}el.}(t)$ is the more relevant for reliability testing. In that case, an age induced efficiency degradation of the LED is also included in the evaluation. Therefore, in the following $Z_{th}(t)$ means $Z_{th\text{-}el.}(t)$.

Evaluation of TTA data can be done in many different ways. Easiest is the evaluation of the thermal resistance $R_{th}$, the termination value $Z_{th}(t = \infty)$, to rate the performance of the complete thermal path of the thermo-mechanical setup. But that way, a degradation is only detectable for the whole thermal path and not assignable to single layers inside the thermo-mechanical setup. To narrow the location of degradation to a single layer, the $Z_{th}(t)$ of the device under test (DUT) is compared to a reference $Z_{th}(t)$. As long as the $Z_{th}(t)$ curves are overlapping, the thermal paths are also identical. At the points of separation, the thermal paths start to differ due to a better thermal performance of one device compared to the other. The closer the layer is to the junction of the LED, the earlier the point of separation occurs in $Z_{th}(t)$ and vice versa [22]. In that way, different time intervals can be connected to different material layers and a $Z_{th}(t)$ increase at a certain time assigned to certain degradation types. For an exact definition of the separation time, [22] describes a method using the derivative $a(z)$ of $Z_{th}(t)$ with respect to $z = ln(t)$:

$$a(z) = dZ_{th}(z)/dz. \tag{5}$$

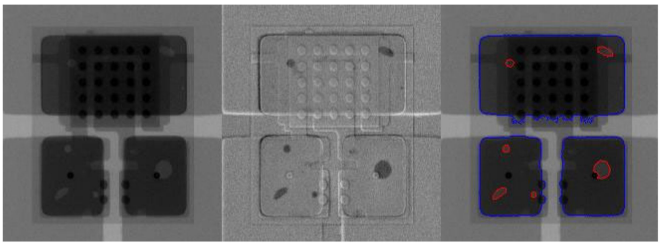
The separation time is defined as the point where the difference $\Delta a(z)$ between the two sample exceeds a predefined limit.

Besides the comparison of $Z_{th}(t)$, there are also more complex mathematical evaluation methods popular with TTA such as the normalized logarithmic derivative [23] and the structure function [24], but a deeper discussion of the field of TTA evaluation would go beyond the scope of the paper.

For the TTA measurements, an in-house developed automatic TTA measurement equipment [25] was used to allow the inspection of the high sample count. The IMS-PCBs are fixed to a temperature stable plate with a thermal interface material (TIM) in between and spring probes mounted on a XYZ-table are used to successively contact and measure all LEDs. Each LED was measured with a sample frequency of 10 MHz for $t_{Heat} = t_{Sense} = 3$ s (sufficient to reach thermal equilibrium) and 10 repetitions to reduce noise. $I_{Heat}$ was set to $I_{Nom}$ (see Table I) and $I_{Sense}$ to 20 mA for all LEDs. Before the TTA sequence, *SEN* is determined by measurement of $V_f$ at four temperature levels between 25 °C and 55 °C. With this setting, a measurement of one IMS-PCB with 90 LEDs took about 3 h with the automatic measurement equipment including automatic SEN measurement at four different temperatures. A manually measurement of all 20 substrates wouldn't be realizable.

TABLE III
AVERAGE AND STANDARD DEVIATION OF VOID RATIO BY LED TYPES (AVERAGE OVER ALL SOLDER PASTES)

| | | FC-SP1 | FC-SP2 | FC-SP3 | FC-SP4 | FC-GB1 | FC-GB2 | FC-GB3 | VTF1 | VTF2 |
|---|---|---|---|---|---|---|---|---|---|---|
| Void ratio | Ø | 0.53% | 2.45% | 2.37% | 3.16% | 2.35% | 1.34% | 5.33% | 2.86% | 3.47% |
| | σ | ±0.79% | ±1.71% | ±1.45% | ±2.25% | ±1.68% | ±1.13% | ±3.47% | ±2.30% | ±1.88% |



(a) (b) (c)

Fig. 5. Visualization of void detection algorithm for one sample LED of type FC-GB1 with a void ratio of 2.7%. (a): raw X-ray image of the DUT with disturbing internal structures; (b) average image subtracted from (a); (c) final image with marked LED outline (blue) and marked void outline (red) determined by thresholding of (b).

## IV. RESULTS

### A. Void Inspection

Only X-ray images were used for solder interconnect void inspection. SAM images contain information of lager voids too, but smaller ones are not detected due to limited resolution. For this reason, SAM images are not further investigated in this paper but used for evaluation of crack propagation while thermal shock cycling as discussed in the subsequent paper about this study.

The void ratio (Void area compared to solder interconnect area) was determined by an in-house developed image processing algorithm in MATLAB and is complex compared to even advanced algorithms [26]. The fine internal metallic structures with sharp edges of the LEDs (e.g., top metallization of the submount, wire bonds and gold stud bumps) prevent a simple threshold analysis. Instead, at first the outline of all LEDs of one type is detected and the average image generated by overlapping all of them to obtain a "void-less" X-ray image. The average image is then subtracted from the DUTs X-ray image to receive information of voids only, without or with minimized disturbing internal structures. In this image, it is possible to detected the voids by thresholding. A visualization of the algorithm can be seen in Fig. 5.

The results of the void ratio determination are summarized in Fig. 6 and listed in Table III. For all LED types except FC-GB3, an average over all pastes void ratio below 4% was achieved due to soldering under vacuum. For FC-GB3 only SAC+Sb had a voiding comparable to the other LEDs. All other showed an intense voiding, visible in Fig. 7 with five representative LEDs. Even so all LED types had a similar gold pad surface finish and were solder on the same IMS-PCB at the same time, a possible reason for the more intense voiding is a contamination of the solder pads of FC-GB3. Hereby the flux in the SAC+Sb paste was able to handle the contamination, but the other pastes not.

Overall, a relation between the Ag parts in the paste and void ratio is observed. SAC+SbBiNi with the most silver parts reached the lowest average void ratio with 1.5% over all LEDs. Followed by SAC+Sb with 2.2% void ratio, SAC305 and SAC+BiIn both with 2.9%. SAC105 with the fewest silver parts showed the highest void ratio with 3.9%.

### B. Temperature Sensitivity

The sensitivity *SEN* was determined individually for all LEDs. $V_f$ at $I_{Sense}$ was measured at four different temperatures (25 °C, 35 °C, 45 °C and 55 °C) and the dependency calculated by simple linear regression [27]. All LEDs showed a coefficient of determination $r^2$ of at least 0.9999, proofing a strong linear correlation. A Burn-In for 24 h at $I_{Nom}$ to reduce variance in *SEN* like described in [20] was not performed for reasons of complexity with the high sample count.

The measurement results for one representative LED of each type are plotted in Fig. 8(a) with measurement points as cross marks and the calculated linear regression as dashed line. The slope of linear regression represents *SEN*. Linear dependency is given for all LED types. However, *SEN* and $V_f(I_{Sense})$ vary between the LED types and also for LEDs of the same Type.

To evaluate average and variation in *SEN* and $V_f(I_{Sense})$ between and inside the LED types, the *SEN* values of all LEDs are plotted over their $V_f(I_{Sense})$ at 25 °C in Fig. 8(b) as a point cloud. Each point represents a single LED and the different LED types are sorted by color. Additionally, average and variance of *SEN* and $V_f(I_{Sense})$ are listed in Table IV. The four FC-SP LEDs showed the smallest *SEN* between −1.0 and −1.1 mV/K with a small variance of approx. 1%. The influence of the LED structure on *SEN* will be discussed later in this section. The small *SEN* of the four SP LEDs imply smaller temperature induced $V_f$ drift in application and accordingly require smaller operation ranges for the power supply, but for TTA they are adverse since they reduce measurement signal and therefore signal quality. The small variance in *SEN* for these LEDs allows a reduction of measurement time by calculating $Z_{th}(t)$ based on an average *SEN* value and not on an individual measurement for each LED without excessively disturbing the results. However, in this study all *SEN* were measured individually and used for the later $Z_{th}(t)$ calculation. For FC-GB2 and FC-GB3, *SEN* is slightly higher with a higher variance around 4.5%, which already requires an individual determination to avoid errors. VTF1 and VTF2 showed even higher *SEN* with −1.45 mV/K resp. −1.63 mV/K, and the highest variances of the LED types with 10.6% resp. 12.2% mandating an individual *SEN* determination. For the FC-GB1 LEDs the highest SEN with −2.0 mV/K was observed with a variance of only 1.0% offering the best conditions for TTA measurement in principle.

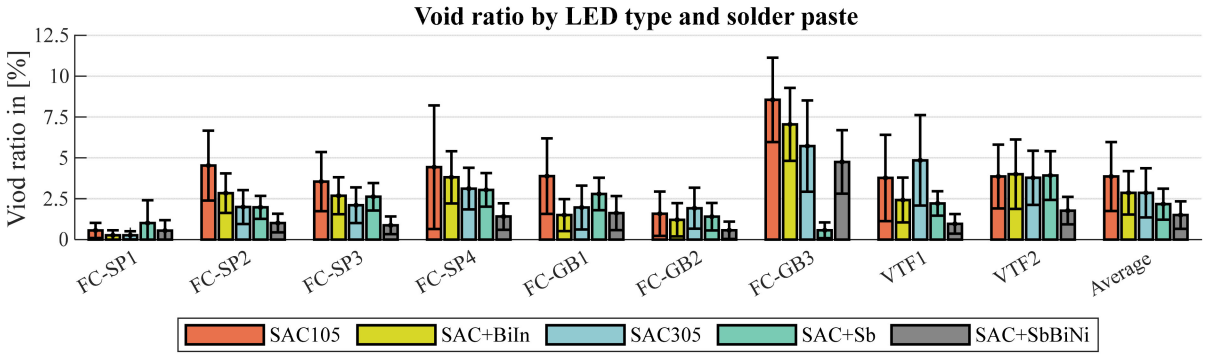



Fig. 6. Average void ratio and standard deviation separated by LED type and solder pastes. On the right side, the average void ratio over all LED types is added. The solder pastes are sorted by ascending silver parts from left to right.

TABLE IV
AVERAGE AND STANDARD DERIVATION OF THE FORWARD VOLTAGE AT SENSE AND NOMINAL CURRENT PLUS SENSITIVITY SEPARATED BY LED TYPES

| | | | FC-SP1 | FC-SP2 | FC-SP3 | FC-SP4 | FC-GB1 | FC-GB2 | FC-GB3 | VTF1 | VTF2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_f(I_{Sense})$ | Ø | [V] | 2.64 | 2.60 | 2.62 | 2.64 | 2.71 | 2.63 | 2.63 | 2.65 | 2.65 |
| | σ | [V] | ±0.003 | ±0.005 | ±0.004 | ±0.003 | ±0.004 | ±0.005 | ±0.007 | ±0.011 | ±0.021 |
| *SEN* | Ø | [mV/K] | -1.04 | -1.11 | -1.08 | -1.08 | -2.00 | -1.21 | -1.25 | -1.45 | -1.63 |
| | σ | (rel.) | ±1.3% | ±1.1% | ±1.0% | ±1.0% | ±1.1% | ±4.4% | ±4.6% | ±10.6% | ±12.2% |
| $V_f$ ($I_{Nom}$) | Bin.-R. | [V] | 2.75 ... 3.0 (1) | 2.9 (2, 3) | 2.9 ... 3.5 (1) | 2.8 ... 3.4 | 2.79 ... 3.03 (1, 2) | 2.9 ... 3.5 | 2.9 ... 3.9 | 3.0 ... 3.25 (1) | 3.0 ... 3.25 (1) |
| | Ø | [V] | 2.98 | 2.95 | 3.08 | 3.16 | 2.95 | 3.10 | 3.23 | 3.05 | 2.99 |
| | σ | [V] | ±0.008 | ±0.021 | ±0.020 | ±0.023 | ±0.006 | ±0.034 | ±0.032 | ±0.051 | ±0.029 |

(1) Without reaching thermal equilibrium ($t_{measurement} < 25$ ms)

(2) Measured at 85 °C

(3) No Range given in the datasheet

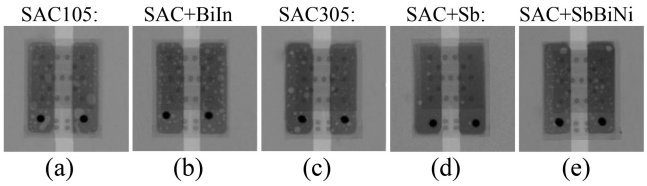



Fig. 7. Voiding of the solder paste for five representative LEDs of type FC-GB3. Besides for (d) SAC+Sb, all other pastes showed intense voiding.

Overall, a linear dependency between *SEN* and $V_f(I_{Sense})$ is observable in Fig. 8(b) over all LEDs. With increasing $V_f(I_{Sense})$, *SEN* is decreasing (the absolute value of *SEN* is rising). This behavior can be explained using the theoretical approach

$$SEN = \underbrace{\frac{eV_f - E_g}{eT} + \frac{1}{e}\frac{dE_g}{dT} - \frac{3k_B}{e}}_{due\ to\ junction} \underbrace{- \frac{1}{2}\frac{E_a + 2Sk_BT}{k_BT^2} IR_S}_{due\ to\ resistance} \quad (6)$$

with the band gap energy $E_g$, the elementary charge $e$, the Boltzmann constant $k_B$, the activation energy of the acceptors in the p neutral region $E_a$ and the parameter $S = -2/3$ at room temperature [28], [29]. Since the temperature dependency of only the junction [30] would describe an inverse behavior then observed in Fig. 8(b), (6) is extended by the temperature dependency the serial resistance $R_S$ of the p neutral region. Higher $R_S$ increases $V_f(I_{Sense})$ and also decreases *SEN*, but the observed $R_S < 0,5\Omega$ at nominal condition would solely cause a significant lower change of the *SEN* and didn't explain the magnitude. However, for the low $I_{Sense}$ the LED is not specified in the datasheet since these currents doesn't affect the normal operation range. Therefore, inhomogeneous current distribution at the low $I_{Sense}$ can be a potential reason which can increases $R_S$ significantly and explain the magnitude of the change of *SEN*. An inhomogeneous current distribution can cause a higher $R_S$ at $I_{Sense}$, due to a reduction of the effective area through which the current flows. A potential reason for that is the lower number of n-Vias for the LEDs which reveal the negative dependency of SEN from $V_f(I_{Sense})$ compared to the higher number of n-Vias for the FC-SP LEDs, for which the effect wasn't observed. Further investigations are required and ongoing to proof this hypothesis.

### C. Forward Voltage at Nominal Current

$V_f$ was measured at $I_{Nom}$ for all LEDs by considering the last stable measurement point while heating in the TTA sequence, meaning in thermal equilibrium after 3 s. However, the manufacturers mention different measurement conditions in their datasheet (e.g., at a higher temperature or without reaching thermal equilibrium) and therefore the values are not directly comparable.

The binning voltage ranges from the datasheets plus the measured average and variance of $V_f(I_{Nom})$ are summarized in Table IV. Compared to $V_f(I_{Sense})$, the variance of $V_f(I_{Nom})$ is increased for all LED types. At $I_{Nom}$, besides

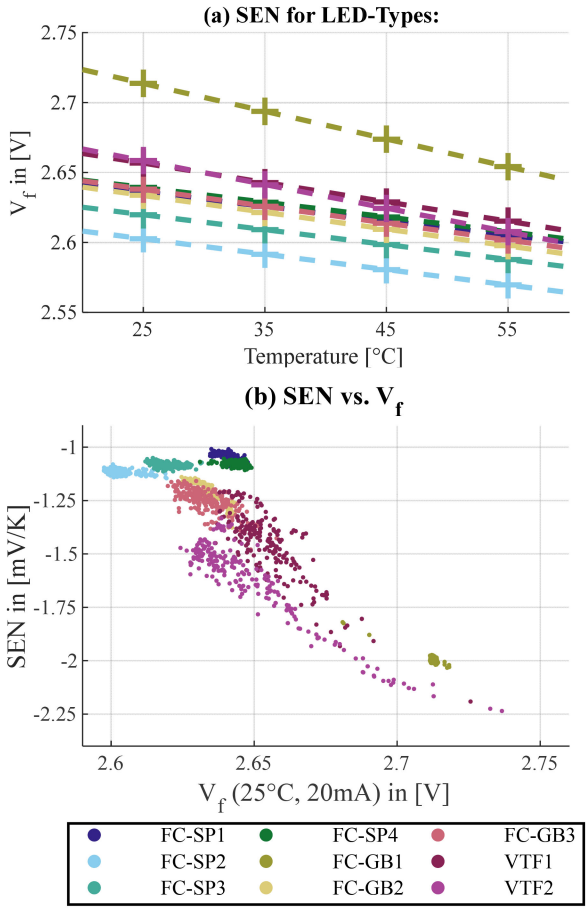



Fig. 8. (a) Measured $V_f$ at $I_{Sense}$ at different temperatures for one sample LED of each type. The measurement points are marked with crosses and the calculated linear fit as dashed line. The slope of the linear fit represents the sensitivity SEN. (b) SEN over $V_f$ at 25°C at $I_{Sense}$ for all sample in form of a point cloud. Each point represents one LED.

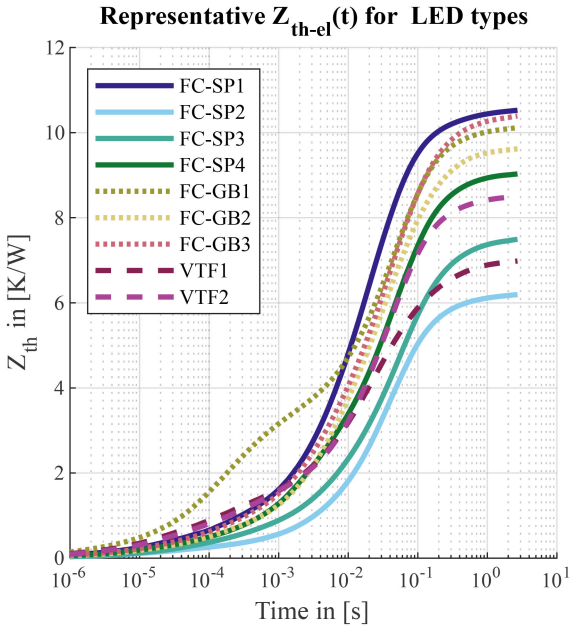



Fig. 9. Thermal impedance $Z_{th}(t)$ of one representative sample LED of each LED type. The line styles of the curves refer to the different chip technologies. Solid Line: FC-SP; Dotted Line: FC-GB; Dashed Line: VFC.

the semiconductor pn-junction itself, the variance of parasitic serial resistance of Ω-Layer and package affects the electrical behavior, causing the higher variation. Except for VTF1 and VTF2, all samples are inside the specified binning range, with a variance much smaller than the range itself. VTF1 and VTF2 both specify $V_f(I_{Nom})$ not at thermal equilibrium but after a short pulse, causing an average value close to the lower border with a few samples below the specified range.

### D. Interpretation of the Thermal Impedance

The results in $Z_{th}(t)$ for one representative sample LED of each type are plotted in Fig. 9 with the different chip technologies assigned to different line styles (Solid line: FC-SP, Dotted line: FC-GB and Dashed Line: VTF).

In the early time range until approx. 1 ms all LEDs follow similar trends except FC-GB1 (above), FC-SP2 and FC-SP3 (both below). This time range is mainly defined by the thermal properties of the LED die and the attach technology to the ceramic/copper submount. FC-GB1 shows a poorer thermal performance in this time range due to the underfill in the gold bump layer. For FC-GB2 and FC-GB3 (using the same technology), this effect was not observed. The smaller gold bump height (15 $\mu$m compared to 30 $\mu$m of the FC-GB1) and a higher thermal conductivity of the underfill are possible reasons. For FC-SP2 and FC-SP3 the better thermal performance in early time range is explicable by wider heat spreading due to a larger die (1.9 mm$^2$ resp. 1.3 mm$^2$ compared to approx. 1.0 mm$^2$ for the others). However, FC-SP1 has the smallest die with 0.6 mm$^2$ but is comparable to the other LEDs, implying good die design and die attach for this LED type.

After 1 ms, the $Z_{th}(t)$ curves follow different trends and finally terminate in different steady state $R_{th}$ values. This time range is mainly defined by the ceramic/copper submount, the solder interconnect, the substrate and the TIM to the temperature stable plate. The lowest $R_{th}$ with 6.1 K/W is achieved by the FC-SP2 due to the largest die and good package properties. Next best with ca. 6.8 K/W is the VTF1 with the largest package (14 mm$^2$) and solder pad design (5.4 mm$^2$), allowing a better thermal dissipation through wider head spreading. Additionally, a copper submount has a higher thermal conductivity than a ceramic submount. FC-SP3 reached the third lowest $R_{th}$ with 7.4 K/W. Here as well the reason is the better heat spreading due to a larger package with 5.0 mm$^2$ compared to the remaining LEDs.

FC-SP4, FC-GB2, FC-GB3 and VTF2 reached different $R_{th}$, even if all have similar package sizes between 2.5 and 3.0 mm$^2$. FC-GB2 and FC-GB3 show a poorer performance with ca. 9.5 K/W resp. 10.3 K/W. The early $Z_{th}(t)$ separation from the other two before 10 ms suggest that the ceramic submount is the limiting factor. The thinner submount metallization or an inferior thermal conductivity of the ceramic itself are possible reasons. The different trend between these two after 100 ms is explainable by the pad design, whereby the three-pad design of FC-GB2 is advantageous compared to the two-pad design of FC-GB3. Also, for VTF2 and FC-SP4 the pad design is potentially responsible for different $R_{th}$ with

8.4 K/W resp. 9.0 K/W. For VTF2 all three pads have approx. the same size, allowing a shared heat transfer which seems to show better performance than one huge thermal pad and two smaller electrical pads of FC-SP4.

FC-GB1 reached a $R_{th}$ of 10.0 K/W, much above the expected value according the great package size of 4.4 mm$^2$. The increase of $Z_{th}(t)$ after 1 ms is comparable to FC-SP3 with a similar size, but the huge difference already emerged earlier due to the gold bumps and underfill previously mentioned, causing the higher $R_{th}$.

With ca. 10.6 K/W, the FC-SP1 has the highest $R_{th}$ caused by the smallest die and package size. However, the good die and package design allows a comparable thermal performance even with a smaller size.

### *E. Rating of the Thermal Impedance by Time Interval Separation*

Interpreting and understanding TTA curves is one thing, but direct quantitative rating is difficult. Therefore, the $Z_{th}(t)$ curves are separated into three main time intervals in this paper using the dual interface (TDI) method described in [22]. First one is dedicated to the LED package and ends at the time $t_{Case\text{-}LED}$. The second interval is dedicated to the solder interconnect and substrate and ends with $t_{Case\text{-}Sub}$. The final interval is dedicated to the TIM and last until the end. The change in $Z_{th}(t)$ within these intervals is defined as the thermal resistance of the LED package for junction to case $R_{th\text{-}JC}$, the thermal resistance of solder interconnect and substrate $R_{th\text{-}S\&S}$ and the thermal resistance of the TIM $R_{th\text{-}TIM}$.

The times $t_{Case\text{-}LED}$ and $t_{Case\text{-}Sub}$ are determined individually for each LED type. For $t_{Case\text{-}Sub}$, one sample is measured two times, once with the standard TIM and once without TIM, leading to a reduced thermal performance. At the point of separation, the influence of the substrate on $Z_{th}(t)$ is ending and the TIM defines the further behavior. The separation point is therefore defined as $t_{Case\text{-}Sub}$ and is determined by inspection of the difference $\Delta a(z)$ between the two measurements.

For $t_{Case\text{-}LED}$, the process is more complex since no changes can be carried out in the solder interconnect for one sample. Instead, two different samples with different voiding ratios are used. Voids reduce the heat flow cross section of the solder interconnect and decrease the thermal performance. However, the samples for this method have to be selected carefully to avoid artefacts earlier then $t_{Case\text{-}LED}$ due to different package properties. Also, too high void ratios in one interconnect, especially single big voids, lead to an earlier separation because the heat flow inside the LED package is changed. The process to determine $t_{Case\text{-}LED}$ is exemplary described for FC-GB3 in Fig. 10 showing the difference $\Delta Z_{th}(t)$ in (a) and difference $\Delta a(z)$ in (b) of two low void samples (bluish lines), two mid void samples (reddish lines) and an inadequate sample in grey. Earlier than 10 ms, no difference in *a(z)* between the low and mid void samples is observed, implying a lack of thermal difference. Afterwards the mid void samples show a higher *a(z)* because of voiding and the exact separation point (marked as vertical dashed line in Fig. 10) is determined when the value

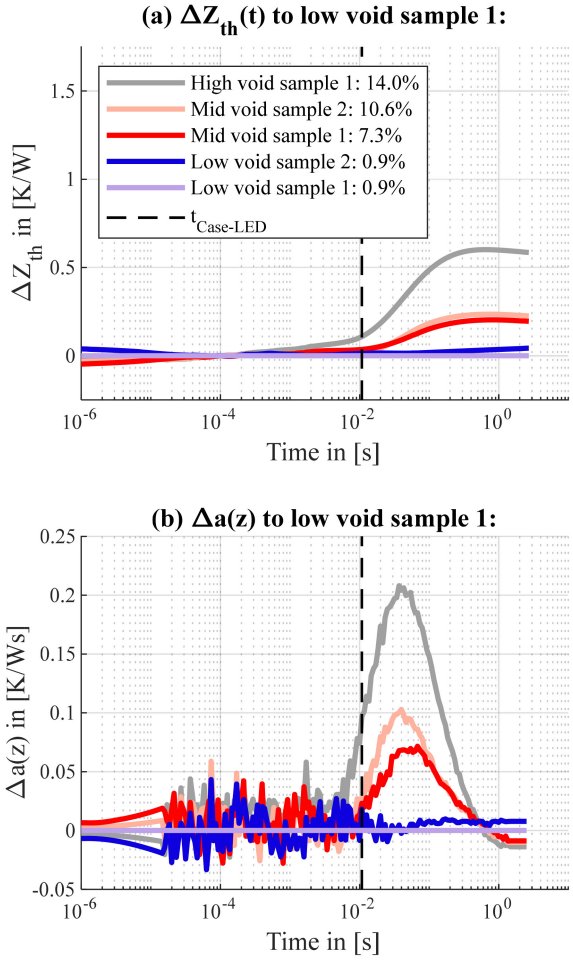



Fig. 10. Transient dual interface method adapted to determine $t_{Case\text{-}LED}$ for $R_{th\text{-}JC}$ calculation of the LED package by comparing samples with different void ratios. (a) shows the difference $\Delta Z_{th}(t)$ between the sample under test and the low void reference sample 1 and (b) shows the difference $\Delta a(z)$ between the samples and the low void reference sample 1.

is significantly larger than the noise, e.g., at 10% of the maximum $\Delta a(z)$. For the inadequate sample the separation occurs earlier, showing how its use would cause a wrong estimation. Instead of using $\Delta a(z)$ like in this paper, $\Delta Z_{th}(t)$ can be also used, but the lower sensitivity to changes leads to later separation points visible in Fig. 10(a).

This method was only possible using solely samples from the study for FC-GB3. For all other types, the number of higher voided samples was too low. Therefore, additional samples were soldered using a modified SAC105 paste, e.g., with addition of Ni particles, where larger void ratios are created. This paste showed a slightly higher voiding with approx. 5% on average for all LED types. Actually, when using a standard reflow profile without vacuum, the distribution of voids is much broader and high void and low void samples can be found in every solder batch.

The results for $t_{Case\text{-}LED}$ and $t_{Case\text{-}Sub}$ together with the average and variance values of $R_{th\text{-}JC}$, $R_{th\text{-}S\&S}$ and $R_{th}$ are summarized in Table V and Fig. 11. For $R_{th\text{-}JC}$, the maximum (red horizontal lines), minimum (blue horizontal lines) and/or typical value (black horizontal lines) from the datasheet are added if available.

TABLE V
AVERAGE AND STANDARD DEVIATION OF THERMAL RESISTANCES JUNCTION TO CASE, SOLDER & SUBSTRATE AND COMPLETE PLUS RELATED SEPARATION TIMES OF THE LED TYPES

| | | | FC-SP1 | FC-SP2 | FC-SP3 | FC-SP4 | FC-GB1 | FC-GB2 | FC-GB3 | VTF1 | VTF2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{Case\text{-}LED}$ | | [ms] | 6.0 | 14 | 18 | 9.5 | 21 | 10 | 11.0 | 9.0 | 15 |
| $R_{th\text{-}JC}$ | Ø | [K/W] | 3.77 | 2.08 | 3.01 | 3.19 | 5.52 | 3.62 | 4.04 | 2.90 | 3.68 |
| | σ | [K/W] | ±0.07 | ±0.09 | ±0.08 | ±0.07 | ±0.11 | ±0.09 | ±0.14 | ±0.09 | ±0.010 |
| $t_{Case\text{-}Sub}$ | | [ms] | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| $R_{th\text{-}S\&S}$ | Ø | [K/W] | 5.97 | 2.98 | 2.79 | 4.13 | 2.93 | 4.30 | 4.54 | 2.81 | 3.49 |
| | σ | [K/W] | ±0.16 | ±0.09 | ±0.05 | ±0.10 | ±0.05 | ±0.08 | ±0.16 | ±0.05 | ±0.08 |
| $R_{th}$ | Ø | [K/W] | 10.59 | 6.15 | 7.42 | 8.98 | 10.05 | 9.52 | 10.32 | 6.82 | 8.41 |
| | σ | [K/W] | ±0.19 | ±0.19 | ±0.13 | ±0.19 | ±0.17 | ±0.12 | ±0.30 | ±0.15 | ±0.17 |

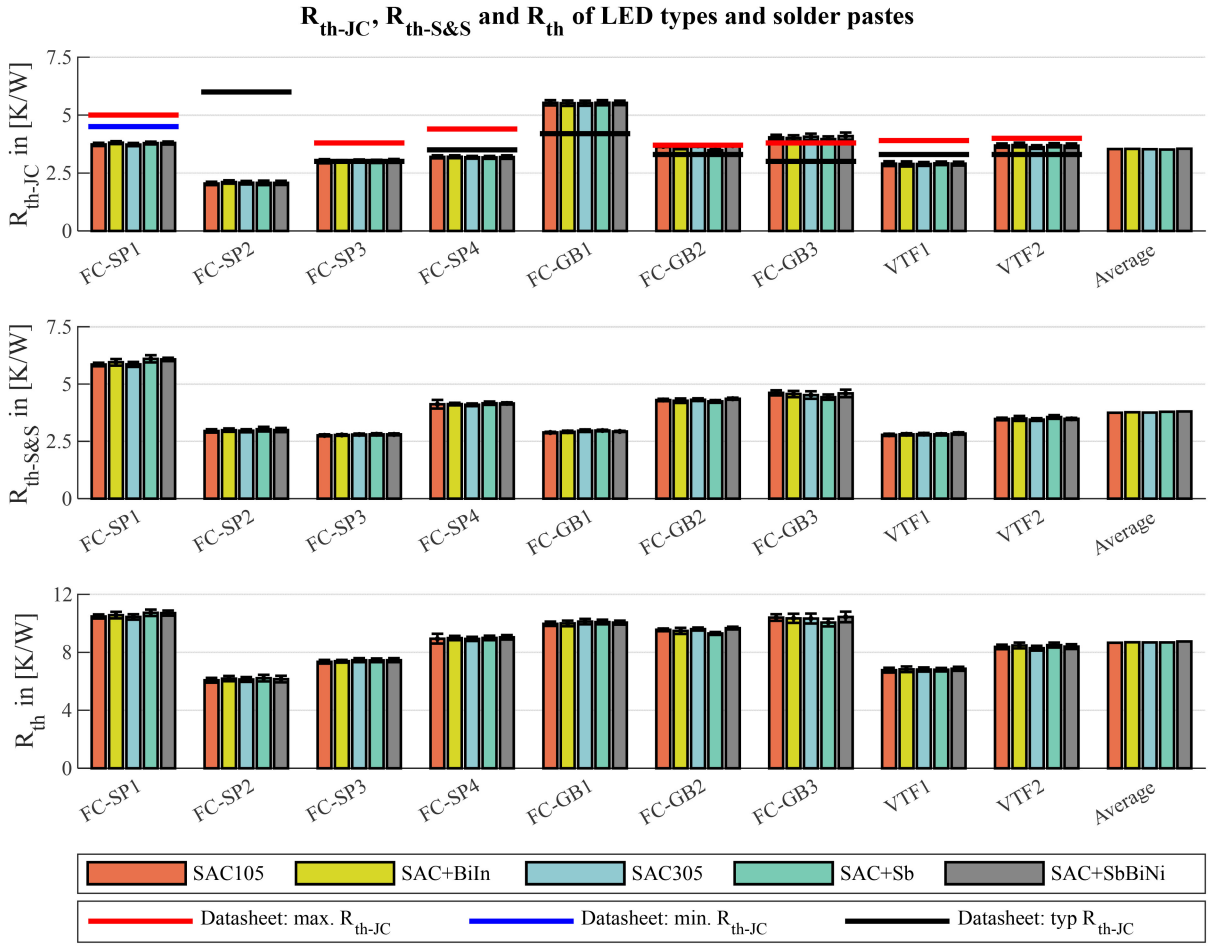



Fig. 11. Average and standard deviation of $R_{th\text{-}JC}$, $R_{th\text{-}S\&S}$ and $R_{th}$ grouped by LED type and solder pastes. Each group contains 40 LEDs. On the right side the average over all LEDs with the same solder paste is added.

With around 10 ms, $t_{Case\text{-}LED}$ is in a similar range for all LEDs. The two LEDs with copper submount (FC-SP1 and VTF1) showed smaller $t_{Case\text{-}LED}$ due to the higher thermal diffusivity of copper compared to AlN allowing a faster heat transfer [31]. With 100 ms, $t_{Case\text{-}Sub}$ is identical for all LEDs since it's mainly defined by the IMS-PCB, which is identical for all.

For $R_{th\text{-}JC}$, only small variances due to variations in manufacturing process are observed, with no dependency on the solder paste for all LED types. In case of a maximal $R_{th\text{-}JC}$ given by the datasheet, all LEDs were below this level except FC-GB3 exceeding it slightly. Conspicuous is the FC-SP2 with a measured $R_{th\text{-}JC}$ far below the typical value mentioned in the datasheet, only reasonably explained by a very conservative estimation of the manufacturer. FC-GB1 is found above the typical value. However, the datasheet mentions only one $R_{th\text{-}JC}$ for all optical efficiency bins. The used LEDs were from the poorest bin and hence produce more thermal losses at same electrical input, which increases $Z_{th\text{-}el.}(t)$.

This adaption of the TDI is an efficient way to determine $R_{th\text{-}JC}$ without relying on the datasheet value. However, depending on the location of the voids, a slight variation is

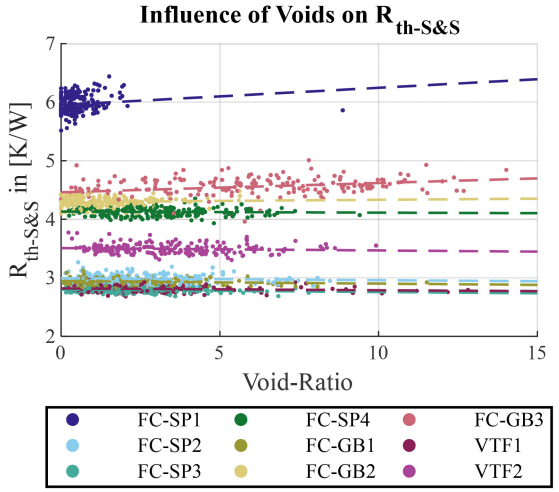



Fig. 12. Correlation between void ratio and $R_{th\text{-}S\&S}$. Each point represents a single LED separated by color for the different LED types. A linear fit is added for every LED type as dashed line.

observed but well below 10%. Compared to other methods to separate $R_{th}$ of the package from the contribution of the board, the method is accurate and in addition requires no further material or experimental effort.

For $R_{th\text{-}S\&S}$ only slight variances are observed for most of the LED types, mainly due to material variations of the IMS-PCB dielectric. For FC-GB3, the SAC+Sb paste shows a smaller average $R_{th\text{-}S\&S}$ due to the lower voiding compared to the other pastes (see Section IV-A). A greater variation is observed for FC-SP1 where SAC+Sb and SAC+SbBiNi show higher average values and also a higher voiding. Overall $R_{th\text{-}S\&S}$ correlates with the solder pad size of the LEDs. FC-SP1 with the smallest pads and therefore least heat spreading shows the highest $R_{th\text{-}S\&S}$, followed by FC-GB2, FC-GB3 and FC-SP4 with the next smallest pad size. However, the distinctly bigger pad size of VTF1 compared to the others does not reduce $R_{th\text{-}S\&S}$ to the same extent.

A simple rating is also possible with $R_{th}$, but the variance is higher compared to $R_{th\text{-}JC}$ and $R_{th\text{-}S\&S}$. $R_{th}$ depends on the thermal properties of TIM, susceptible to changes by deterioration due to usage and compression force. This study also concentrates on the degradation of LED, solder interconnect and substrate and therefore the TIM is excluded from the data by analyzing $R_{th\text{-}JC}$ and $R_{th\text{-}S\&S}$ in the defined time intervals.

### *F. Influence of Voids on the Thermal Resistance*

To evaluate the influence of voids on the thermal performance, the void ratio is plotted against $R_{th\text{-}S\&S}$ in Fig. 12. Each point represents an LED and the different LED types are separated by color. A linear fit was used to determine the correlation for all LED types and is shown in Fig. 12 as a dashed line. An identifiable increase of $R_{th\text{-}S\&S}$ with the void ratio is only observed for LEDs with already the highest $R_{th\text{-}S\&S}$ (FC-SP1, FC-GB3) and their correlation listed in Table VI. For FC-GB3 a 10% voiding ratio leads to an increase of 0.16 K/W on average, which is close to the expected increase of 0.11 K/W (interconnect height: 40 $\mu$m; thermal conductivity: 58 W/mK; assumption of constant interconnect volume, i.e., height is increased by 10% for the voided interconnect). The remaining part is caused by the cross-section reduction in the substrate due to the voids. A rise by 0.16 K/W would be an increase of only 3.6% in $R_{th\text{-}S\&S}$ and of 1.6% on $R_{th}$. For FC-SP1, 10% voiding results in 0.3 K/W increase, a change of 5.0% in $R_{th\text{-}S\&S}$ and of 2.8% on $R_{th}$. The expected increase of the interconnect would be 0.20 K/W. However, for FC-SP1 the correlation is not accurate for higher voiding since no samples were in this range. All others LED types showed no correlation between $R_{th\text{-}S\&S}$ and void ratio. Compared to the variance of $R_{th\text{-}S\&S}$ in total, the influence of voiding is small and voiding under a certain limit is uncritical for the initial thermal performance for all LEDs in this study.

TABLE VI
CORRELATION BETWEEN VOID RATIO AND $R_{th\text{-}S\&S}$

| LED | Linear correlation: $R_{th\text{-}S\&S}$(Void ratio) |
|---|---|
| FC-SP1 | 5.95 K/W + 0.030 K/W * (Void-Ratio in %) |
| FC-GB3 | 4.46 K/W + 0.016 K/W * (Void-Ratio in %) |

## V. OUTLOOK

The second paper about this study will concentrate on the long-time thermal performance of the LEDs and the solder paste. Thermal shock cycling between −40 °C and 125 °C for 1500 cycles is used for accelerated ageing and the LEDs measured after certain cycling progress by TTA, SAM and X-ray and destructive cross-sections. The main goal is to observe the degradation process of LED, solder interconnect and substrate to evaluate key parameters for quality and reliability for LED lighting modules.

## VI. CONCLUSION

An extensive reliability study with 1800 white high-power LEDs is carried out having nine LED packages from different LED manufactures and five solder pastes under investigation. The dominating package types for high-power LEDs is the ceramic submount package, i.e., only two lead frame packages were identified for the study. In this paper, the measurement methods X-Ray, SAM and TTA are described, which are applied for the first time in combination in such a large reliability study. First, X-ray images were used to determine the void ratio with an in-house developed algorithm to disregard disturbing internal LED package structures. Through the used vacuum soldering profile, the void ratio was kept under 4% on average for all LEDs except one LED type, which showed higher voiding. With increasing proportions of silver in the paste, less voids are observed. Second, SAM images provided a smaller resolution compared to X-ray impeding an accurate void ratio determination, but SAM will be important and reveal it strength later when inspecting solder interconnect crack propagation. Third, TTA was used to rate the initial thermal performance of the LEDs. The temperature sensitivity was inspected individually for every LED, showing a sensitivity range between −1.0 mV/K and −2.0 mV/K, strongly dependent on the LED type. Due to variance inside one LED type, some LED types require an individual inspection of

the sensitivity to obtain accurate TTA data, but not all. The interpretation of the thermal impedance of the LED types allows an analysis of the package designs with pros and cons. For a quantitative rating, the transient dual interface (TDI) method was applied to low and mid voided LEDs and the package thermal resistance $R_{th\text{-}JC}$ was measured directly. TDI was also applied to measure the thermal resistance of solder and substrate $R_{th\text{-}S\&S}$. Especially for $R_{th\text{-}JC}$ this is a simple, in the paper documented method, which enable to test datasheet values and separate LED failures from solder and substrate failures. Only slight variations in $R_{th\text{-}JC}$ are observed within the individual LED types, however, discrepancies with the data sheet values of some LEDs are found. For $R_{th\text{-}S\&S}$ nearly no differences are observed between the solder pastes, proving that the solder material has no influence on the initial thermal performance. A correlation between void ratio and $R_{th\text{-}S\&S}$ could be obtained for the two LEDs with the smallest solder area, where the contribution of the solder interconnect is relatively high. For all other LEDs, the achieved void ratio showed no measurable impact on the initial thermal performance. $R_{th\text{-}S\&S}$ depends on the LED package size. Larger packages allow a heat spreading inside the packages reducing $R_{th\text{-}S\&S}$, which has to be considered for the evaluation of the thermal performance.

## REFERENCES


[1] R. Karlicek, C.-C. Sun, G. Zissis, and R. Ma, *Handbook of Advanced Lighting Technology*. Cham, Switzerland: Springer, 2016.

[2] *Implementing Directive 2005/32/EC of the European Parliament and of the Council With Regard to Ecodesign Requirements for Non-Directional Household Lamps*, European Parliament, Brussel, Belgium, (EC) no. 244/2009, 2009.

[3] D. F. de Souza, P. P. F. da Silva, L. F. A. Fontenele, G. D. Barbosa, and M. de Oliveira Jesus, "Efficiency, quality, and environmental impacts: A comparative study of residential artificial lighting," *Energy Reports*, vol. 5, pp. 409–424, Nov. 2019, doi: 10.1016/j.egyr.2019.03.009.

[4] E. F. Schubert, *Light-Emitting Diodes*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2014.

[5] C. J. Lasance and A. Poppe, *Thermal Management for LED Applications*. New York, NY, USA: Springer, 2014.

[6] W. D. van Driel and X. J. Fan, *Solid State Lighting Reliability*. New York, NY, USA: Springer, 2013.

[7] X.-L. Hu, Z.-Y. Qi, H. Wang, and X.-C. Zhang, "Performance of InGaN-based thin-film LEDs with flip-chip configuration and concavely patterned surface fabricated on electroplating metallic substrate," *IEEE Photon. J.*, vol. 8, no. 1, Feb. 2016, Art. no. 1600307, doi: 10.1109/JPHOT.2016.2516911.

[8] Lumileds, Amsterdam, The Netherlands, "LUXEON FlipChip and LUXEON FlipChip UV: Assembly and Handling Information," 2015. [Online]. Available: https://www.lumileds.com/wp-content/uploads/files/AB116.pdf

[9] O. B. Shchekin, "High performance thin-film flip-chip InGaN–GaN light-emitting diodes," *Appl. Phys. Lett.*, vol. 89, no. 7, 2006, Art. no. 71109, doi: 10.1063/1.2337007.

[10] B. Hahn, B. Galler, and K. Engl, "Development of high-efficiency and high-power vertical light emitting diodes," *Jpn. J. Appl. Phys.*, vol. 53, no. 10, 2014, Art. no. 100208, doi: 10.7567/jjap.53.100208.

[11] H. Steen and B. Toleno, "Development of a lead-free alloy for high-reliability, high-temperature applications," in *Proc. IPC APEX EXPO*, 2009.

[12] *IPC J-STD-001E-2010: Requirements for Soldered Electrical and Electronic Assemblies*, IPC, Bannockburn, IL, USA, 2010.

[13] R. Vaga and K. Bryant, "Recent advances in x-ray technology," in *Proc. Pan Pac. Microelectron. Symp. (Pan Pacific)*, Big Island, HI, USA, 2016, pp. 99–108.

[14] P. Aryan, S. Sampath, and H. Sohn, "An overview of non-destructive testing methods for integrated circuit packaging inspection," *Sensors*, vol. 18, no. 7, p. 1981, 2018, doi: 10.3390/s18071981.

[15] H. E. Martz, C. M. Logan, D. J. Schneberk, and P. J. Shull, *X-Ray Imaging: Fundamentals, Industrial Techniques, and Applications/Harry*. Boca Raton, FL, USA: CRC Press, 2016.

[16] S. Branda, P. Czurratisb, P. Hoffroggeb, and M. Petzolda, "Automated inspection and classification of flip-chip-contacts using scanning acoustic microscopy," *Microelectron. Rel.*, vol. 50, no. 9, pp. 1469–1473, 2010.

[17] M. Y. Mehr *et al.* "An overview of scanning acoustic microscope, a reliable method for non-destructive failure analysis of microelectronic components," in *Proc. 16th Int. Conf. Thermal Mech. Multi Phys. Simulat. Exp. Microelectron. Microsyst. (EuroSimE)*, Budapest, Hungary, 2015, pp. 1–4.

[18] R. S. Gilmore, K. C. Tam, J. D. Young, and D. R. Howard, "Acoustic microscopy from 10 to 100 MHz for industrial applications," *Philosoph. Trans. Roy. Soc. London Series A, Math. Phys. Sci.*, vol. 320, no. 1554, pp. 215–235, 1986.

[19] F. Bertocci, A. Grandoni, and T. Djuric-Rissner, "Scanning acoustic microscopy (SAM): A robust method for defect detection during the manufacturing process of ultrasound probes for medical imaging," *Sensors*, vol. 19, no. 22, p. 4868, 2019.

[20] *Implementation of the Electrical Test Method for the Measurement of Real Thermal Resistance and Impedance of Light-Emitting Diodes With Exposed Cooling*, JEDEC, Arlington, VA, USA, JESD51–51, Apr. 2012.

[21] T. Q. Khanh, P. Bodrogi, Q. T. Vinh, and H. Winkler, *LED Lighting: Technology and Perception*. Weinheim, Germany: Wiley-VCH, 2015.

[22] *Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices With Heat Flow Through a Single Path*, JEDEC, Arlington, VA, USA, JESD51–14, Nov. 2010.

[23] A. Hanss, M. Schmid, E. Liu, and G. Elger, "Transient thermal analysis as measurement method for IC package structural integrity," *Chin. Phys. B*, vol. 24, no. 6, 2015, Art. no. 68105.

[24] V. Székely, "A new evaluation method of thermal transient measurement results," *Microelectron. J.*, vol. 28, no. 3, pp. 277–292, 1997.

[25] G. Elger, M. Schmid, A. Hanss, and D. Müller, "Automatic panel level transient thermal tester," in *Proc. LED Professional Symp. Expo*, 2017, pp. 44–51.

[26] O. Kovac, T. Girasek, and A. Pietrikova, "Image processing of die attach's X-ray images for automatic voids detection and evaluation," in *Proc. 39th Int. Spring Seminar Electron. Technol. (ISSE)*, Pilsen, Czech Republic, 2016, pp. 199–203.

[27] M. Pal and P. Bharati, *Applications of Regression Techniques*. Singapore: Springer, 2019.

[28] D. S. Meyaard, J. Cho, E. F. Schubert, S.-H. Han, M.-H. Kim, and C. Sone, "Analysis of the temperature dependence of the forward voltage characteristics of GaInN light-emitting diodes," *Appl. Phys. Lett.*, vol. 103, no. 12, 2013, Art. no. 121103, doi: 10.1063/1.4821538.

[29] Y. Xi *et al.*, "Junction temperature in ultraviolet light-emitting diodes," *Jpn. J. Appl. Phys.*, vol. 44, no. 10, pp. 7260–7266, 2005.

[30] Y. Xi and E. F. Schubert, "Junction–Temperature measurement in GaN ultraviolet light-emitting diodes using diode forward voltage method," *Appl. Phys. Lett.*, vol. 85, no. 12, pp. 2163–2165, 2004, doi: 10.1063/1.1795351.

[31] A. N. Salazar, "On thermal diffusivity," *Eur. J. Phys.*, vol. 24, no. 4, pp. 351–358, 2003, doi: 10.1088/0143–0807/24/4/353.