Guest Editorial
TDMR IIRW Special Section

FOR YEARS, the IEEE International Integrated Reliability Workshop (IIRW) has been held at the edge of Fallen Leaf Lake in California, just south of Lake Tahoe. Typically, the conference is a four-day event comprised of lively discussions, beautiful vistas, and is an unparalleled informal event that is a fertile ground for the exchange of ideas and professional networking. For 2020 however, the conference was held virtually over a one-month period and was comprised of a blend of live video content and pre-recorded presentations.

The 2020 IIRW technical program solicited research focused on thermal simulation, novel materials and devices, gate and ILD dielectrics, plasma damage mechanisms, back end of line (BEOL) defect mechanisms, and advanced packaging reliability. In addition, there were multiple emerging memory and FinFET submissions.

The third reliability expert's forum (REF) at the 2020 IIRW was composed of moderated, focused discussions with industry experts in three distinct areas: BEOL time dependent dielectric breakdown (TDDB), electromigration (EM) and stress migration (SM). These live video conferences had a large audience and drew many questions and comments-from the attendees.

The conference drew 83 attendees from Europe, Asia, and the Americas. The diverse technical program contained a blend of tutorials, invited talks and submitted research. There were 21 accepted submissions for 2020 from nine countries representing governmental, academic, and industrial affiliations. The four invited talks included a discussion on FinFET self-heating, an overview of the accelerated testing used on SiC power devices, a look at plasma damage detection and test structure design, as well as the on-state threshold voltage instability of GaN HEMTs. The five tutorials, each presented as a live video event, covered a broad array of reliability topics. Advanced packaging reliability challenges, emerging applications for neuromorphic networks, atomistic simulation of oxide degradation, analysis of random telegraph noise (RTN), and photonics reliability were all covered in the tutorials for the 2020 IIRW.

The five selected papers represented in this special section are a cross-section of the material presented at IIRW 2020. One invited paper, two student papers, and two other submissions accepted for oral talks comprise this group. Topics ranging from GaN devices, to plasma damage on planar Hi-K FET devices, neural networks, the interface layer effects for SiHfO2 ferroelectric FET's (FeFET's), and the defect step height distributions for SiON dielectric transistors.

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In the first paper, Dr. Arno Stockman and his co-authors discuss the effect of changing the AlGaN/GaN high electron mobility transistor (HEMT) p-GaN sidewall passivation treatment has on the threshold voltage variation with applied stress duration. The authors show that with the change in sidewall passivation, the on-state gate current correlates to gate area with one treatment, while the gate perimeter correlates to the on-state current with the original p-GaN passivation. The authors also discuss the mechanism for the improved threshold voltage variation due to changes in the charge trapping mechanisms during HEMT stress.

The second paper discusses impact of the hafnium dioxide to silicon interface layer on device characteristics of SiHfO2 based FeFET's. Taehwan Jung and co-authors describe how the silicon termination being hydrogen rich or oxygen rich modulates the effective permittivity of the metal ferroelectric insulator semiconductor (MFIS) devices. The authors postulate the difference in effective permittivity is due to the ratio of structural phases in the HfO_2 material. The different phases are metastable at operational temperatures, and changes in HfO_2 phase composition affects the charge trapping vs. polarization behavior of the material. Changes in the carrier conduction mechanism will influence the change in Vt during extend measure-stress-measure testing. The paper indicates that the FeFETs fabricated with hydrogen–rich silicon interfacial layers displays only positive shift under bias stress at 25C or 85C, whereas the transistors fabricated with a SiO_2 or SiON terminated silicon layer exhibit a transition from positive ΔVt at elevated temperatures to a negative ΔVt at room temperature.

In the third paper, Tomasso Zanotti and co-authors investigate the circuit reliability effects of multiple binarized neural network (BNN) architectures using a physics based compact model calibrated from literature. The work highlights the BNN material implication (IMPLY) architecture's reliability concern as logic state degradation from the circuit reliability simulation. The degradation arises from positive voltage the P and Q transistors of the bit cell during the V_{SET} and V_{COND} voltage levels that degrades the RRAM resistance over time, resulting in bit corruption. The authors also compare the IMPLY BNN architecture with an alternate smart material implication (SIMPLY) architecture where transistor P and Q V_{SET} and V_{COND} level stay lower, and consequently little RRAM resistance degradation occurs.

In the fourth manuscript, Gaspard Hiblot and co-authors discuss the damage on high-κ (HK) replacement metal gate NMOS transistors caused by process plasma charging at the gate level. The number of plasma processes seen by gate level antenna structures on FinFETs studied in this work

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depends on the architecture used in fabrication. For the HK-first transistors, there are multiple plasma processes, including a plasma-etch and deposition process, where the HK-last process has only a PECVD process at the gate level. The difference in plasma processing steps results in HK-first material showing gate-induced drain leakage (GIDL) impacts correlated to the area and perimeters of the PID structures, while the HK-last transistors exhibit increased gate leakage correlated to the area ratio of the antenna to gate. The authors discuss the likely physical implication for the shifts seen, such as trap assisted tunneling (TAT) being responsible for the GIDL in the HK-first hardware.

For the fifth paper in this special section, Konstantinos Tselios and co-authors discuss the distribution of ΔVt step heights observed in the recovery phase of a BTI measure-stress-measure test and how these relate the Vt degradation of devices within technologies using SiON gate dielectrics. The authors report that a bi-modal exponential distribution of ΔVt step heights exists in the technology evaluated, and that when compared to the conventional charge sheet approximation (CSA) used in many simulations, the results are under-estimated by the CSA based tools. Additionally, the authors use a physics based compact model simulation tool with the extracted step-height distributions to predict the empirical results.

I would like to thank the IIRW 2020 Management committee for successfully producing the virtual event. Special thanks to Dr. Stanislav Tyaginov, the General chair, and Dr. Alexander Makarov, the IT chair, who both worked to devise and implement the virtual conference framework used.

I would like to express my gratitude to the authors in this special section, as the additional preparation for these expanded papers compared to the ones included in the IIRW 2020 proceedings is significant. The reviewers who carefully read and provided feedback to improve the manuscripts further are also due a hearty thank you.

In addition to the technical reviewers and authors, I would like to thank the Editor-in-Chief of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, Dr. Edmundo Gutierrez for the opportunity for the guest editorial of this special section. Lastly, I would like to thank Rosemary Schreiber for her help in keeping me focused on getting this IIRW special section to press and answering my questions in the process.

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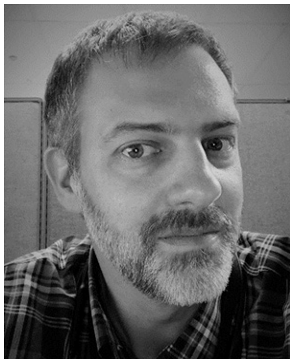

Matthew Ring received the B.S. degree in chemical engineering from the University of Maine in 2000, and the Ph.D. degree in electrical and computer engineering from the Iowa State University of Science and Technology in 2004, where he studied amorphous semiconductor devices and materials for solar cell and thin-film transistor applications. He has worked with Intel Corporation and Fairchild Semiconductor as a Process Development Engineer on multiple process technology nodes ranging from 45 to 500 nm. As a Reliability Engineer with Fairchild Semiconductor, and later ON Semiconductor, he has focused on back-end-of-line reliability failure mechanisms. He has increased his scope, including oxide and transistor reliability, during his tenure with the reliability organization. He is currently the Manager of the S. Portland Intrinsic Reliability Lab. He has authored multiple publications and two U.S. patents and has served on the IIRW Management Committee in various capacities, including the Technical Program Chair in 2020 and the General Chair in 2021.