Editorial—Robust System Design IEEE IOLTS 2019

YOU ARE reading the Editorial of the Special Section of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY with a collection of the best papers of the 2019 edition of the IEEE IOLTS, an established IEEE symposium which focuses for exactly one quarter of a century on the challenges and solutions for computing and electronic circuits and systems *robust design*. Robustness from the IOLTS technical point of view spans across the circuit, microarchitecture, architecture, system, and software layers.

Held for its first twenty-one years as the IEEE International On-Line Testing Symposium it was afterwards renamed to the *International On-Line Testing and Robust Systems Design Symposium* keeping its well recognized acronym IOLTS; the 25th edition was held in July 2019 in the beautiful island of Rhodes, Greece attracting a large number of high quality paper submissions and attendees from twenty-two countries around the globe.

The specialized technical meeting was first held since 1995 in the format of a Workshop (the IEEE International On-Line Testing Workshop – IOLTW – at that time) and was created at a time when the diversity of electronic systems applications was growing rapidly. This growth, together with formidable increase in system complexity, led to an increasing need for on-line detection and protection techniques. Thus, the need for on-line testing started to be felt beyond the traditional high RAS (Reliability Availability Serviceability) industry and new application domains started to rely on integrated circuits enabled by on-line testing to achieve market-driven dependability requirements. Its elevation from the IEEE from an informal Workshop to a formal Symposium in 2003 reflected the importance of these trends.

Since then, the needs for on-line testing techniques, and more generally for design for robustness (DfR) against any possible threat for the correctness of a system operation, has increased dramatically across all computing and electronics systems domains. This was the natural result of the unprecedented complexity increase of electronics, and more importantly, the aggressive nanometric scaling, which impacted adversely the noise margins, the process, voltage, and temperature variations, the aging and wear-out phenomena, the soft error rates, the EMI sensitivity, and the power density and heating requirements. The employment of design for robustness techniques became mandatory to improve the yield of chip manufacturing process, to increase the reliability of the system, and to extend the lifetime of modern integrated circuits. Design for reliability becomes also mandatory for low power design, as voltage reduction (often used to reduce power) and frequency boosting (often used to increase performance) both strongly affect reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, as well as by modifying the circuit delays and thus the likelihood and severity of timing faults. There is also a strong relation between design for reliability and design for security, as security attacks are often fault-based. These issues are further exacerbated, in the current era of massive parallel chips that will soon comprise thousands of processing cores and memories.

IOLTS, the International Symposium on On-Line Testing and Robust System Design is an established forum for presenting novel ideas and experimental data on all these areas, and is recognized among those working in the field as a major forum for identifying key problems and challenges, sharing unique experiences, as well as identifying innovative and effective solutions. An indication of IOLTS' technical value for the research community is the number of citations IOLTS papers regularly receive and place IOLTS among the highest cited events in the domain of Test and Reliability.

Interestingly, as DfX techniques are proliferating (Design for Test, Design for Debug, Design for Yield, Design for Reliability, Design for Low-Power, Design for Security, Design for Verification, ...), it becomes mandatory to address these issues holistically, in order to moderate their impact on area, power, and/or performance, and increase their global efficiency. There is therefore a related need for an international consolidated forum bringing together specialists from all these domains to enhance interactions and cross-fertilization. To address these needs, starting from 2016 the IOLTS is organized under the umbrella of the IEEE Federative Event on Design for Robustness (FEDfRo), which brings together, at the same time and place, several IEEE technical meetings focusing on these areas. The 2019 edition of IOLTS (to which this Special Section is devoted) was part of the 4th FEDfRo event.

The five papers of this Special Section of IEEE TDMR represent a subset of the best papers presented at the Symposium in July 2019 in Rhodes island, Greece. All papers are extended versions of those published in the IEEE proceedings of IOLTS 2019 and all manuscripts went through the IEEE TDMR peer-review process including revision rounds to comply with the technical suggestions of the reviewers and the manuscript quality requirements of the prestigious IEEE Transactions.

The first paper, "*Automated Die Inking*", by C. Xanthopoulos, A. Neckermann, P. List, K.-P. Tschernay, P. Sarson, and Y. Makris, introduces a novel machine learning-based methodology to predict devices that are likely to fail, based on their proximity to known failed devices on

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the wafer thus eliminating the need for time-consuming human intervention.

The second paper, "*Stealthy Information Leakage through Peripheral Exploitation in Modern Embedded Systems*" by D. Tychalas, A. Keliris, and M. Maniatakos discusses an information leakage attack in embedded systems which exploits peripheral devices and presents a generic defense scheme against such attacks.

The third paper, "*Run-time Protection of Multi-Core Processors from Power-Noise Denial-of-Service Attacks*", by V. Tenentes, S. Das, D. Rossi, B. Al-Hashimi discusses the other side of hardware security, i.e., denial-of-service attacks which exploit power viruses software in voltage scaled microprocessors and proposes a mitigation approach against such attacks.

The fourth paper, "*Cell-Aware Defect Diagnosis of Customer Returns Based on Supervised Learning*" by S. Mhamdi, P. Girard, A. Virazel, A. Bosio, E. Faehn, A. Ladhar proposes a new learning-guided approach for diagnosis of intra-cell defects that may occur in customer returns.

Finally, the fifth paper, "*Exceeding Conservative Limits: A Consolidated Analysis on Modern Hardware Margins*", by G. Papadimitriou, A. Chatzidimitriou, D. Gizopoulos, V. J. Reddi, J. Leng, B. Salami, O. Unsal, A. Cristal Kestelman is a comprehensive survey of the state-of-the-art in voltage scaling approaches at the system level for modern CPU, GPU, and FPGA hardware.

We would like to thank all successful authors of this Special Section and of course all the authors of the symposium papers for submitting the best of their work to IOLTS. As it wouldn't be possible to prepare this special section without the precious time devoted by the reviewers of the articles, we thank them very much for timely and diligently reviewing.

We also want to warmly thank the previous and current Editors-in-Chief of IEEE TDMR Tony Oates and Edmundo Gutiérrez-D. for giving us again the opportunity to summarize the best of IOLTS in one of the top IEEE Transactions series in the scientific domain of robust circuits and systems design (this is third time IOLTS best papers are hosted in TDMR). Last but not least, we owe special thanks to Rosemary Schreiber for a timely coordination of the peer review process under a tight schedule.

We hope you will enjoy the articles!

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