Analysis of Reduction in Lag Phenomena and Current Collapse in Field-Plate AlGaN/GaN HEMTs With High Acceptor Density in a Buffer Layer

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Abstract—We make a 2-D transient analysis of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer, where only a deep acceptor above the midgap is considered. The deep-acceptor density is varied between 10^{17} cm^{-3} and 8×10^{17} cm^{-3}. It is studied how the deep-acceptor density and the field plate affect the buffer-related drain lag and gate lag, and current collapse. It is shown that the lags and current collapse are reduced by introducing a field plate. This reduction occurs because electron trapping by the deep acceptors is weakened by the field plate. It is also shown that without a field plate, the drain lag and current collapse increase with increasing the deep-acceptor density as expected, although the gate lag decreases when the deep-acceptor density becomes high in the region between 2×10^{17} cm^{-3} and 8×10^{17} cm^{-3}. On the other hand, with a field plate, surprisingly, the lags and current collapse decrease when the deep-acceptor density becomes high. This is attributed to the fact that the reduction in drain lag and current collapse by introducing a field plate becomes more significant when the deep-acceptor density becomes higher.

Index Terms—AlGaN/GaN HEMT, buffer layer, current collapse, deep acceptor, field plate, two-dimensional analysis.

I. Introduction

RECENTLY, AlGaN/GaN high electron mobility transistors (HEMTs) are receiving a great interest because of their applications to high-power microwave devices and high-power switching devices [1], [2]. However, slow current transients are often observed even if the gate voltage and the drain voltage are changed abruptly [3]. These are called gate lag and drain lag. In microwave device applications, the slow current transients mean that RF current-voltage (*I-V*) curves can be quite different from the dc *I-V* curves, and this leads to a situation that the available RF power becomes rather lower than that expected from the dc operation [1]. This phenomenon is called current collapse. Experimentally, the current collapse is sometimes characterized as a current reduction in pulsed
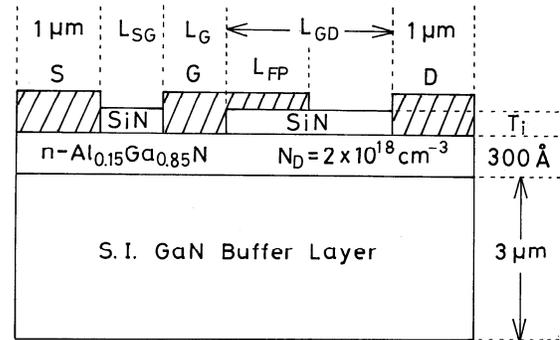
Fig. 1. Device structure analyzed in this study.

I-V curves from the dc *I-V* curves when the gate voltage is switched on. In switching device applications, the current collapse appears as an increase in dynamic on resistance [2]. These lags and current collapse are serious problems and many experimental studies have been made [1]–[11], and several theoretical studies have also been made [11]–[15]. As for the mechanisms, effects of surface states and traps in the buffer layer are suggested, but the detailed mechanisms are not well understood. Therefore, these phenomena are still significant problems now [9], [10], [15]. It is recognized both experimentally and theoretically that the introduction of field plate reduces the current collapse because the electric field at the drain edge of the gate is reduced [16]–[19]. The field plate is also known to increase the breakdown voltage of AlGaN/GaN HEMTs [20]–[23].

In our previous theoretical studies on lags and current collapse, the semi-insulating buffer layer is usually regarded as undoped, and a deep donor and a deep acceptor are considered in it [12], [24]. The deep donor is assumed to compensate the deep acceptor. Effects of field plate on lags and current collapse are also analyzed in the undoped case [18], [25]. On the other hand, recently, Fe- and C-doped semi-insulating buffer layers are receiving a great attention, and they act as deep acceptors [8], [26]–[29]. Particularly, the energy level of Fe lies above the midgap [26], [30]. So the deep acceptor may play the same electrical role as the deep donor in the undoped semi-insulating buffer layer. Therefore, it is interesting to analyze the case with the deep acceptor close to the conduction
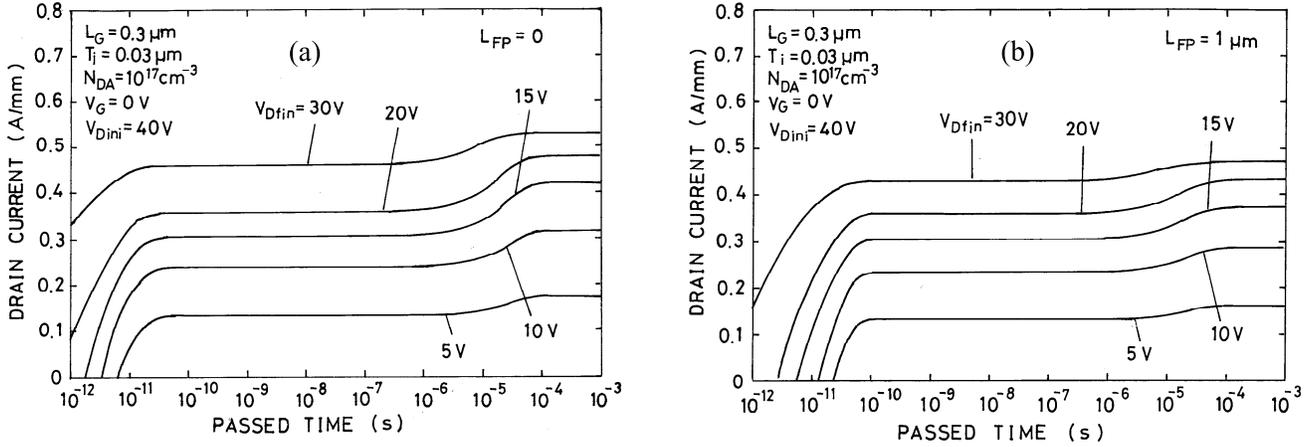
Fig. 2. Calculated drain-current responses of AlGaN/GaN HEMTs when V_D is changed abruptly from 40 V to V_{Dfin}. V_G is kept constant at 0V. $N_{DA} = 10^{17}$ cm^{-3} and $E_C - E_{DA} = 0.5$ eV. (a) Without field plate ($L_{FP} = 0$), (b) with field plate ($L_{FP} = 1$ μm, $T_1 = 0.03$ μm).
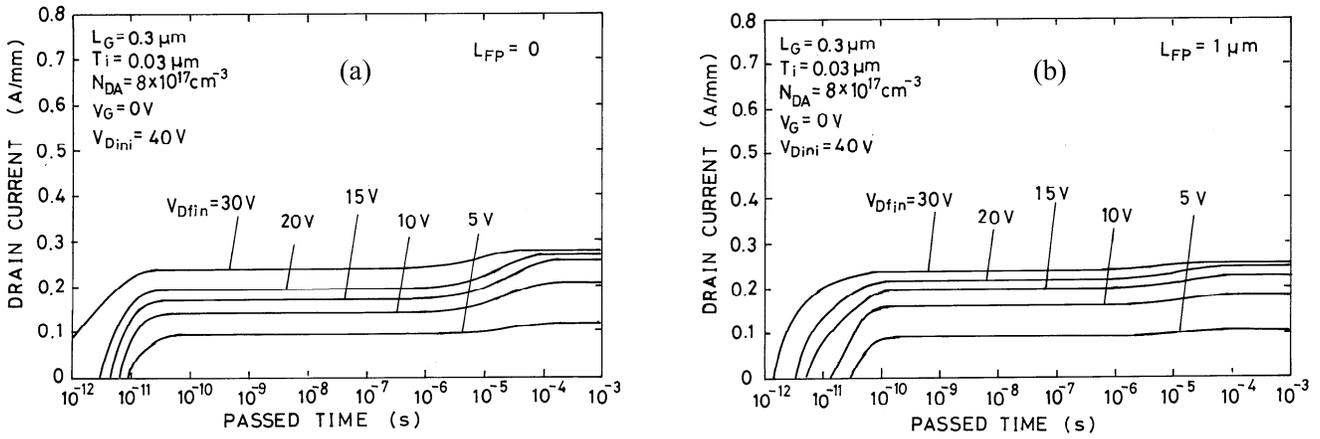

Fig. 3. Calculated drain-current responses of AlGaN/GaN HEMTs when $N_{DA} = 8 \times 10^{17}$ cm^{-3}. The rest is the same as in Fig. 2. (a) Without field plate ($L_{FP} = 0$), (b) with field plate ($L_{FP} = 1$ μm, $T_1 = 0.03$ μm).

band. Thus, in this work, we make analysis of lags and current collapse in field-plate AlGaN/GaN HEMTs with a buffer layer having only a deep acceptor located above the midgap. We have particularly studied the dependence on the deep-acceptor density in the buffer layer, where it is varied between 10^{17} cm^{-3} and 8×10^{17} cm^{-3} here. As a result, we have found that without a field plate, the drain lag and current collapse increase with increasing the deep-acceptor density as expected, but with a field plate, surprisingly, the drain lag, gate lag and current collapse decrease when the deep-acceptor density becomes high.

In Section II, we describe physical models used here, such as a device structure, a buffer-trap model, and basic equations for the analysis. In Section III, calculated slow current responses are discussed in terms of drain lag. An example of pulsed *I-V* curves and current collapse are described in Section IV. Then, in Section V, we describe the dependence of lags and current collapse on the deep-acceptor density in the buffer layer in terms of the field-plate length. In Section VI, their dependence on the deep-acceptor density in the buffer layer is described in terms of the insulator thickness under the field plate. Finally, the conclusion is given in Section VII.

II. PHYSICAL MODEL

Fig. 1 shows a device structure analyzed in this study. The gate length L_G and the gate-to-drain distance L_{GD} are 0.3 μm and 1.5 μm, respectively. The field-plate length L_{FP} is varied between 0 and 1 μm, but typically set to 1 μm. The SiN layer thickness T_i is also varied between 0.01 μm and 0.1 μm, but typically set to 0.03 μm. We set polarization charges of 10^{13} cm^{-2} at the heterojunction interface, and it is assumed that surface polarization charges are compensated by surface-state charges [12], [20]. As a buffer layer, we consider a Fe-doped semi-insulating buffer layer. The Fe level (E_{DA}) is set 0.5 eV below the bottom of conduction band, and it is considered to be a deep acceptor. The energy levels of around $E_C - E_{DA} = 0.5$ eV are reported in [26] and [30]. In this case, the deep acceptors act as electron traps. The deep-acceptor density in the buffer layer N_{DA} is varied between 10^{17} cm^{-3} and 8×10^{17} cm^{-3} here.

Basic equations to be solved are Poisson's equation, continuity equations for electrons and holes, and a rate equation for the deep acceptor [31], [32]. These are expressed as follows.

a) Poisson's equation

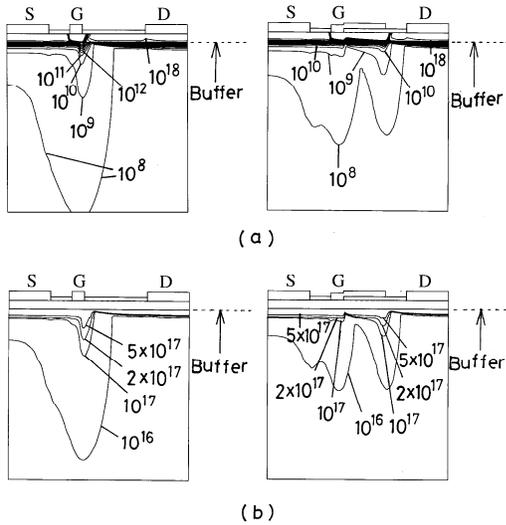$$\nabla \bullet (\varepsilon \nabla \psi) = -q\left(p - n + N_D - N_{DA}^-\right) \quad (1)$$

Fig. 4. (a) Electron density profiles and (b) ionized deep-acceptor density N_{DA}^{-} profiles at $V_D = 40$ V and $V_G = 0$ V. $N_{\mathrm{DA}} = 8 \times 10^{17} \mathrm{cm}^{-3}$ and $E_C - E_{\mathrm{DA}} = 0.5$ eV. The left shows the case without field plate, and the right shows the case with field plate ($L_{\mathrm{FP}} = 1$ µm, $T_1 = 0.03$ µm).

TABLE I
TRAP PARAMETERS OF DEEP ACCEPTOR USED IN THIS STUDY

Parameters	Values
energy level ($E_C - E_{\mathrm{DA}}$)	0.5 eV
capture cross section for electrons ($\sigma_{n,\mathrm{DA}}$)	10^{-13} cm^2
capture cross section for holes ($\sigma_{p,\mathrm{DA}}$)	10^{-15} cm^2

b) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \bullet J_n - R_{n,\mathrm{DA}} \qquad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \bullet J_p - R_{p,\mathrm{DA}} \qquad (3)$$

where

$$R_{n,\mathrm{DA}} = C_{n,\mathrm{DA}}\left(N_{\mathrm{DA}} - N_{\mathrm{DA}}^{-}\right)n - e_{n,\mathrm{DA}}N_{\mathrm{DA}}^{-} \qquad (4)$$

$$R_{p,\mathrm{DA}} = C_{p,\mathrm{DA}}N_{\mathrm{DA}}^{-}p - e_{p,\mathrm{DA}}\left(N_{\mathrm{DA}} - N_{\mathrm{DA}}^{-}\right) \qquad (5)$$

c) Rate equation for the deep acceptor

$$\frac{\partial N_{\mathrm{DA}}^{-}}{\partial t} = R_{n,\mathrm{DA}} - R_{p,\mathrm{DA}} \qquad (6)$$

where N_{DA}^{-} represents the ionized deep-acceptor density. $C_{n,\mathrm{DA}}$ and $C_{p,\mathrm{DA}}$ are the electron and hole capture coefficients of the deep acceptor, respectively, and $e_{n,\mathrm{DA}}$ and $e_{p,\mathrm{DA}}$ are the electron and hole emission rates of the deep acceptor, respectively. These capture coefficients and emission rates are expressed as functions of the deep-acceptor's energy level $E_C - E_{\mathrm{DA}}$ and electron and hole capture cross sections of the deep acceptor ($\sigma_{n,\mathrm{DA}}$, $\sigma_{p,\mathrm{DA}}$). These values are given in Table I. The above equations are put into discrete forms in two dimensions and solved numerically.

III. DRAIN LAG

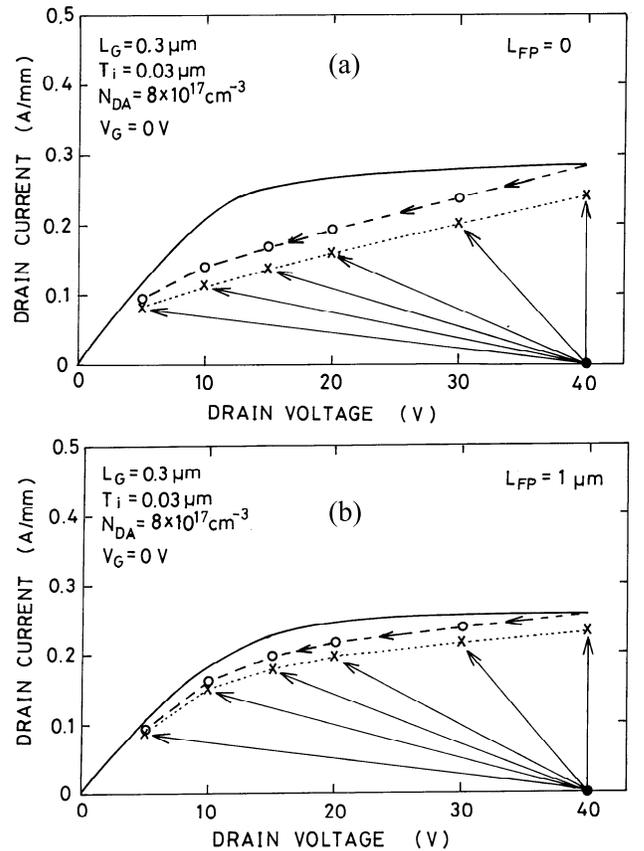Figs. 2 and 3 show calculated drain-current responses of AlGaN/GaN HEMTs with $N_{\mathrm{DA}} = 10^{17}$ cm^{-3} and

Fig. 5. Steady-state I_D-V_D curves (solid lines: $V_G = 0$ V) and quasi-pulsed I_D-V_D curves (x, ○) of AlGaN/GaN HEMTs. $N_{\mathrm{DA}} = 8 \times 10^{17}$ cm^{-3}. (a) Without field plate ($L_{\mathrm{FP}} = 0$), (b) with field plate ($L_{\mathrm{FP}} = 1$ µm, $T_1 = 0.03$ µm). (○): Only V_D is changed from 40V ($V_G = 0$ V), (x): V_D is changed from 40 V and V_G is changed from V_{th} to 0 V.

8×10^{17} cm^{-3}, respectively when the drain voltage V_D is changed abruptly from $V_{\mathrm{Din}} = 40$ V to the respective voltage V_{Dfin}. Here, the gate voltage V_G is not changed at 0 V. Figs. 2(a) and 3(a) show the cases without a field plate ($L_{\mathrm{FP}} = 0$), and Figs. 2(b) and 3(b) show the cases with a field plate ($L_{\mathrm{FP}} = 1$ µm). Here, the SiN layer's thickness T_i is 0.03 µm. In all cases, after the large negative displacement currents, the drain currents remain at lower values than the steady-state values for some periods ("quasi-steady state" [33]), and they begin to increase gradually, reaching the real steady-state values. This slow transient is called drain lag. At higher V_D, more electrons are captured by deep acceptors in the buffer layer and the buffer is more negatively charged. Therefore, even if V_D is lowered abruptly, the drain currents remain low until the deep acceptors respond and emit electrons. It is considered that the drain currents start to increase gradually when the deep acceptors begin to emit electrons. Comparing the cases with and without a field plate, the change rates of drain currents during the slow response seem to be smaller in the case with a field plate. This indicates that the drain lag is smaller in the field-plate structure. Comparing Fig. 2 and Fig. 3, the overall currents are rather smaller in the case of higher $N_{\mathrm{DA}}(8 \times 10^{17}$ cm$^{-3})$. This is because the ionized deep-acceptor densities around the channel-buffer interface are

Fig. 7. Conduction-band-edge energy profiles along the line from the center of gate electrode to the buffer layer, with N_{DA} as a parameter. $V_D = 0$ V and $V_G = 0$ V. $L_{FP} = 1$ μm and $T_i = 0.03$ μm. The energy barrier toward the buffer layer is steeper for higher N_{DA}.

Fig. 8. Comparison of electron density profiles between (a) $N_{DA} = 10^{17}$ cm^{-3} and (b) $N_{DA} = 8 \times 10^{17}$ cm^{-3} without field plate. The left shows the cases of ON state ($V_G = 0$ V, $V_D = 40$ V), and the right shows the cases of OFF state ($V_G = V_{th}$, $V_D = 40$ V).
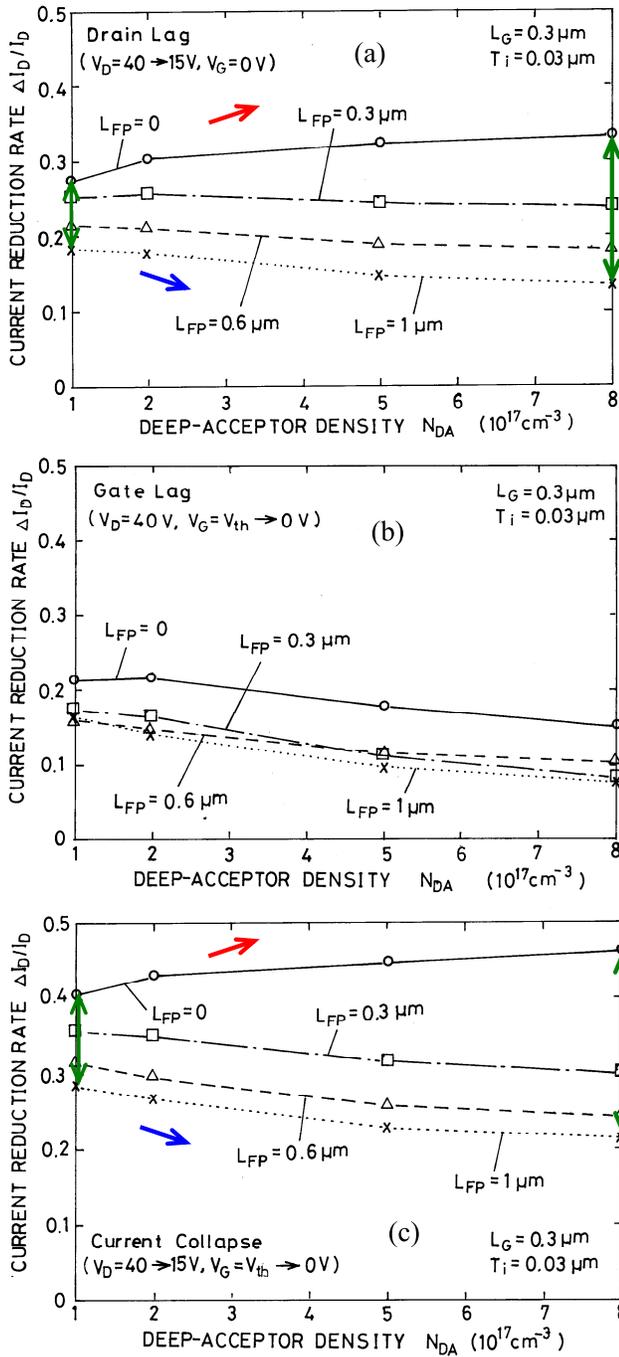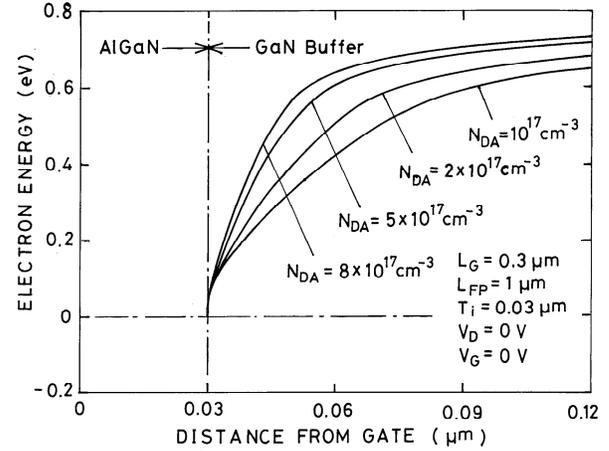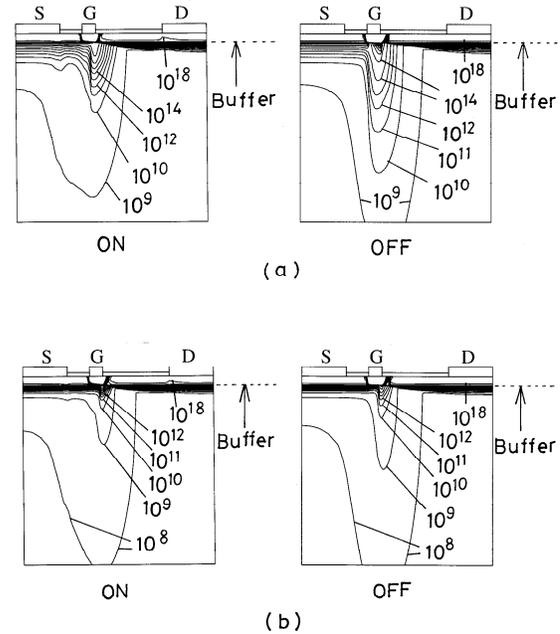
Fig. 6. Current reduction rate $\Delta I_D/I_D$ due to (a) drain lag, (b) gate lag and (c) current collapse as a function of the deep acceptor density in the buffer layer N_{DA}, with the field-plate length L_{FP} as a parameter. $T_i = 0.03$ μm.

higher and hence the electron energy at the channel-buffer interface is raised, leading to lower electron densities in the channel and lower buffer leakage current due to the steeper barrier. It is also seen that the reduction in drain lag by introducing a field plate seems to be more remarkable for higher N_{DA}, but this point will be described again in Section V. We describe below why the drain lag is smaller in the case of field-plate structure.

Fig. 4(a) shows a comparison of electron density profiles at $V_D = 40$ V and $V_G = 0$ V between the two cases without (left) and with (right) a field plate ($L_{FP} = 1$ μm). Here, N_{DA}

is 8×10^{17} cm^{-3}. Fig. 4(b) shows the corresponding ionized deep-acceptor density N_{DA}^- profiles. These figures represent a state before V_D is changed in Fig. 3. From Fig. 4(a), we see that in the case without a field plate, due to a stronger electric field at the drain edge of the gate, more electrons are injected deeper into the buffer layer under the gate region. These electrons are captured by the deep acceptors in the buffer layer. Therefore, as seen in Fig. 4(b), N_{DA}^- increases in the deeper region of the buffer layer under the gate. When V_D is lowered abruptly, the electron injection should become weaker, but the deep acceptors do not respond to the voltage change soon, and N_{DA}^- remains unchanged. Thus, the drain current remains
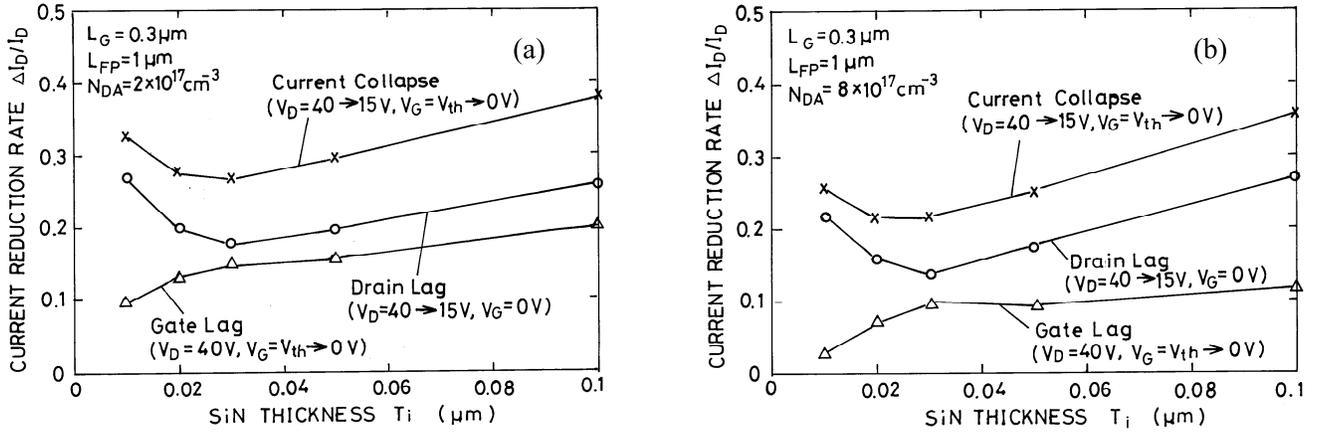
Fig. 9. Current reduction rate $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse as a function of the SiN thickness T_i. $L_{FP} = 1$ μm. (a) $N_{DA} = 2 \times 10^{17}$ cm^{-3}, (b) $N_{DA} = 8 \times 10^{17}$ cm^{-3}.

at a low value until the deep acceptors respond and begin to emit electrons. Therefore, the large drain lag arises. On the other hand, in the case with a field plate, due to a weaker electric field at the drain edge of the gate, the electron injection under the gate region is weaker, and hence the increase in N_{DA}^- under the gate region is smaller, as seen in Fig. 4(b). This indicates a smaller trapping effect in the field-plate structure. Here, it should be mentioned that with a field plate, electrons are also injected into the buffer layer under the field plate. But, the overall injection depth is not so deep and the increase in N_{DA}^- is not so significant. From these reasons, the drain lag becomes smaller in the field-plate structure.

IV. CURRENT COLLAPSE AND PULSED I-V CURVES

Next, we calculate the turn-on characteristics of AlGaN/GaN HEMTs when V_G is switched on. V_G is changed from the threshold voltage V_{th} to 0 V, and V_D is changed from 40 V to the on state drain voltage V_{Don}. V_{th} is defined here as a gate voltage when the drain current I_D becomes 0.5 mA/mm at $V_D = 40$ V. The obtained turn-on characteristics (not shown here) are similar to those in Fig. 2 and Fig. 3, showing the current collapse and gate lag behavior. The current collapse is a combined effect of drain lag and gate lag. Note that the gate lag exists because the slow transients arise when only the gate voltage is changed. From these turn on characteristics, quasi-pulsed I-V curves can be obtained as shown below.

Fig. 5 shows a comparison of calculated $I_D - V_D$ curves of AlGaN/GaN HEMTs between the two cases (a) without and (b) with a field plate ($L_{FP} = 1$ μm). Here, N_{DA} is 8×10^{17} cm^{-3}. The solid lines show the steady-state $I_D - V_D$ curves. The point (x) is the drain current taken at $t = 10^{-8}$ s in the turn-on characteristics for respective $V_D(V_{Don})$. These curves can be regarded as pulsed $I_D - V_D$ curves with pulse width of 10^{-8} s. The curves come significantly lower than the steady-state $I_D - V_D$ curves, particularly in the case without a field plate (Fig. 5(a)). This represents current collapse and gate lag behavior. The gate lag is indicated as the current reduction in pulsed $I_D - V_D$ curves at $V_D = 40$ V here, and

it is rather large [34]. In this figure, we also plot (○) which is taken at $t = 10^{-8}$ s from Fig. 3 for respective V_D, as is similar to (x). In Fig. 3, only V_D is changed, and hence these pulsed $I_D - V_D$ curves indicate the drain lag behavior. From Fig. 5, we can definitely say that the drain lag, gate lag and current collapse become smaller in the field-plate structure.

V. DEPENDENCE OF LAGS AND CURRENT COLLAPSE ON FIELD-PLATE LENGTH AND DEEP-ACCEPTOR DENSITY

We next study the dependence of lag phenomena and current collapse on the field-plate length L_{FP} and the deep-acceptor density in the buffer layer N_{DA}. Fig. 6 shows (a) the drain lag rate, (b) gate lag rate, and (c) current collapse rate as a function of N_{DA}, with L_{FP} as a parameter. Here the SiN thickness T_i is 0.03 μm. The rate is defined as a drain-current reduction rate $\Delta I_D/I_D$, where ΔI_D is the drain-current difference between the pulsed I_D-V_D curve and the steady-state I_D-V_D curve, and I_D is the steady-state drain current. The drain lag rate and current collapse rate are taken when V_D is changed from 40 to 15 V (see Fig. 5). It is seen that without a field plate ($L_{FP} = 0$), the drain lag and current collapse increase as N_{DA} increases, as expected, because the trapping effects should be more significant when the deep-acceptor density is higher (the deep acceptor act as electron traps). It is also seen that at a given N_{DA}, when L_{FP} becomes long, the drain lag and current collapse decrease. This is because by introducing a longer field plate, the electric field at the drain edge of the gate is more reduced [18], and hence electron injection into the buffer layer under the gate is more weakened, leading to less trapping effects as mentioned in Section III. This tendency is more pronounced when N_{DA} becomes higher (see green lines) [25], indicating that the field-plate effects are stronger for higher N_{DA}. Finally, it is clearly seen that with a field plate ($L_{FP} > 0$), the drain lag and current collapse decrease as N_{DA} increases, suggesting that the trapping effects are smaller for higher N_{DA} in the field-plate structures. This is a surprising result, because the deep acceptor should act as traps.

This behavior has not been experimentally verified because these types of experiments have not been ever reported to our knowledge. We hope this will be checked experimentally. This behavior can occur because as shown in Fig. 7, an energy barrier at the channel-buffer interface is steeper for higher N_{DA}, and hence electrons in the channel are not so diffused into the buffer layer, leading to less trapping effects in the field-plate structures. That is, the effects of field plate set on the device surface to reduce the drain lag and current collapse should become stronger when N_{DA} is higher. Therefore, the above result is attributed to the fact that the reduction in drain lag and current collapse by introducing a field plate becomes more significant when N_{DA} becomes higher (see green lines) [25]. This behavior is not so sensitive to the deep-acceptor's energy level between $E_C - E_{DA} = 0.5$ and 0.6 eV.

From Fig. 6(b), we also see that without a field plate ($L_{FP} = 0$), the gate lag slightly increases when N_{DA} increases from 10^{17} to 2×10^{17} cm^{-3}, but it clearly decreases when N_{DA} increases from 2×10^{17} cm^{-3} to 8×10^{17} cm^{-3}. In a previous work with an undoped semi-insulating buffer layer [34], the gate lag increases when a deep-acceptor density is changed from 10^{16} to 10^{17} cm^{-3}. So, the gate lag rate may take a peak around $N_{DA} = 2 \times 10^{17}$ cm^{-3}. We will discuss below why the gate lag decreases when N_{DA} becomes high. Fig. 8 shows a comparison of electron density profiles at (a) $N_{DA} = 10^{17}$ cm^{-3} and (b) $N_{DA} = 8 \times 10^{17}$ cm^{-3}. The left figures show the cases of ON state ($V_D = 40$ V, $V_G = 0$ V) and the right figures show the cases of OFF state ($V_D = 40$ V, $V_G = V_{th}$). From this figure, we see that in both cases ((a) and (b)), when V_G changes from 0 V to V_{th} (OFF state), electrons are injected into the buffer layer under the gate. But, the injection is less remarkable for higher N_{DA} (Fig. 8(b)), which should lead to less trapping effects. This may be due to the steeper barrier at the channel-buffer interface for higher N_{DA}. Therefore, the gate lag becomes smaller in the case of higher N_{DA}. From Fig. 6(b), we also see that with a field plate ($L_{FP} > 0$), the gate lag is reduced at a given N_{DA}. This is because the electric field at the drain edge of the gate is reduced, and electron injection into the buffer layer is suppressed. In addition, with a field plate, the gate lag decreases when N_{DA} increases, as in a case without a field plate. This may be due to the steeper barrier at the channel-buffer interface for higher N_{DA}, as mentioned before. Here, it should be noted that the gate lag in AlGaN/GaN HEMTs should occur mainly due to surface-state effects [3]. Therefore, to clarify the field-plate effects on surface-related gate lag is an important task yet to be done.
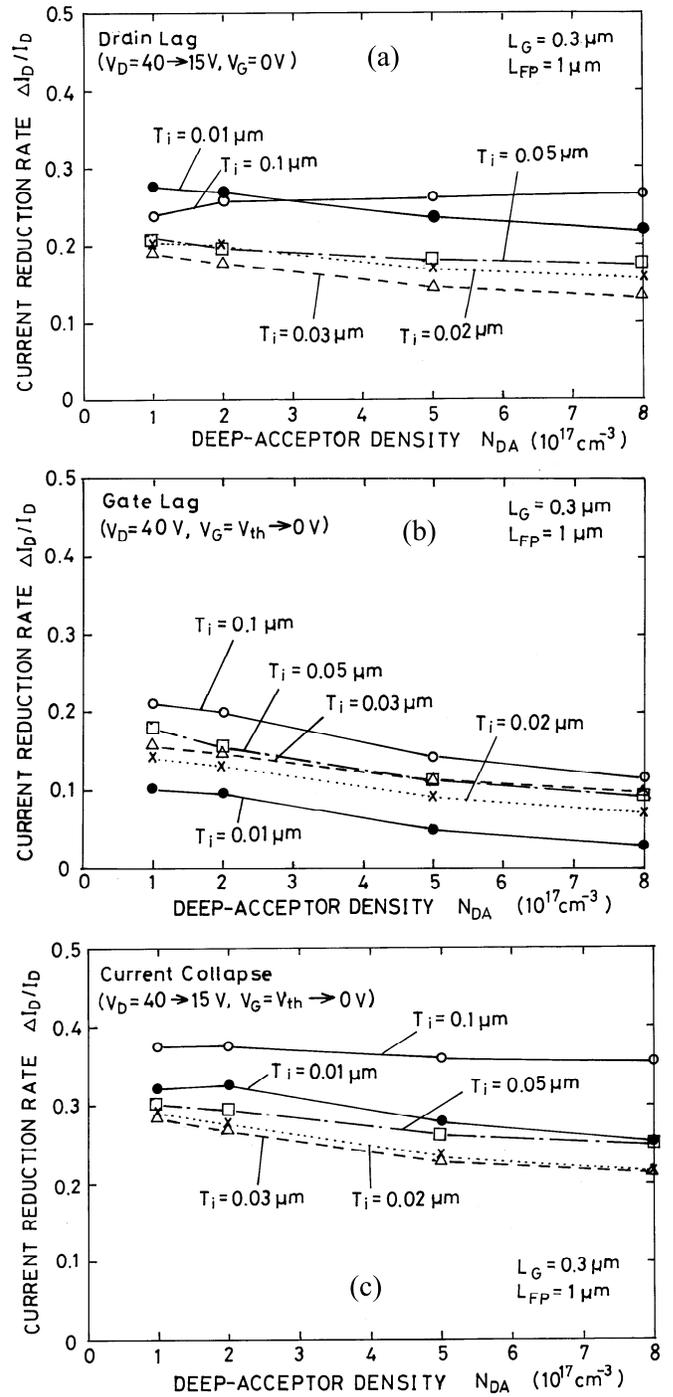

Fig. 10. Current reduction rate $\Delta I_D / I_D$ due to (a) drain lag, (b) gate lag and (c) current collapse as a function of the deep acceptor density in the buffer layer N_{DA}, with the SiN thickness T_i as a parameter. $L_{FP} = 1$ μm.

VI. DEPENDENCE OF LAGS AND CURRENT COLLAPSE ON SiN THICKNESS AND DEEP-ACCEPTOR DENSITY

We finally study the dependence of lag phenomena and current collapse on the SiN layer's thickness T_i and the deep-acceptor density in the buffer layer N_{DA}. Fig. 9 shows the current reduction rate $\Delta I_D / I_D$ due to drain lag, gate lag and current collapse as a function of T_i. Fig. 9(a) shows the case of $N_{DA} = 2 \times 10^{17}$ cm^{-3}, and Fig. 9(b) shows the case of $N_{DA} = 8 \times 10^{17}$ cm^{-3}. Here, $L_{FP} = 1$ μm. In both cases,

when T_i is relatively thick, the drain lag, gate lag and current collapse are relatively large. This is because the electric field at the drain edge of the gate remains relatively high and the field plate effects are weak. But, when T_i becomes thin, the lags and current collapse decrease. This occurs because the electric field at the drain edge of the gate is reduced, and the trapping effects become small, as described in Section III. However, the drain lag and current collapse increase when T_i becomes

very thin. This is because when T_i is very thin, the field plate becomes acting like a gate electrode, and hence the electric field at the drain edge of the field plate can be very strong. Then, electrons are injected deep into the buffer layer under the field-plate region, contributing to the drain lag and current collapse. Therefore, the U-shaped behavior arises, and the current collapse and drain lag take minimum values at $T_i = 0.03$ µm in these cases. These types of measurements also have not yet been reported. On the other hand, the gate lag becomes small when T_i becomes very thin. This is because the gate lag becomes small when the gate length becomes long [34]. From these two figures, we also see that generally, the lags and current collapse seem to be smaller in the case of higher N_{DA}.

Fig. 10 shows (a) drain lag rate, (b) gate lag rate, and (c) current collapse rate as a function of the deep-acceptor density in the buffer layer N_{DA}, with the SiN layer's thickness T_i as a parameter. The drain lag rate and current collapse rate are taken when V_D is changed from 40 V to 15 V. Here, $L_{FP} = 1$ µm. It is seen that when $T_i = 0.1$ µm, the drain lag increases as N_{DA} increases. This is because the field-plate effects are weak for thick T_i as mentioned before, and the current collapse remains high in this case. It is seen that the drain lag rate and current collapse rate take minimum values around $T_i = 0.03$ µm for all N_{DA} (the examples can be seen in Fig. 9 for the two values of N_{DA}). And the gate lag rate takes the smallest value when T_i is thinnest (0.01 µm) for all N_{DA}, because the effective gate length become long [34]. However, the most interesting point here is that the lags and current collapse generally decrease as N_{DA} increases in the range from 10^{17} to 8×10^{17} cm^{-3}, except for $T_i = 0.1$ µm. This is because the field-plate effects to reduce the lags and current collapse become stronger when N_{DA} becomes higher, as mentioned in Section V. That is, an energy barrier at the channel-buffer interface is steeper for higher N_{DA}, and electrons are not so diffused into the buffer layer, resulting in less trapping effects in the field-plate structures.

VII. Conclusion

A two-dimensional transient analysis of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer has been performed where relatively high densities ($1{\sim}8 \times 10^{17}$ cm^{-3}) of deep acceptor above the midgap are considered. It has been shown that the drain lag, gate lag and current collapse are reduced by introducing a field plate. This reduction occurs because electron trapping by the deep acceptors in the buffer layer is weakened by the field plate. It has also been shown that without a field plate, the drain lag and current collapse increase with increasing the deep-acceptor density as expected, although the gate lag decreases when the deep-acceptor density becomes higher than 2×10^{17} cm^{-3}. On the other hand, with a field plate, surprisingly, the lags and current collapse decrease when the deep-acceptor density becomes high. This is attributed to the fact that the reduction in drain lag and current collapse by introducing a field plate becomes more pronounced when the deep-acceptor density becomes higher [25]. In other words, this may be explained that when the deep-acceptor density is higher, electrons are not so diffused into the buffer due to the steeper barrier, and hence the effects of field-plate set on the device surface should become stronger.

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