Fast-Pulsed Characterization of RF GaN HEMTs in Lifetest Systems

Bruce M. Paine, *Member, IEEE*, Steve R. Polmanter, Vincent T. Ng, Neil T. Kubota, and Carl R. Ignacio

***Abstract*—We report a new application of microsecond-pulsed current–voltage characterization of field-effect transistor (FET) devices; namely, in compact, mutlichannel DC and RF lifetest systems. This application is important for routine monitoring of trap-related signature parameters in lifetests, and is particularly useful for study of GaN high electron mobility transistors (HEMTs) due to the wide variety of traps in the present generations of this technology. Also, we report a systematic approach to identifying the significant populations of traps, their general locations, and the qualitative changes that occur during lifetesting. This enables quick evaluation of device quality, likely degradation mechanisms and their signature parameters, and degradation rates—all with good statistics (up to 30 specimens simultaneously in one of our systems) and high reproducibility (± a few %). We use static I-V measurements as well, to separate the slow trap effects (longer than 10 min) from the fast ones (a few microseconds to about 1 min). We illustrate these techniques, with measurements of unstressed specimens of two GaN HEMT technologies. Evolution of the traps as the lifetests proceed will be described in a later paper.**

***Index Terms*—Gallium nitride, high electron mobility transistors (HEMT), characterization, trapping, pulsed I-V.**

I. Introduction

FAST-PULSED (microsecond) current-voltage (I-V) characterization is of particular interest for lifetest studies of GaN HEMTs because it can detect the effects of fast charge-traps, which cause degradation of RF power with aging [1], [2]. In earlier work [3], we have shown how to compare I-V curves measured with conventional or static I-V equipment, after different "pre-treatments" that fill or empty traps, and deduce a qualitative indication of *slow* trap densities (i.e., traps with time constants of 10 minutes or more). We now extend this technique to pulsed equipment, to get information on *fast* trap densities.

Another advantage of pulsed testing is the fact that self-heating is negligible [4], [5], so the characterizations can be done at a fixed channel temperature (T_{ch}), equal to the base temperature, unlike static testing where T_{ch} varies due to self-heating with the biases necessary to conduct the measurement. Also, for the same reason, pulsed testing allows measurements at high current densities (up to 1 A/mm), without risk of overstress. It is helpful to conduct such tests throughout a lifetest, because they provide:

1. An immediate picture of the quality of the semiconductor material in a device, after fabrication. This is particularly useful to evaluate its initial condition, and any traps that may have been left by the fabrication processes.

2. An early picture of how these trap distributions change with lifetest time, and how others may be added.

3. Quantitative signature parameters for monitoring trap-related degradation mechanisms. Two examples are (a) the change in pulsed threshold voltage (δV_{th}), which tracks electron trapping under the gate, resulting in reduced current flow, and (b) the change in drain resistance (δR_d), which tracks electron trapping in the gate-drain access region (G-D region), also causing reduced current flow. These are essential for determining the mean times to failure by these mechanisms. Also the measured thermal activation energy may help with identification of known atomic trap structures.

4. Means and standard deviations for the parameters above, over a large sample size (tens of specimens).

We have found that removing parts from the lifetest system to characterize them on the bench, sometimes causes parametric changes that are comparable with those occurring in the lifetest intervals. This is probably caused by small changes in plug-in connections, and waveguide connections (for mm-wave devices). Also, doing this for all specimens, at all intervals, in a long lifetest, is very time-consuming. Therefore *in-situ* testing is essential. However, pulsed I-V testing, *in-situ* in multi-channel lifetest systems (up to 30 channels) has not been reported before, most-likely because of two challenges: 1) there is usually minimal space in a lifetest rack, for an extra set of high-speed cables, and 2) bias circuitry for the test specimens usually incorporates large capacitors, which prevent high-speed characterization.

We have solved these challenges, in both DC and RF lifetest systems, and developed systematic techniques for getting qualitative information on trap densities, as well as their general locations in the FET – under the gate, or in the G-D region.

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B. M. Paine and N. T. Kubota are with the Technology Qualification Laboratory, Boeing Network and Space Systems, El Segundo, CA 90045 USA (e-mail: bruce.paine@boeing.com).

S. R. Polmanter is with Boeing Network and Space Systems, Kirtland Air Force Base, Albuquerque, NM 87117 USA.

V. T. Ng is with Boeing Network and Space Systems, El Segundo, CA 90045 USA, and also with the University of Southern California, Los Angeles, CA 90089 USA.

C. R. Ignacio is with Ecoleaders Inc., Quezon City 1104, Philippines.

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These are based on well-established principles [6], [7], but to our knowledge, a systematic approach to extract all the available information when several different trap phenomena are occurring, has not been reported before. We will report the use of this approach in actual lifetests, separately [8].

Traps in GaN HEMT have been monitored versus stress, by a variety of techniques including measurement of light response, gate-lag, drain lag, G_m dispersion, low-frequency noise measurement, and frequency-dependent capacitance and conductance (see [9]–[14]). Also, it has recently been shown that trap energies, densities, and approximate locations can be found for stressed HEMT devices, by transient-based deep level transient and optical spectroscopy's (DLTS/DLOS) [15], [16]. Similar analysis can be applied to capacitance- and conductance-based DLOS [17]. But all of these techniques require custom equipment (making *in-situ* measurement nearly impossible) and significant time, for example to measure time- and temperature-dependences. Therefore we regard these techniques as best suited for definitive identification of traps, in a small number of specimens, at the beginning and end of a lifetest. But for routine characterizations of the overall trap distributions in many specimens, at many intervals throughout a lifetest, the techniques that we describe, with static and fast-pulsed IV curves, are optimal.

The traps that we detect directly are those whose populations can be changed by simple "pre-treatments" before the I-V characterization. These were designed to produce "traps full" and "traps empty" states. They were generated with biases within the range of voltages covered in normal RF oscillations – that way we avoided populating traps that may not occur during normal operation. In addition, there are deeper traps (i.e., requiring more energy to de-populate) that can have a significant effect on RF operation. We measure *changes* in the densities of these traps, from characteristic changes in the I-V curves, with increased time on lifetest. We subdivide the traps in our study into "slow traps" with time constants of 10 minutes or more and "fast traps" with time constants between microseconds and 1 minute.

For static measurements [3], the pre-treatments were "traps empty" (E) which consisted of a bake at 150 °C for 60 min, and "traps full" (F) which consisted of holding a large gate-drain voltage for a few milliseconds. Of course *all* traps were not emptied or filled, but significant, and reproducible, numbers of slow traps were. For pulsed measurements, the pre-treatments were the quiescent biases we chose, which were applied by the test instrument throughout a measurement, except for microsecond pulsed excursions to measure the points of the I-V curves.

II. Parts, Equipment and Test Fixtures

Foundry 1 devices are designed for operation at V- and W-bands. The epitaxial material is grown by nitrogen plasma-enhanced (PE) MBE on SiC, giving a Ga-polar surface. The FETs have 150 μm gate periphery, and gate length of 0.15 μm. They have "mushroom" gates with minimal overhangs, compared to the gate length. The recommended drain operating bias is 12 V. The Foundry 2 parts are designed for operation at C-band. For these, the material is grown by MOCVD on SiC, presumably also giving a Ga-polar surface. We utilized FETs with nominal output powers of 2 W - they have total gate peripheries of 1.2 mm, and nominal gate lengths of 0.7 μm. They have a wide "mushroom" profile, with overhangs of about 0.5 μm. The recommended drain operating bias is 40 V.

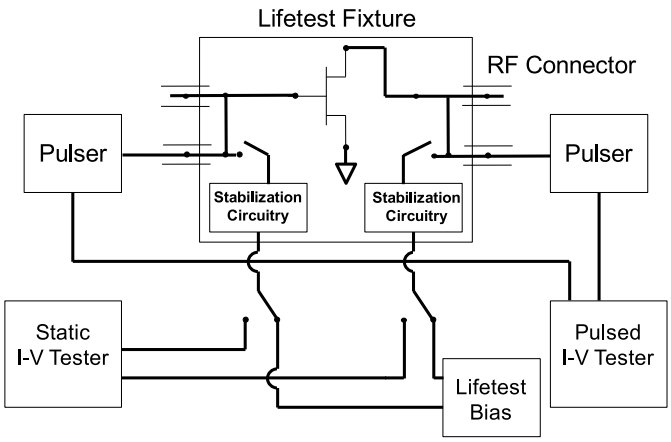

Fig. 1. Instrumentation for static and pulsed characterization of FETs in a lifetest fixture. Manual switches within the fixture allow disconnection of the stabilization circuitry and associated instruments, while pulsed testing is in progress. The pulsers are connected with coaxial cabling that is attached manually only for the pulsed tests. RF matching circuitry is not shown.

The DC lifetest system was from a commercial supplier. The RF lifetest systems were built in-house, designed for 62 and 4 GHz, for Foundries 1 and 2 respectively. Static I-V characterization was done with an HP 4142B Modular DC Source/Monitor for DC lifetests, and an Agilent B1500A Semiconductor Parameter Analyzer for RF lifetests. Pulsed characterization was done with an Auriga Microwave Model 4750, for all lifetests. All of the characterizations were *in-situ*, i.e., the fixture was not moved from the lifetest rack, and in darkness, since the lifetest fixtures were fully closed.

The fixtures in our RF lifetest systems were configured for pulsed testing, as shown in Figure 1. An extra pair of RF ports was constructed, to bring in the pulsed signals. For our DC lifetest system, the configuration was the same, except we used existing RF ports, since actual RF characterization was not needed. Switches (operated manually from outside the fixture) were added, to disconnect the FET from the normal bias lines, with their slow stabilization circuitry, and connect them to the fast pulsers for microsecond I-V measurements. (But the RF stabilization remained in the circuit.) The geometry of the switch elements ensured that they did not add significant parasitic impedances. The normal bias lines were switched outside the fixture, under program control, between the bias supplies for the lifetest, and the static I-V characterization equipment.

Coaxial cables from the pulsers were attached manually, to each fixture in turn, followed by operation of the switches. This was labor-intensive, but necessary to keep the density of cabling in the lifetest racks manageable. And the time (a few minutes) was much less than the time taken by the actual suite

of pulsed measurements (several hours). Each fast-pulsed measurement was repeated 64 times, to attain accuracy of a few percent because with the fast timing, the pulsed measurements are relatively noisy. On completion, the cables from the pulsers were removed, and the manual switches restored.

Our *in-situ* testing allowed the cables to be short (30 cm), and 50 Ω termination to be provided in the stabilization circuit, immediately adjacent to the device. This avoids possible problems with impedance mis-matches that require sophisticated measures [18]. For all pulsed tests V_g and V_d go on and off simultaneously, the pulse length was 4 μs, and the pulse period was 4 ms. Transients after the leading edge of a pulse settled in < 0.5 μs, and sampling was done over a 0.25 μs window centered 3.0 μs after the leading edge. The reproducibility of currents through the manual switches was ± 2 %; reproducibility of the I-V curves was ± 3 % with no identifiable trends with time. Checks were made for changes caused by self-heating at the highest pulse powers, and they were found to be negligible.

III. Procedures

A. Static I-V Curves

The timing of stress, pre-treatments and static characterizations is shown schematically in Figure 2(a). After the lifetest stress was turned off for all specimens simultaneously, there was an interval of up to 10 hrs, before the pre-treatments and static DC characterizations were conducted. This is due to the large quantity of specimens, and the need to measure them sequentially. As a result, some of the traps populated by the stress may have de-populated, so we designed the pre-treatments to reverse these. We did not attempt to run the static I-V curves immediately (say after a few milliseconds) after the pre-treatment because it is difficult to program conventional I-V systems in this manner. Instead, the pre-treatment was applied once, and a sequence of three static I-V's were measured within a few minutes – quick enough to preserve the traps with time constants of 10 minutes or more (Fig. 2(b)). The voltages during the characterizations were limited carefully to avoid changing slow trap populations significantly. This was established by trial-and-error, with repeated checks of the reproducibility of the curves – any loss was an indication of a change of slow traps caused by the characterization itself [3]. We now give the details of the measurements for Foundry 1. For Foundry 2, they are exactly analogous, with V_d increased and V_g decreased to cover the wider voltage swings of the lower-frequency devices.

The pre-treatments for static measurements were (in this order):

E. "Traps empty": (V_g, V_d, T_b) = (0 V, 0 V, 150 °C) for 60 min, up to several hours.

F. "Traps full": (V_g, V_d, T_b) = (V_g, 10, 50), with V_g stair-stepped from +1 to -4 V.

After each one of these, the following static I-V curves were measured, in this order, in immediate succession, with the base held at 50 °C.

1. Drain I-V curve with $V_g = 0$ V only, V_d millisecond pulsed from 0 to 3 V only.

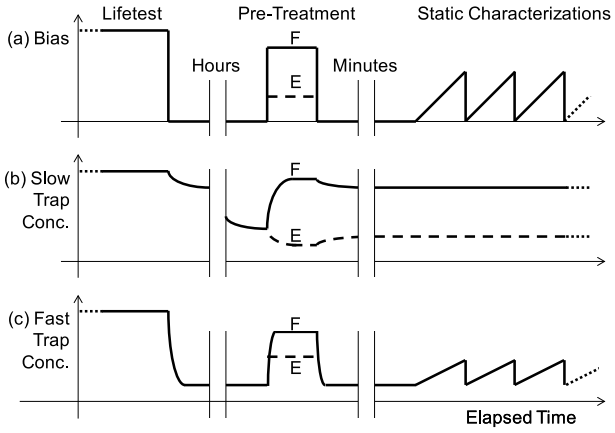

Fig. 2. Schematic time lines for static DC characterization. The pre-treatment is applied just once, before the characterizations are begun.

2. Standard transfer curve with $V_d = 10$ V, and V_g millisecond pulsed, from +1 to −4 V. (This is similar to the "traps full" pre-treatment, but is conducted with millisecond pulsing, instead of stair-step mode. This minimizes any changes to the trap populations.)

3. Low-voltage transfer curve with $V_d = 1.0$ V, and V_g millisecond pulsed from −4 to +3 V.

4. Forward gate I-V curve with $V_d = 0$, V_g stair-stepped from +3 V to 0 V. (Done after "Traps Full" pre-treatment only. Results are the same for either pre-treatment because starting with $V_g = +3$ V is an effective pre-treatment itself.)

Parameters extracted from these were labelled X_f, or X_e for pre-treatments F and E respectively. A key parameter that is found from the transfer curve is the threshold voltage (V_{th}), defined as $V_{peak} - I_{peak}/G_{mp}$, where V_{peak} and I_{peak} are the V_g and I_d corresponding the maximum of the transconductance, G_m.

The slow and fast traps' reactions to this sequence of biases during static I-V testing are illustrated schematically in Figs. 2(b) and (c). During the minutes-long interval between the pre-treatment and the characterization, the slow traps stay close to where they were left by the pre-treatment, while all the fast traps relax to the zero-bias equilibrium, which is independent of the pre-treatment. Then during static characterization electric charges in slow traps contribute to a different electric field distribution, depending on whether the pre-treatment was traps-full or traps-empty. Thus the difference between the two gives an indication of the density of slow traps. But the fast traps respond rapidly to the applied voltages in the same fashion, whether the pre-treatment was traps-full or traps-empty, so we do not detect them in the differences.

B. Pulsed I-V Curves

These tests were conducted up to 10 days after completion of the static measurements. (Unlike for the static measurements, these required operator actions.) The sequence is shown schematically in Figure 3(a). In pulsed testing, the analog of the pre-treatments described so far is the quiescent bias: it is applied continually, with only several-microsecond departures

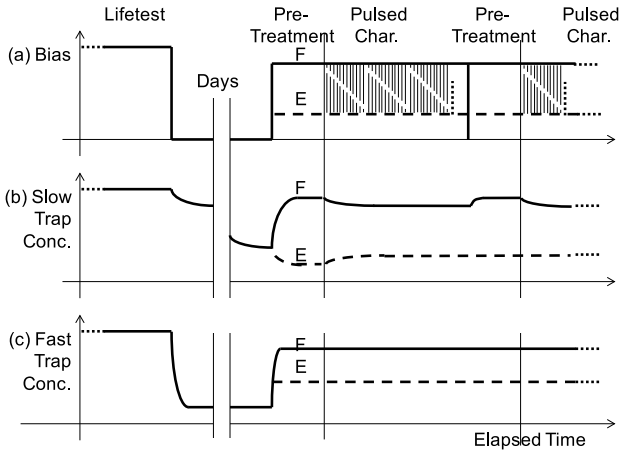

Fig. 3. Schematic time lines for pulsed DC characterization. The pre-treatment is applied before each of the three IV curves.

to points on the I-V curve, which return again. A channel temperature of 150 °C was chosen for the pulsed measurements because this is a typical temperature in normal operation. The base temperatures, necessary to give this channel temperature during quiescent bias, were calculated from the net power deposited in the device channels, with our thermal models [19].

The quiescent points for pulsed measurements were (in this order):

E. "Traps empty": hold Quiescent Point (V_g, V_d, T_{ch}) = (0, 0, 150) for 60 min, up to several hours.

F. "Traps full": hold Quiescent Point (V_g, V_d, T_{ch}) = (−4, 15, 150) for 40 s.

By pulsing from each one of these quiescent points, the following curves were recorded, in this order, in immediate succession.

1. Drain I-V curve with V_d swept from 0 to 10 V, V_g stepped from −4 to +1 in 0.25 V steps.

2. Standard transfer curve with V_d = 10 V, and V_g swept from −4 to +3 V.

3. Low-voltage transfer curve with V_d = 1.0 V, and V_g swept from −4 to +3 V. (For efficiency, since V_d is so small, we recorded I_g as well as I_d, and used this as our pulsed "forward gate I-V curve" as well. This makes the measured gate turn-on voltages (V_{gon}) a little higher than reality.)

Parameters extracted from the pulsed curves are labelled Y_{fp}, and Y_{ep}, for pre-treatments F, and E respectively.

The slow and fast traps' reactions to this sequence of biases during pulsed I-V testing are shown schematically in Figs. 3(b) and (c). Again, slow traps stay close to where they were left by the pre-treatment, but now the fast traps do the same. So the characterization senses the net effect of the slow and fast traps.

IV. Interpretation, Trap Densities and Examples

We now interpret the differences between I-V curves in terms of trap populations, based on well-established principles for GaAs devices [6], [7]. This is done in terms of electrons only, but this should be taken to mean also possible converse effects for holes. The differences are between trap densities

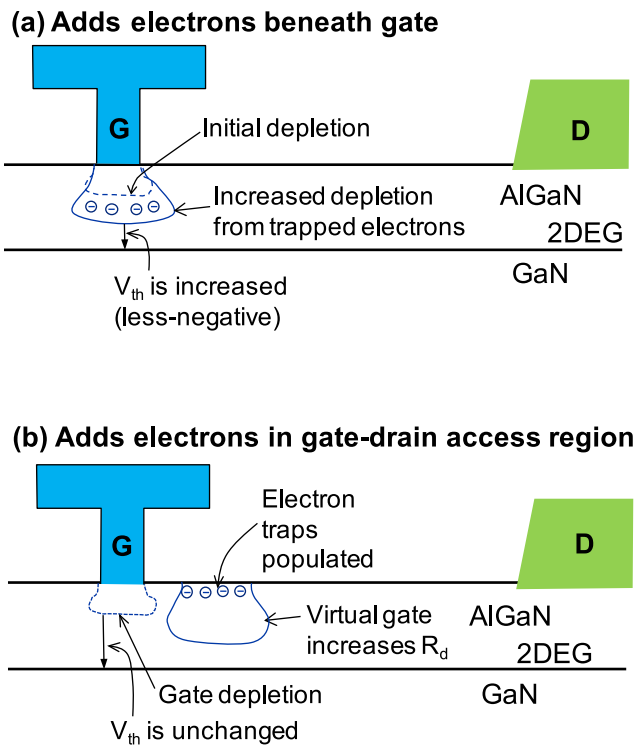

Fig. 4. Schematic diagrams showing possible effects of "traps full" treatment. (a) Electrons populate traps beneath the gate, increasing V_{th}. (b) Electrons populate traps in the gate-drain access region, increasing R_d.

that can be changed by our treatments – a background of deep traps may be present, but we are not sensitive to them, unless their populations are changed by external stresses, such as during wearout [8]. We refer only to the transfer curves, described above; some examples are shown in Fig. 7.

A. Summary of Interpretations

1. The "traps full" pre-treatment can populate traps under the gate or in the gate-drain access region (or both), as illustrated in Fig. 4. The "traps empty" pre-treatment can de-populate any of these traps.

2. At V_g's from V_{po}, i.e., V_g for I_g < 1 mA/mm, to V_{peak}, i.e., V_g where G_m reaches its maximum, changes in the transfer curves are most sensitive to the changes in the populations of traps under the gate [6], as illustrated in Fig. 5 (a). This is because at low V_g's (large negative) the FET is nearly pinched off and current is regulated mostly by depletion under the gate. Meanwhile, traps in the gate-drain access region will increase the drain resistance (R_d), and reduce the maximum current (I_{dmax}) but this does not affect I_d at low V_g's. This can be seen from electrical considerations [15], the physical picture (Fig. 5(a)), from typical drain I-V curves [20], and from experiment [16]. We choose V_{peak} as the dividing line because we calculate threshold voltage, which characterizes the lower part of the curve, by extrapolating from this point.

a. The V_{th}'s for the F curves are at higher (less-negative) V_g's, than for the E curves.

b. The difference between the V_{th}'s for static E and F curves (V_{thdiff} = V_{thf} - V_{the}) indicates population of slow traps under the gate.

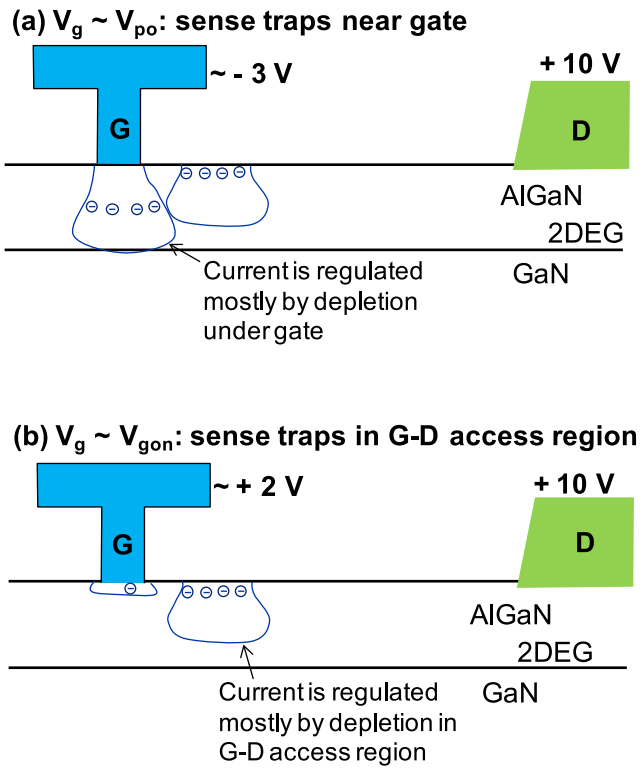

Fig. 5. Illustration of how the transfer curve is sensitive to traps at different locations, depending on V_g.

c. The difference between the V_{th}'s for pulsed E and F curves ($V_{thdiffp} = V_{thfp}$ - V_{thep}) indicates population of slow *and* fast traps under the gate.

d. Approximate quantitative trap densities can be found from the V_{th} differences, as described later.

e. Comparing static and pulsed curves is less useful because the static curves will mostly be measured at different channel temperatures, due to self-heating. Also, the pre-treatments are not exactly equivalent.

3. At higher V_g's, from about V_{peak} to V_{gon} (where forward conduction in the gate begins), the transfer curve is most sensitive to the population of traps in the gate-drain access region [7], as illustrated in Fig. 5(b). This is because at higher V_g's depletion under the gate is reduced and the FET current can become regulated by depletion in the G-D access region instead [13].

a. The F curves tend to "roll over" to even higher (less-negative) V_g's, relative to the E curves. This is also evident as reduced gradient (i.e., reduced G_m) [13], [21].

b. Further voltage difference between static E and F curves indicates population of slow traps in the gate-drain access region.

c. Further voltage difference between pulsed E and F curves indicates population of slow *and* fast traps in the gate-drain access region.

d. While standard transfer curves are convenient for observing the qualitative changes, it is difficult to extract quantitative trap densities from them. Rather it is more accurate to use changes in the drain resistance (δ R_d), extracted from the linear regions of the drain I-V curves, as will be described later. However it is not easy to observe these quickly, in standard plots of these curves.

We note that some researchers use the G_m curves (i.e., dI_d/dV_g) in an analogous way to what we have described [21]. We prefer the raw I_d curves because they are less noisy, and it is easy to see where current compression begins (if V_d is above the knee voltage), causing saturation of the transfer curves.

B. Trap Densities

We made rough estimates of trap densities by means of the analysis developed at Ohio State University [15], [16], [22], [23]. That analysis was used for gate-controlled and drain-controlled constant-I_d DLTS and DLOS measurements of turn-on transients from "traps full" to "measurement" states. The parameters δ V_{th} and δ R_d that they find from transient measurements can just as well be measured with our pulsed I-V techniques. But unlike the DLTS and DLOS techniques, we have very little timing information, so we cannot extract information about trap energy levels. Therefore we must assume that a single trap species is responsible for the observed changes, which puts uncertainties of perhaps 10x on the absolute results. (But relative results should be accurate to around $\pm$ 20 %.) δ V_{th} is measured as described above; extraction of δ R_d will be described below.

1. Trap concentration under the gate is deduced from δ V_{th}, with constant I_d (zero in our case), maintained by adjusting V_g (to V_{th} in our case). This is measured with V_d in the saturated regime, to ensure that changes of R_d, which would shift V_d, do not have a significant effect on the current. We assume all the traps are in the AlGaN layer. Then the surface density of traps is

$$n_T = \frac{-2\varepsilon_o \varepsilon_{AlGaN} \delta V_{th}}{q t_{AlGaN}} \tag{1}$$

where ε_o is the permittivity of free space (8.854 x 10^{-14} F/cm), ε_{AlGaN} is the dielectric constant of AlGaN (8.9), q is the elemental electric charge (1.602 x 10^{-19} C) and t_{AlGaN} is the thickness of the AlGaN layer. An analogous formula would apply for traps in another layer.

2. Trap concentration in the drain access region is deduced from δ R_d, the change in R_d after switching from "traps full" to "traps empty", again with constant drain current, I_d^o, but now maintained by adjusting V_d. This is measured in the linear regime of the drain I-V curves, where resistance change *is* reflected by a voltage change, but at low current (I_d^o < 300 mA/mm), to ensure minimal contributions from changes in the source resistance. Now

$$n_T = (n_s)^2 \left[n_s - \frac{L_{dep,max}}{q \mu_n \delta R_d} \right]^{-1} \tag{2}$$

where n_s is the sheet density of charge in the 2-dimensional electron gas (2DEG) (typically around 1 x 10^{13} cm^{-2}), $L_{dep,max}$ is the maximum laterally depleted region associated with the fill pulse (estimated to be 0.15 μm for devices studied by Ohio State University [22]), and μ_n is electron mobility in the 2DEG (typically 1800 cm^2/V.s). For the measurement, I_d^o and V_g^o are chosen to ensure the current stays in the

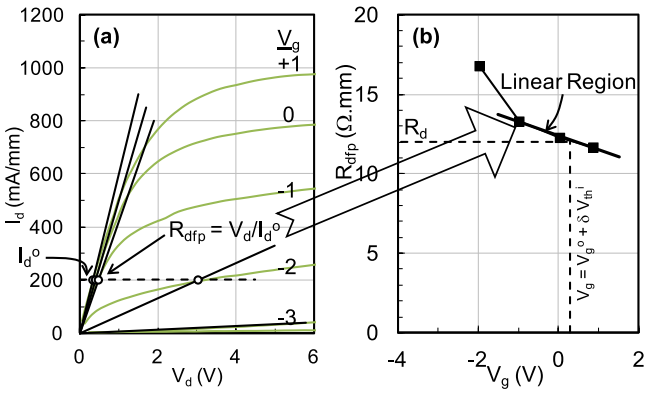

Fig. 6. Illustration of extraction of R_d. Gradients are found between the origin and a chosen I_d^o (< 300 mA/mm, but in the linear regime for the V_g's of interest). R_{dfp} is R_d measured from "traps full" pulsed I-V curves.

linear regime. But after the first measurement, corrections should be made at each interval i for the threshold voltage shift at that interval, by using $V_g^i = V_g^o + \delta V_{th}^i$. The measurement is most-easily done by recording a set of drain I-V curves, with V_g ranging from pinch-off to +1 V, and plotting R_d (i.e., the inverse of the gradients of the curves, read from the origin to I_d^o) versus V_g, as illustrated in Fig. 6. Then R_d can be read off at $V_g^o + \delta V_{th}^i$. This R_d increase, caused by stress, is often termed "knee walk-out" because the onset of saturation moves to higher V_d. Finally we note that this quantitative method is similar (but not identical) to the easily-observed qualitative method described earlier (applied at low V_d): the former measures V_d for given I_d^o (chosen in the linear I_d-V_d regime) and V_g^o (adjusted for V_{th} changes): the latter measures V_g (the transfer curve "roll-over") for given I_d^o and V_d^o (both chosen in the linear I_d-V_d regime).

It is important to note that the precise locations of the traps that are detected depend strongly on the device geometry, trap type, and pre-treatments adopted for "traps full" and "traps empty" characterizations. Therefore the sampling of traps "under the gate" in one study may be different from the sampling taken "under the gate" in another one, and only order-of-magnitude differences between studies are likely to be significant. However, small changes observed in the same technology, with the same pre-treatments are likely to be significant.

Also, it is straightforward to relate these signature parameters (δV_{th} and δR_{th}) *accurately* to loss of power, or gain in a FET [24]. Therefore the measurements that we describe are very important for tracking small changes in trap-related phenomena in lifetests [25].

C. Example – Foundry 1

Fig. 7(a) shows transfer curves measured on a specimen from Foundry 1, by both static and pulsed systems, with both "traps full" and "traps empty" treatments. The inset displays our conclusions – the numbers are our estimates of the areal densities of traps, in units of 10^{12} traps/cm^2. Peak G_m is at $V_g \sim -2.0$ V. First we consider the populations of traps under the gates, i.e., V_g from −4 to −2 V. The static measurements after

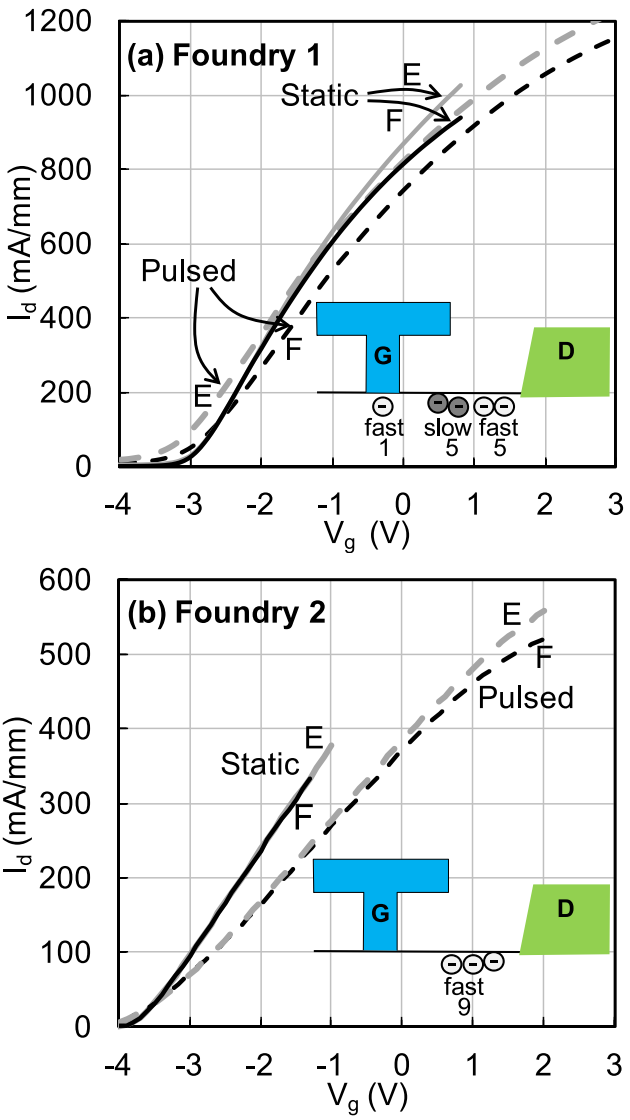

Fig. 7. Examples of transfer curves. Static measurements are indicated with continuous curves; pulsed measurements are indicated with dashed curves. After "traps empty" treatment: gray curves; after "traps full" treatment: black curves. The insets show schematically the trap speeds, locations, and approximate areal densities in units of 10^{12} traps/cm^2, all deduced from the transfer curves. Note that since uncertainties in the absolute densities are large ($\sim \pm 10$x), their differences between the two foundries are not significant.

the two treatments are nearly identical, indicating negligible population of slow traps under the gate. But the pulsed measurements after the two treatments show 255 mV separation, indicating significant combined population of fast and slow traps under the gate. We therefore conclude there is a significant population of fast traps only, under the gate. From Formula (1), assuming the traps are in the AlGaN layer, we find their density is 1 x 10^{12} traps/cm^2, with an uncertainty of ±10x. This is probably significantly higher than the ∼1 x 10^{10} traps/cm^2 reported from a DLTS/DLOS study of PE MBE material from another source [16].

For V_g from −2.0 V to V_{gon}, the F static curve diverges to higher V_g, indicating that there are some slow traps in the G-D region. To estimate their density, we found the corresponding δR_d; it was −0.036 W.mm. $L_{dep,max}$ was estimated

to be 0.1 μm, and we used the typical values for μ_n and n_s quoted above. Then Eqn. 2 gave approximately 5 x 10^{12} slow traps/cm^2, in the G-D region. We believe this is the first time that quantitative densities of > 10 minute time-constant traps has been obtained for GaN HEMTs. Meanwhile the pulsed curves moved further apart slightly, indicating traps (slow and fast, summed) in the G-D access region, with a density that is probably greater than the density of slow traps alone, in that region. Therefore we conclude there is also a significant population of fast traps in the G-D region. To find its density, we found δ R_d and after correcting for the V_{th} shift (as described above and in Fig. 6); it was –1.531 Ω.mm. After subtracting the slow trap density, we deduced approximately 5 x 10^{12} fast traps/cm^2, in the G-D region. This appears to be consistent with a separate DLTS/DLOS study of the PE MBE material mentioned above, after allowing for multi-defect interactions [26].

D. Example – Foundry 2

Fig. 7(b) shows transfer curves measured on a specimen from Foundry 2. Peak G_m's occurred at approximately −1 V. Since this FET had a dense array of gates, we had to limit the static measurements to below 360 mA/mm to avoid significant heating. But we looked at the static R_d data and found there is no separation, up to $V_g = +1$ V.

The E and F V_{th}'s are equal to < 10 mV, for both static and pulsed measurement, so with the assumptions above, the trap densities (both slow and fast) are < 1 x 10^{10} traps/cm^2, which is consistent with other reports on MOCVD devices [15].

The only visible divergence of F and E curves is between the pulsed curves, for $V_g > V_g$(peak G_m). This indicates a significant population of fast traps in the drain access region, and minimal trap population under the gate. To estimate the quantitative density in the G-D region, we found δ R_d was −1.285 Ω.mm. No correction was needed for threshold voltage changes. $L_{dep,max}$ was estimated to be 0.35 μm, in modelling by the foundry, and we used the typical values for μ_n and n_s quoted above. Then Eqn. 2 gave approximately 9 x 10^{12} traps/cm^2, in the drain access region, again with an uncertainty of ±10x. This is certainly consistent with about 5 x 10^{12} traps/ cm^2, reported for two other industrial suppliers of MOCVD-grown GaN/AlGaN HEMTs [27].

V. Conclusion

We have incorporated microsecond-pulsed I-V characterization in DC and RF lifetest racks, and developed sequences for "traps full" and "traps empty" characterizations, that (in conjunction with static I-V characterizations) allow us to deduce qualitative densities of fast and slow traps in different locations within GaN HEMT devices. Compared to more-quantitative spectroscopic measures of trap characteristics, this approach is quick and covers large quantities of specimens throughout a lifetest. Thus one can have an immediate picture of the quality of the semiconductor material after device fabrication, and also rapidly develop a picture of trap growth in all specimens, as a lifetest proceeds. At the same time, these characterizations yield accurate *quantitative* measures of signature parameters for trap-related degradation mechanisms, that are essential for predicting mean times to failure.

In the two GaN HEMT technologies that we used to demonstrate our approach, we observed rather different trap distributions, most likely due to different material parameters and gate configurations. We quantified the slow traps, which we believe has not been done before. We also quantified the fast traps, and found some consistency with other such measurements in the literature, for each of the epitaxial material types. These observations suggest that the technique is applicable GaN HEMT technologies with a wide variety of trap configurations, and yields trap concentrations that are probably accurate to within an order of magnitude. However it's best application will be to measuring *changes* in a given technology (eg. in a lifetest), rather than finding absolute figures.

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Bruce M. Paine (M'80) received the B.Sc. (Hons.) and Ph.D. degrees in physics from the University of Melbourne, Melbourne, Australia, in 1975 and 1979, respectively.

He was with the California Institute of Technology, for six years, finishing as a Senior Research Fellow, working on materials science. He was with Hughes Aircraft Company, researching GaAs and InP monolithic microwave integrated-circuit process development. Since 1993, he has been with the Boeing (formerly Hughes) Satellite Division, El Segundo, CA, USA. There he initiated (and still leads) the Technology Qualification Group, to qualify new solid state technologies for high-reliability applications, and assist with their transfer to production. Their research activities are mostly lifetesting, environmental testing (including radiation and hydrogen), device characterization, and physical analyses.

Dr. Paine has more than 70 publications, including six invited articles and one book chapter.

Steve R. Polmanter received the B.S. degree in optical engineering from the University of Houston, Houston, TX, USA, in 1991.

Since 2003, he has been with the Boeing Co., developing electro-optical systems and lasers. His current research interests include adaptive optics and high speed data acquisition systems.

Vincent T. Ng received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, USA.

His work has been in the area of analog and mixed analog–digital integrated-circuit design, analysis, and characterization. He also teaches undergraduate and graduate electrical engineering courses with the University of Southern California.

Neil T. Kubota received the B.S. degree in electrical engineering from California State University, Long Beach, CA, USA, in 1992.

He was with Hughes Aircraft Corporation GaAs Operations, Torrance, CA, USA, where he was responsible for reliability analysis of GaAs devices for radar and space applications. Since 1998, he has been with Boeing Network and Space Systems, El Segundo, CA, USA, where he is involved with the reliability analysis of GaN, SiGe, and InP devices and laser diodes for space applications.

Carl R. Ignacio received the B.S. degree in electrical engineering from California State University, Long Beach, CA, USA, and the M.S. degree in electrical engineering with an emphasis on microwave networks and devices from the University of Southern California, Los Angeles, CA, USA.

He has been involved in the design and development of various analog and digital satellite communication hardware elements and specializes in the use of RF circuit and system modeling tools in design and worst case analysis. He has also been involved in GaN reliability testing and analysis and (separately) the development of a major digital satellite communications product line.