A DLTS Study on Deep Trench Processing-Induced Trap States in Silicon Photodiodes

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***Abstract*—We present a Deep Level Transient Spectroscopy (DLTS) study on dedicated test samples to investigate the defect landscape of deep trench (DT) sidewalls. The DT is commonly used to prevent crosstalk between two neighboring optoelectronic devices or as a separator between different functional blocks on a monolithic semiconductor chip. However, in minority carrier-based optoelectronic devices, such as photodiodes, carriers might recombine at trap states located at the DT to silicon interface causing performance degradation. The extracted parameters of the DLTS study are further utilized to investigate this recombination in terms of TCAD simulations. The results suggest that carrier recombination at the DT sidewalls of DT-terminated photodiodes may lead to non-linear responsivities with respect to the optical radiant flux. Furthermore, on the example of silicon dangling bonds, we investigate the influence of structural relaxations at the defect sites which are incorporated in the nonradiative multiphonon (NMP) model. By a comparison between the NMP model to the conventional Shockley-Read-Hall (SRH) model we show, that a difference in the emission barrier of approx. 50 meV will arise, resulting in a strong shift of the corresponding DLTS transients.**

***Index Terms*—Deep trench isolation, photodiode, interface recombination, responsivity, linearity.**

I. Introduction

In RECENT decades, considerable attention has been devoted to the investigation of trap states at the Si/SiO_2 interfaces of integrated devices. The defect landscape, crucial to understanding the impact of such trap states, is known to be intricately linked to the details of oxide processing and annealing. In this study, we investigate the silicon-to-oxide interface of deep trenches (DTs) with an aspect ratio (width-to-depth ratio) of approximately ten. Such trenches are used as guard rings for photodiodes or to separate different blocks of circuitry and devices on a semiconductor chip. The processing of these grooves is inherently challenging often resulting in elevated trap densities and high amounts of fixed oxide charges which may cause intensity-dependent recombination phenomena [1]. Our investigations hold particular relevance in the realm of photodetectors and image sensors, where the emergence of interface problems has presented significant challenges. Addressing these challenges is pivotal as the interaction of charge carriers with trap states significantly influences the performance and reliability of integrated devices. Therefore, different techniques and strategies have evolved to passivate the interface and minimize losses due to recombination [2]. To gain further insides into the vertical Si/SiO_2 interface associated with the sidewalls of deep trenches we characterize the defects employing Deep Level Transient Spectroscopy (DLTS).

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II. Experimental

A. Test Structures and Setup

For the DLTS study, dedicated test structures were processed in a conventional 180 nm process with a DTI processing option. The test structures consist of alternating n-well and p-well regions separated by DTs fabricated on a 20 µm thick p-doped epitaxial layer grown on a p+ substrate. A schematic of the test structure is shown in Fig. 1. The deep reactive ion etching technique is used to fabricate the grooves for the DTI. After the DTI etching, a Boron sidewall implant with a peak doping concentration of $\approx 4 \times 10^{16}\,\mathrm{cm}^{-3}$ is performed and a 140 nm oxide is grown by a two-step oxidation process (40 nm dry oxidation followed by 100 nm TEOS deposition). Finally, the trenches are filled with undoped poly-silicon. More details about the DTI processing are shown elsewhere [3].

In a typical DLTS measurement sequence trap states are filled by applying a pulsed filling voltage to a pn-junction. Then, a quiescent reverse bias is applied and the trap-carrier dynamics are monitored by measuring a transient capacitance. To get a strong impact from trap states located at the DTI Si/SiO_2 interface on the measured DLTS capacitance, devices consisting of alternating *n*-well and *p*-well regions separated by DTs are investigated. In such a device, a large fraction of the depletion zone in the epitaxial layer covers the DTI to Si interface leading to strong DLTS signals from the interface traps. A schematic of the test structures is shown in Fig. 1

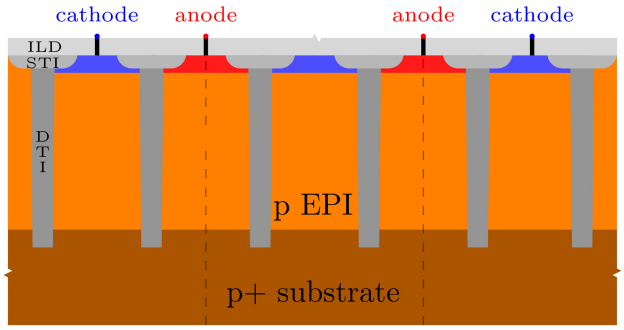

Fig. 1. Schematics of the DLTS test structures. The devices consist of p-doped epitaxial layers (EPI) grown on a p^+ substrate. Pn junctions are formed by n-well and p-well implants that are separated by deep trench isolation (DTI). Each of the stripes is contacted to form the anode and cathode node of the test structure. The DTIs are formed after shallow trench isolation (STI) and the top surface is passivated with an interlevel dielectricum (ILD). The trench-to-trench pitch is 4.42 µm, and the length of the structure in the direction perpendicular to the drawing is ≈ 40 µm. The vertical dashed lines mark the edges of the simulation domain used for the TCAD simulations presented in Section III-A.

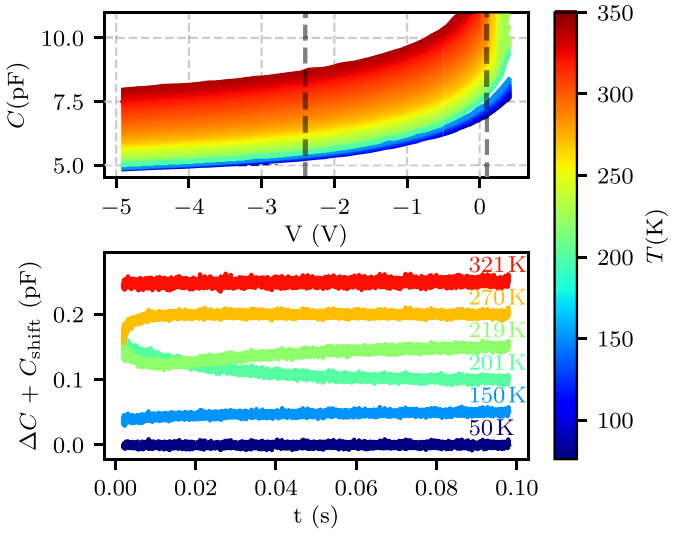

Fig. 2. **(top)** Measured Capacitance-Voltage (CV) characteristics for the DLTS test structure at various temperatures T according to the attached colorbar. The vertical dashed lines (−2.4 V 0.1 V) indicate the applied DLTS voltage levels. **(bottom)** Capacitance C versus time t at a reverse bias of 2.4 V after a 100 ms stress at a forward bias of 0.1 V at specific temperatures with characteristic minority and majority carrier trapping. The curves are arbitrarily shifted for better readability.

and the corresponding capacitance-voltage characteristics are shown in Fig. 2.

For the measurements, we used a cryogenic wafer prober (Lakeshore CRX-4K; probed temperature range 40 K to 330 K). The DLTS experiments consist of capacitance transient measurements (sampling time 100 ms with a time resolution of 10 µs), which are recorded with an in-house measurement instrument, i.e., defect probing instrument [4]. The bias is applied to the cathode while the anode is kept at 0 V.

B. Conventional DLTS

The upper plot in Fig. 2 shows capacitance transients after a 100 ms forward bias pulse voltage of 100 mV at a quiescent reverse bias of 2.4 V. The lower plot shows selected transients indicating no significant trapping at very

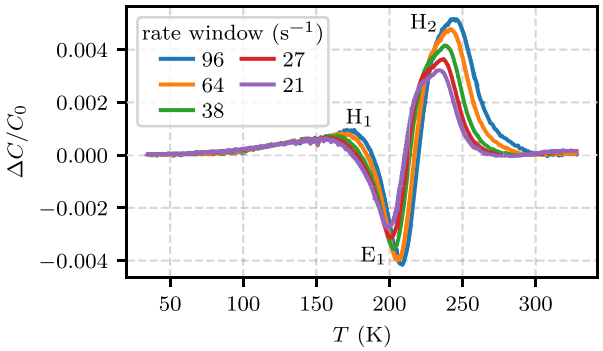

Fig. 3. Conventional DLTS plot: Normalized capacitance difference $\Delta C/C_0$ versus temperature T. Three traps, labelled H_1, H_2 and E_1 are visible.

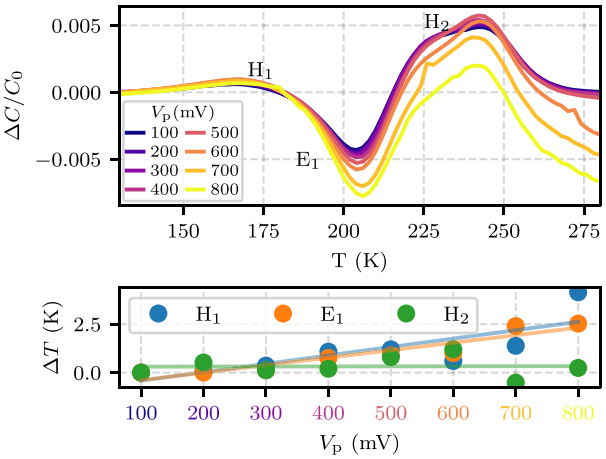

Fig. 4. DLTS analysis for a varied pulse voltage V_p. **(top)** DLTS plots for a fixed rate window of 38 s^{-1} and a varied V_p. **(bottom)** Temperature shift ΔT of the peak position versus V_p. The linear fits act as guide to the eye and show a slight shift of the peak temperature for the traps H_1 and E_1.

low and high temperatures (flat curves) and mixed majority (increasing C) and minority carrier (decreasing C) [5] trapping at about 220 K. Fig. 3 shows the conventional DLTS plot of the capacitance transients presented in Fig. 2, which is constructed by correlating the measured capacitance transient with a square wave weighting function over a varied time window. It should be noted that this form of analysis has advantages over the frequently used double boxcar approach in terms of resolution [6]. In the spectrum, three defects can be identified: two majority carrier defects (H_1, H_2) and one minority carrier defect (E_1). An additional set of DLTS measurements with varied pulse voltages is performed to distinguish between energetically discretely or continuously distributed traps, see Fig. 4. With different pulse voltages V_p the peak positions of $\Delta C(T)$ for a fixed rate window slightly shift for the traps H_1 and E_1, which indicates that these traps are continuously distributed within the bandgap rather than discrete levels [7]. A distribution of energies related to individual trap states is expected because of the amorphous interface structure [8].

C. Laplace DLTS

It is well known that the conventional DLTS analysis, i.e., the maximum temperature analysis of DLTS spectra

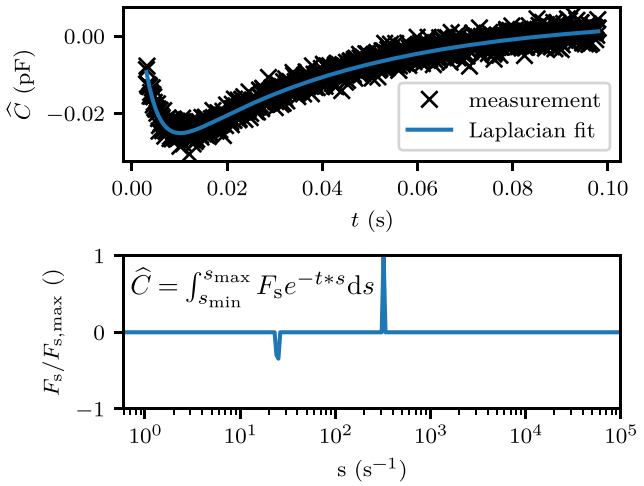

Fig. 5. Laplace DLTS extraction at 219 K with simultaneous minority and majority carrier trapping. **(top)** Normalized capacitance $\widehat{C} = \frac{C(t)-C_0}{C_0}$ versus time t. **(bottom)** Extracted Laplace coefficients F_s versus emission rates s according to inset formula.

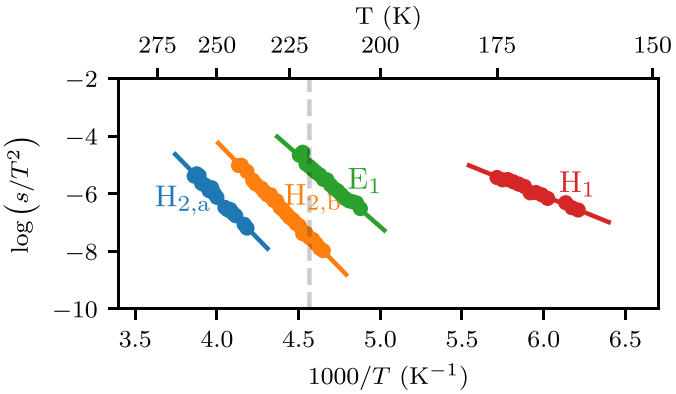

Fig. 6. Arrhenius plot from the emission rates s extracted by the LDLTS method. As can be seen, four traps are detected. The corresponding parameters are presented in Tab. I. The vertical dashed line marks the spectrum obtained at 219 K, which is shown in Fig. 5.

acquired by averaging the recorded capacitance transients with weighting functions such as the boxcar average or square wave weighting function, is limited in resolving overlapping emissions from traps with similar emission time constants [9]. The Laplacian DLTS (LDLTS) analysis has been established to overcome this limitation, where each recorded capacitance transient is de-convoluted into several exponential functions with different time constants. However, this procedure is a mathematically ill-posed problem, and the numerical solution requires advanced computational methods [10]. We employ the Lasso regularization method [11] to extract the LDTLS spectra. The extraction for a capacitance transient at 219 K can be seen in Fig. 5. The spectrum (Fig. 5, lower plot) shows 2 active traps at this temperature, one majority carrier trap and one minority carrier trap. The Arrhenius plot for the LDLTS analysis can be seen in Fig. 6, where 4 traps were detected. These correspond to the peaks H_1, H_2 and E_1 from the conventional approach in Fig. 3. However, H_2 can be resolved as two traps (labelled $H_{2,a}$ and $H_{2,b}$), with the same energies but different cross sections, by means of the

TABLE I
EXTRACTED DLTS PARAMETER

	name	E_A (eV)	σ (cm^2)[a]
●	H_1	$E_v + 0.20$	4.2×10^{-19}
●	E_1	$E_c - 0.43$	8.4×10^{-15}
●	$H_{2,a}$	$E_v + 0.50$	4.7×10^{-15}
●	$H_{2,b}$	$E_v + 0.50$	3.7×10^{-14}

[a] For the hole traps $\sigma = \sigma_p$ and the activation energy is with reference to the valence band, for the electron trap $\sigma = \sigma_n$ and the activation energy is with reference to the conduction band.

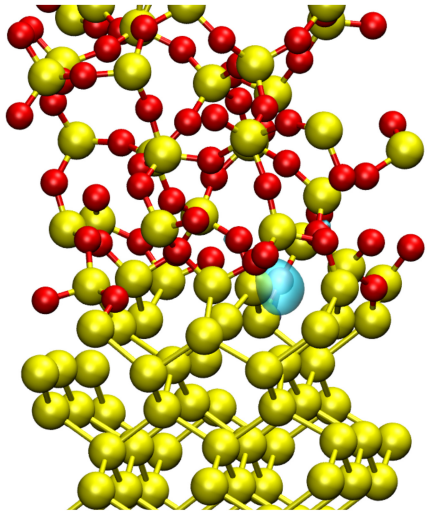

Fig. 7. Isosurface (blue) of the wavefunction (real part) of a localized dangling bond at the Si-SiO_2 interface obtained from density-functional-theory simulations. Replotted with kind permission from [19].

LDLTS analysis. Note that the ability to resolve traps with similar emission characteristics is one of the main advantages of the LDLTS technique compared to the conventional DLTS analysis [12]. Consequently, if applicable, a Laplacian analysis should be preferred over the conventional DLTS analysis. Tab. I summarizes the extracted trap parameters.

D. Defect Identification

With DLTS, the fingerprints of defects, i.e., the activation energy E_A and capture cross section σ, can be extracted. The most important defect for our study, is defect E_1, since this defect tends to interact with minority carriers, as we investigate in TCAD simulations discussed in the next section. A possible candidate for the origin of the measured signal is the P_b center, an unpaired valence electron of a silicon atom at the Si/SiO_2 interface. The trap levels of this defect type lie in the silicon band gap and are distributed around 0.4 eV below the conduction band [12]. The P_b center is also a candidate for the defect H_1 since it is known that the energetic distribution of this trap state also has a distinct peak at about 0.25 eV above E_v [13]. The low value for the cross section for H_1 stands out among the values extracted for the other defects, however, it is still within the range of values reported in the literature for cross sections of the Si/SiO_2 interface [14]. Generally, cross sections extracted by DLTS

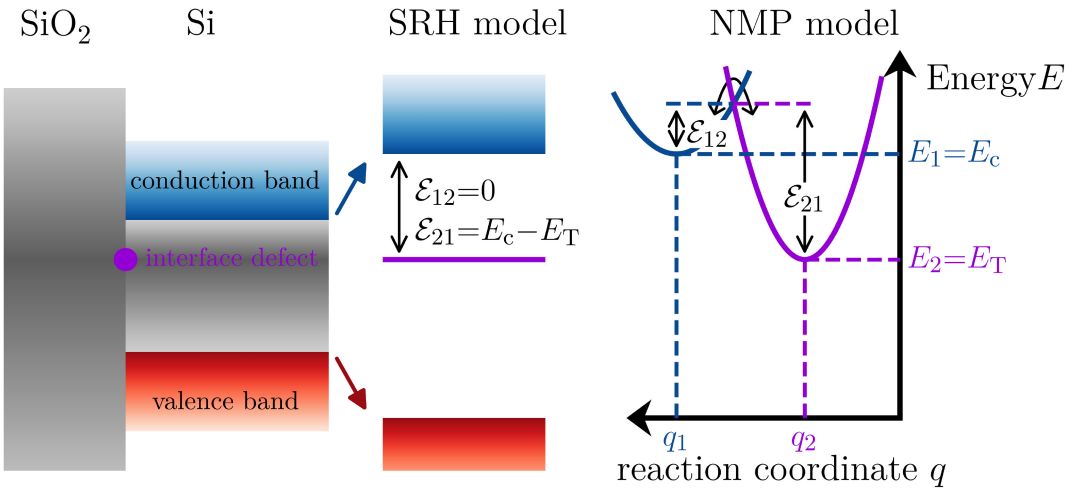

Fig. 8. Defect-carrier interaction at the Si-SiO_2 interface: Shockley-Read-Hall (SRH) model versus non-radiative multi-phonon (NMP) model considering the capture/emission of an electron from/to the conduction band to/from the trap level. **(left)** Schematics of the Si-SiO_2 interface with an interface trap level. **(center)** The SRH model considers no energetic barrier for the capture of an electron ($\mathcal{E}_{12}^{SRH} = 0$) and the barrier for the emission of a trapped electron to the conduction band is given by the trap ionization energy with respect to the conduction band energy ($\mathcal{E}_{21}^{SRH} = E_c - E_T$). **(right)** The NMP model considers the structural relaxation of the nuclei in the vicinity of the defect site.

are not unambiguously discussed [15], therefore we base our main conclusions on the extracted activation energy. It should be noted, that the activation energy E_A, as extracted with DLTS, might differ from the trap energy E_T because of a structural relaxation of the defect when changing its charge state. For the P_b center this energy difference may well be 0.05 eV as is discussed in Section III-A. Finally, a direct identification of defect H_2 remains challenging as there are many possible reported candidates for discrete defects at this energy [16], [17], [18].

III. Modeling and Simulating the DTI Interface Recombination

A. Structural Relaxation of Interface Defects

Typically, trap energies extracted by means of DLTS are considered energies with respect to the corresponding band edges, which is based on the Shockley-Read-Hall (SRH) theory, and hence structural relaxations of the defect depending on its charge state are ignored. A more sophisticated approach to model carrier emission rates from trap states, which considers the structural relaxation of the defect is the nonradiative mulitphonon (NMP) model [20]. In the following, these deviations in terms of extracted trap energies comparing the two models are discussed on the example of the Si-SiO_2 dangling bond, i.e., the P_b center. The real part of an exemplary localized defect state as obtained from density functional theory (DFT) calculations is depicted in Fig. 7. The rate for electron emission at temperature T from a trap state located at the energy E_T within the bandgap into the conduction band E_c considering the SRH model is given by [21], [22]

$$k_{21}^{SRH} = N_c v_{th} \sigma_n e^{\frac{E_T - E_c}{k_B T}} = N_c v_{th} \sigma_n e^{\frac{-\mathcal{E}_{21}^{SRH}}{k_B T}}, \quad (1)$$

where N_c is the effective density of states in the conduction band, v_{th} the thermal velocity of the electrons, and k_B the Boltzmann constant. Similarly, a transition from state 2 (electron is trapped) to state 1 (electron is in conduction band reservoir) considering the NMP model is given by

$$k_{21}^{NMP} = N_c v_{th} \sigma_n e^{\frac{-\mathcal{E}_{21}^{NMP}}{k_B T}}, \quad (2)$$

where the energetic barrier for the transition is larger compared to the SRH barrier, as is indicated in Fig. 8 and outlined below. $\mathcal{E}_{21}^{NMP}$ can be omitted by approximating the potential energy of each state in a second-order expansion (parabola) around their equilibrium position in an effective 1-dimensional coordinate system along the lowest energy path between the two states [20], which is shown schematically in the right-hand side plot of Fig. 8. A transition from one state to the other happens at the intersection of the parabolas and the process is driven by phonons, hence the name of the model. Assuming furthermore the same curvatures for the two parabolas ("*linear electron-phonon coupling*"), the problem can be parametrized in a single variable, the so-called relaxation energy $\mathcal{E}_r$. $\mathcal{E}_{21}^{NMP}$ is then given by

$$\mathcal{E}_{21}^{NMP} = \frac{(\mathcal{E}_r + E_{21})^2}{4\mathcal{E}_r}, \quad (3)$$

where $E_{21} = E_T - E_c$. For the P_b center $\mathcal{E}_r$ has been extracted to be around ≈ 0.2 eV [23], [24]. Considering that the extracted activation energy E_A in Fig. 7 corresponds to $\mathcal{E}_{21}^{NMP}$ rather than $E_{21} = -\mathcal{E}_{21}^{SRH}$ the value for E_T with respect to E_c, which considers the structural relaxation, can be calculated by inverting (3). Such a comparison between the two models is shown in Tab. II. To demonstrate the difference in emission rates of the two models a process simulation of the test structures as shown in Fig. 1 is performed. The domain consists of a single n-well stripe as indicated by the dashed lines in Fig. 1. The utilized TCAD models and corresponding parameters are as presented in [3]. Results of the simulated DLTS experiments are shown in Fig. 9 and 10. First, as shown in Fig. 9, a shift of the DLTS peaks

TABLE II
COMPARISON OF EXTRACTED TRAP ENERGIES

model	Emission barrier[a] $\mathcal{E}_{21}$	Trap energy[b] E_{21}
SRH	0.43 eV	0.43 eV
NMP[c]		0.39 eV

[a] Corresponds to the activation energy E_A as extracted by DLTS.
[b] With respect to the conduction band edge.
[c] Assuming linear electron-phonon coupling and $\mathcal{E}_r = 0.2$ eV.

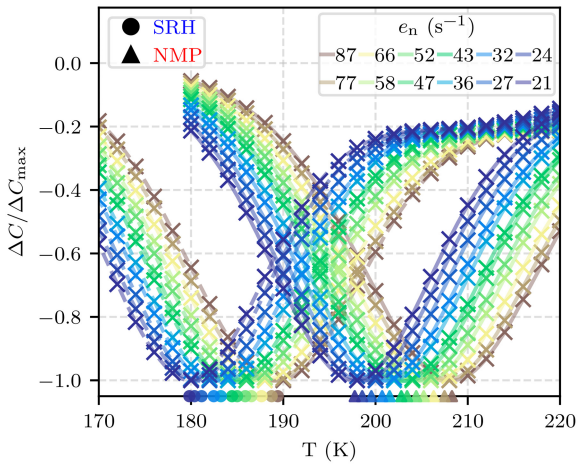

Fig. 9. TCAD simulated DLTS plot with a forward pulse voltage of 0.1 V and quiescent reverse voltage of 2.4 V. A comparison between transients with an emission barrier corresponding to the SRH and NMP model is presented. The circular and triangular markers indicate the extracted peak temperatures. The corresponding value pairs (peak temperature, emission rate) are further presented in the Arrhenius plots shown in Fig. 10.

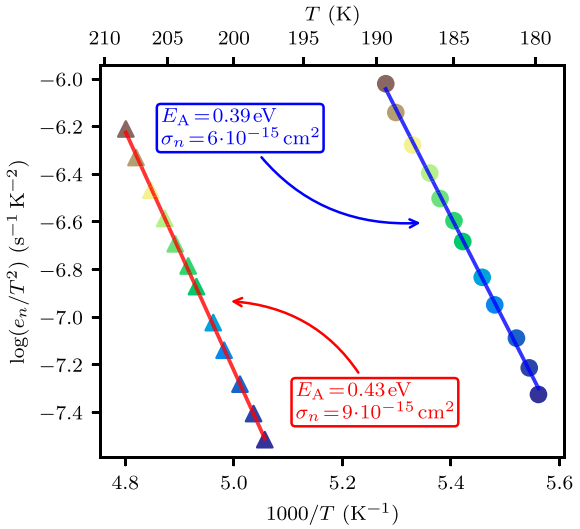

Fig. 10. Arrhenius plot of the TCAD simulated DLTS transients with emission rates and coloring corresponding to the legend shown in Fig. 9. The extracted parameters (emission barrier E_A and electron capture cross section σ_n) for the transients corresponding to emission barriers for the SRH and NMP model are shown as inset.

can be explained by small changes of the emission barriers. Quantitatively, the peak shifts by approx. 20 K although the emission barriers related to the SRH and NPM model differ by only 0.04 eV. This shift reflects the great DLTS resolution capabilities in terms of extracted trap energies as originally pointed out by Lang [5]. Secondly, in Fig. 10 the Arrhenius plots for the two data sets are presented. Here it can be seen, that the activation energies can be correctly extracted, i.e., they correspond to the simulator input as shown in Tab. II. Furthermore, the extracted values for the cross sections are close to the input value of 8.4×10^{-15} cm^2 as presented in Tab. I. Concerning the extraction of cross sections utilizing DLTS it should be mentioned, however, that the logarithm of the interceptions in the Arrhenius plots is proportional to the extracted values. Hence, already small deviations of the extracted intercepts may result in a large mismatch of this extracted parameter. In summary, the DLTS simulations presented in this section validate our experimental defect parameter extraction procedure. Furthermore, the comparison between the SRH and NMP model indicates, that already the quite small difference in emission barriers between the two models will result in a shift of the corresponding DLTS curves that is well resolvable by the linear fits in the Arrhenius plots.

B. Impact on the Performance of Photodiodes

To investigate the influence of DTI trap states in practical applications we model and simulate DTI related interface recombination using parameters extracted in the preceding sections. Recently, it was shown, that the recombination of minority carriers at interface trap states might be non-linear with respect to the excess carrier density, leading to non-linear responses of photodiodes [3]. To specifically investigate the influence of interface trap states on the performance of photodetectors, 2D TCAD simulations based on the drift-diffusion model are performed. A cross section of the simulated device can be seen in Fig. 11. We place trap E_1 at the DTI to Si interface with energy and cross section as extracted by DLTS (adopted from Tab. I). The simulation results are shown in Fig. 12, where the detector's radiant flux Φ dependent responsivity R is compared to experimental results from a DTI terminated island photodiode. The experimental results as well as simulation details are comprehensively presented in [3]. The fixed oxide charge density Q_0 and interface trap density were fitted by minimizing residuals to the experimental results and their values are shown as inset in the plot. The extracted values are well within the range of typically reported parameters for the Si/SiO_2 interface [25], [26], [27]. As can be seen, by modeling the interface recombination via the trap state E_1, good agreement between measurement and simulation can be achieved.

IV. CONCLUSION

By means of DLTS, we show that with the DTI processing a large number of defects is introduced at the critical Si-SiO_2 interface associated with the DTI sidewalls. The P_b center is identified as a possible candidate for two of the electrical active trap states. By utilizing the extracted parameters we can show, that such trap states can lead to injection-dependent recombination of photo-generated charge carriers. These recombination effects may lead to radiant-flux dependent responsivities of photodiodes terminated by deep trenches as is further shown utilizing TCAD simulations. Good

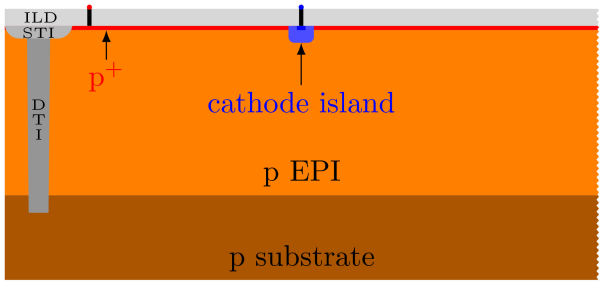

Fig. 11. Schematic of a DTI terminated island photodiode test structure consisting of an n-well cathode island embedded in the epitaxial layer. The p+ layer on top passivates the front surface and acts as an anode contact implant.

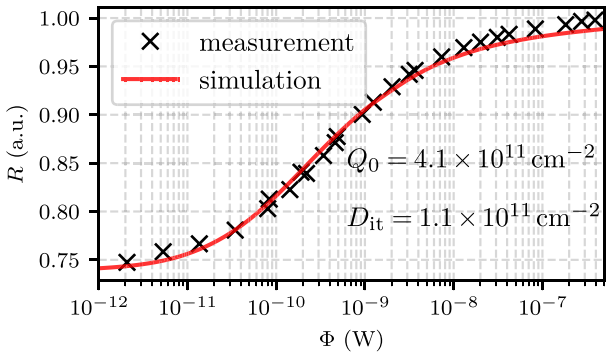

Fig. 12. Simulated and measured responsivity R versus radiant flux Φ. In the simulation trap E_1 was used to model the DTI to Si interface recombination. The fixed oxide charge density Q_0 and the trap density D_{it} were adjusted to match the experiments, the extracted values are written in the inset.

agreement between the simulated and measured responsivities of photodiodes as a function of radiant flux could be achieved by simulating the DTI interface recombination with defect E_1 (assumed to be a P_{b} center) and adjusting the fixed oxide charge density and trap density. The identification of recombination via the Pb center as the possible root cause for non-linear photodiode phenomena can contribute to further DTI processing optimization. These findings are particularly relevant because various strategies for reducing the density of dangling bonds at the Si/SiO_2 interface, including optimized oxidation parameters and specific annealing methods, are discussed in the literature [28], [29]. Finally, the influence of structural relaxation on the trap emission processes observed in DLTS experiments is discussed. A comparison between the SRH and NMP model reveals that structural relaxations (incorporated in the NMP model, ignored by the SRH model), will lead to a shift of the corresponding ΔC versus T plots that is well resolvable by the standard DLTS extraction techniques. For the P_{b} center this difference in the emission barrier is around 0.04 eV.

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