A 120–140-GHz LNA in 250-nm InP HBT

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***Abstract*— This letter presents a *D*-band low-noise amplifier (LNA) in 250-nm InP HBT technology for the next-generation wireless applications. The LNA has a measured peak gain of 13 dB, a 3-dB bandwidth greater than 20 GHz (120–140 GHz), and a measured noise figure (NF) of less than 6 dB in the band. A reduction in the 3-dB bandwidth from simulation was observed during the measurements which was attributed to the substrate waves using full chip electromagnetic (EM) simulation. EM simulations show that a partial or complete removal of the back side metallization of the InP substrate, holes in metal-1 ground plane, or a strategic placement of through-substrate vias suppress these substrate waves. To the authors' knowledge, this is the first 120–140-GHz LNA in the InP 250-nm HBT technology.**

***Index Terms*— 6G, III–V devices, *D*-band, integrated circuits (ICs), low-noise amplifier (LNA), millimeter wave circuits, wideband.**

I. Introduction

THERE is an increasing demand for higher data rates and lower latency in the wireless communication. This has pushed for increasing design efforts in the subterahertz frequency bands due to their higher available bandwidths [1], [2] and compound semiconductors due to their higher cut off frequencies [3], [4] and superior power handling capabilities [5]–[9]. Architectures with heterogeneous integration of integrated circuits (ICs) are being proposed with front-end circuits preferably in III–V technologies such as InP and GaN [6], [7]. Power amplifiers (PA) have been recently published in the *D*-band frequency in InP technology and show high output power (greater than 20-dBm peak saturated output power) and high efficiency (greater than 20% PAE) [8], [9]. In this letter, the authors present the other crucial circuit block of the front-end IC, a low-noise amplifier (LNA) in the *D*-band frequency in InP HBT technology and provide a comparison against the published work in other technologies. Insight into the LNA performance in InP HBTs is crucial for architectural decisions and system partition for multichip solutions. The presented 120–140-GHz LNA has less than 6-dB noise figure in-band which is comparable to the state-of-the-art CMOS and SiGe-based technologies.

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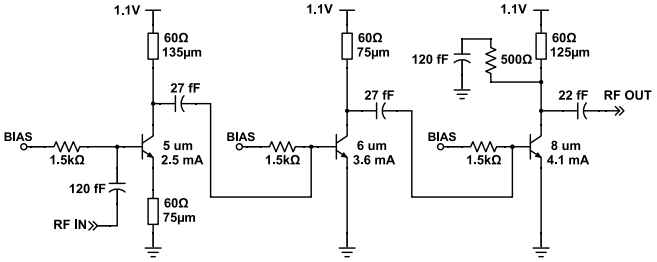

Fig. 1. Schematic of the *D*-band LNA.

II. Design

The presented *D*-band LNA is a three-stage common-emitter (CE) design as shown in Fig. 1. A CE stage with inductive degeneration and an input inductor (part of input pad structure) is used for the first stage, designed to achieve a simultaneous noise and input power match. The second stage further increases gain and the third stage provides a wideband output impedance matching. The two interstage matching are designed with staggered tuning to achieve a wideband flat gain response. A "de-Qing" resistance of 500 Ω is placed in parallel with the drain transmission line (t-lines) of the third stage to increase the 3-dB bandwidth and achieve wideband output impedance match. Current mirror biasing networks (not shown here) provide the required current densities to the three stages independently with an added flexibility of postsilicon tuning. The resistive RF choke in the biasing networks are also beneficial in preventing low-frequency oscillations.

The *D*-band LNA is designed in Teledyne Inc.'s 250-nm InP HBT technology process, featuring transistors with $f_t/f_{\max}$ of 350/600 GHz, CE breakdown voltage (BV_{CEO}) of greater than 4 V, and four metal layers. All transistors in our LNA utilize the standard devices with double-sided collector contact to reduce the collector resistance. S-parameter sweeps were done to compare different typologies and a CE topology was selected for lowest noise. To keep the noise and power consumption low, a low VDD of 1.1 V and a low current density of about 2 mA/μm^2 is used. Simulations show that a lower VDD and current densities provide lower $NF_{\min}$ (with gain trade-off), and a 3.5-dB $NF_{\min}$ and 7.5-dB $G_{\max}$ at 140 GHz for CE at these biasing conditions. The CE transistor is then sized for an optimal $Z_{\mathrm{opt}} \approx 50$ Ω. Inductive degeneration reduces the gain of the first stage and therefore noise from the second stage contributes to the overall noise performance. A trade-off between interstage noise and interstage impedance match is observed and design choices favor impedance match for a flat gain response.

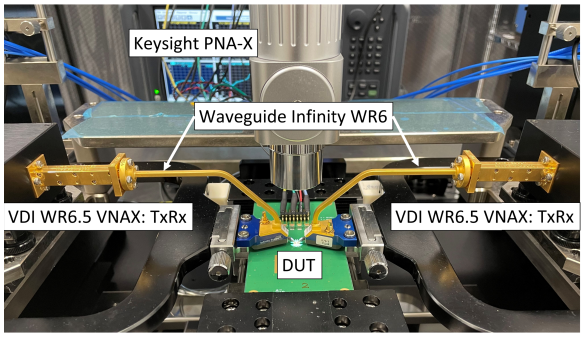

Fig. 2. Wafer probing measurement setup.

All of the inductors are realized using grounded coplanar waveguide (CPW-G) and custom-modeled using momentum electromagnetic (EM) solver. In the CPW-G structure, metal layer 4 (topmost, M4) is used as signal line, metal layers one to four (M1-M2-M3-M4) make the side shields and metal 1 (M1) is the bottom ground. The side shields of the CPW-G are beneficial in decoupling the t-lines in different stages. The t-lines have a higher characteristic impedance of 60 Ω (as opposed to typical 50 Ω) to reduce the physical length and enable compact design.

The input and output ground-signal-ground (GSG) pads are EM simulated and codesigned for optimal input and output impedance match. Due to soft interlayer dielectric, benzocyclobutene (BCB), all the pads are anchored down to the substrate using vias and all three metal layers. The ground plane underneath the signal pads is removed to reduce the parasitic capacitance, and an inverted pyramid structure using metal layers and vias is created to anchor signal pads to the substrate. A complete layout with RF pads, bypass capacitors, and matching networks is EM simulated in momentum for more accurate simulations and confirm the stability at the subterahertz frequencies. A bank of through-substrate vias connect the on-chip ground plane (M1) with the back-plate metallization (gold) of the InP substrate.

III. Measurement Results

The LNA is characterized through wafer-probing (MPI TS150-THz probe station). The bare dies are packaged on printed-circuit-boards (PCBs) with wire-bonded dc connections and substrate's back-plate metal grounded to the PCB ground.

A. S-Parameter Measurement Setup and Results

As shown in Fig. 2, VDI *D*-band extender modules (WR6.5 VNAX: TxRx) are used with a Keysight PNA-X N5247B which together provide a measurement frequency range of 110–170 GHz. FormFactor Inc.'s (formerly CascadeMicrotech) Waveguide Infinity WR6 probes with 100-μm pitch are used. A multiline thru-reflect-line (TRL) calibration is used to calibrate and bring reference to the tip of the probes. An Impedance Standard Substrate (ISS) from CascadeMicrotech provided the required Thru, Short (Reflect), and three line lengths for the TRL calibration.

Figs. 3 and 4 compare the measured (blue curves) and simulated S-parameters (black curves) results of the LNA across

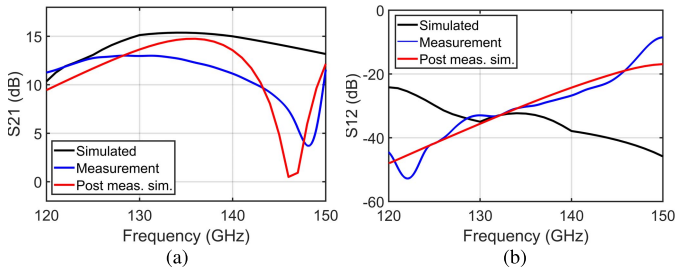

Fig. 3. Simulation, measurement and postmeasurement simulation of (a) S_{21} and (b) S_{12}.

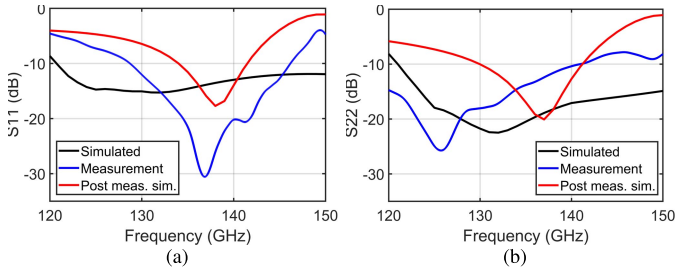

Fig. 4. Simulation, measurement and postmeasurement simulation of (a) S_{11} and (b) S_{22}.

120–150 GHz. The measured S_{21} show a peak gain of 13 dB at around 130 GHz and a 3-dB bandwidth from 120 to 140 GHz, lower than simulated 15-dB gain and wider bandwidth. Both S_{11} and S_{22} measurement results show a reduction in the input and output impedance matching bandwidths, while S_{22} also show a downward shift in frequency. Finally, the measured S_{12} is less than -25 dB up to 140 GHz, as shown in Fig. 3(b), but show a low isolation between input and output at 150 GHz. This difference between measurement and simulations has been traced to the presence of substrate waves at around 150 GHz, as discussed in Section III-B.

B. Substrate Waves and Full-Chip EM Simulation Results

To reduce the parasitic capacitance of the input and output RF pads, the M1 ground plane was removed underneath the RF pads. It was observed that the RF signal then leaks into the substrate through the holes in the M1 ground plane in the upper *D*-band frequencies. Substrate waves are created that propagate through the substrate underneath the LNA, creating an alternate path and reduce the reverse isolation significantly; impacting the S-parameter performance of the LNA negatively and thus reducing the 3-dB bandwidth. The presence of substrate waves was not detected through the EM simulation using momentum EM solver during the design. Postmeasurement full-chip EM simulation using Ansys HFSS show these substrate waves, as depicted in Fig. 5. The on-chip M1 ground plane and the grounded back-plate metal provide a waveguide-like structure for the propagation of substrate waves. The low resistivity of the InP substrate contributing to the phenomenon. Figs. 3 and 4 show the simulated S-parameter of the LNA in the presence of substrate waves (red curves) that closely match with the measurement results. EM simulations using Ansys EDT HFSS show that the (strategically-) partial or complete removal of the back-plate metallization, discontinuity in M1 ground plane (e.g., in the presence of inductors/transformers),

TABLE I
LNA PERFORMANCE COMPARISON

	This Work	[10] 2019	[2] 2021	[11] 2021	[12] 2018	[13] 2017	[14] 2008	[15] 2018
Process	InP HBT 250nm	InP HBT 250nm	CMOS 65nm	CMOS FD-SOI 22nm	SiGe BiCMOS 130nm	GaAs mHEMT 50nm	InP HEMT 35nm	InP HEMT 500nm
Freq. (GHz)	130	180	152.2	145	144	130	170	135
3-dB BW (GHz)	120-140	140-220	146.7-157.7	131-162	110-162	97-164	155-185	120-150
Max Gain (dB)	13	17.7	17.9	21	32.6	30.8	16	21
NF (dB)	4-6	7.5*	4.7-6.2	5.5-6*	4.8-6.1	3-4	3.7-5	3.7-4.5
DC Power (mW)	11.22	48	13.73	46	28	57.6	–	47
Area (mm^2)	0.042**	0.42	–	0.02**	0.6**	–	0.5	0.69

*simulated. **active area w/o pads. (The values are estimated from the plots if not mentioned explicitly by authors in the text.)

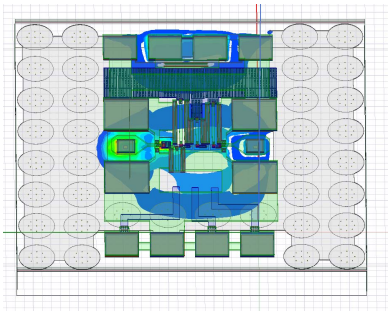

Fig. 5. Figure showing electric field in the substrate at 150-GHz signifying substrate wave propagation.

and/or a strategic placement of through substrate vias help in preventing the propagation of substrate waves. This is a significant learning outcome from these measurements and simulation exercises and provide crucial insights for future designs in this technology.

C. Noise Figure Measurement Setup and Results

Noise figure (NF) is measured using the Y-factor technique with a Rohde & Schwarz spectrum analyzer (FSW43) and a *D*-band mixer (R&S FS-Z170), shown in Fig. 6. An ELVA Model ISSN-06 noise source is used to provide a *D*-band input noise with an excess noise ratio (ENR) in the range of 10.5–15.5 dB. An external LNA by Radiometer Physics (RPG D-LNA 110–170 GHz) is used between our device-under-test (DUT) and the spectrum analyzer to reduce the measurement noise floor. The external LNA has a typical 20-dB gain and 4.5-dB NF in the 120–140-GHz band. The input and output losses of the waveguide probes (typical 3.5 and 2.5 dB, respectively, from the manufacturer tables) are deembedded using the Friis equation. The R&S FSx-K30 software option automates the NF measurement. Fig. 7(a) shows the simulated (both in-the-presence-of and without the substrate waves) and the measured NF of the LNA. Simulations show a 6–6.5-dB NF in 120–140 GHz whereas the measurement show better NF of less than 6 dB.

The LNA has a -19-dBm simulated input $P_{1\text{ dB}}$ at 140 GHz. Fig. 7(b) shows the die photograph. The LNA design is quite compact with only 140×300 μm^2 (without pads and bypass caps) core area. The diced LNA die size is approximately 955×1000 μm^2 but only 385×700 μm^2 of that is active area including the dc pads, the RF pads, and the on-chip bypass caps. Finally, from a 1.1-V supply the LNA consumes a 10.2-mA current and 11.22-mW dc power. The biasing network consume another 10-mA current.

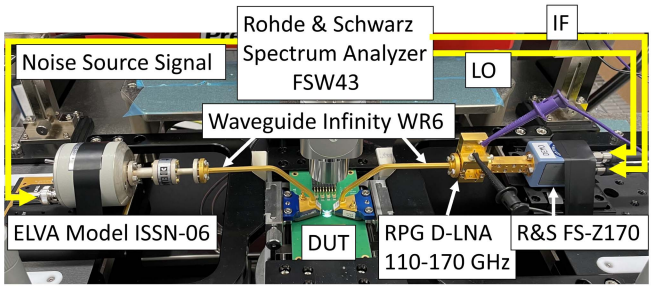

Fig. 6. NF measurement setup.

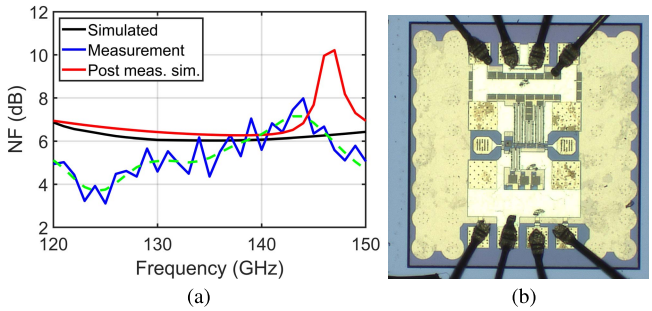

Fig. 7. (a) Simulation, measurement and postmeasurement simulation of NF and (b) die photograph of the *D*-band LNA (955×1000 μm^2 die size with 140×300 μm^2 core area excluding all pads).

IV. CONCLUSION

A compact *D*-band LNA which provides low noise and high gain across 120–140 GHz has been presented. The LNA has less than 6-dB NF in the 3-dB bandwidth and a 13-dB peak gain. Substrate waves are observed at 150 GHz facilitated by a combination of low resistivity of the substrate, M1 ground plane, and the back plate metallization that reduce the bandwidth. Table I compares the presented 130-GHz InP LNA to the state-of-the-art and show that an LNA in the InP HBT technology can provide NF comparable to the state-of-the-art CMOS and SiGe-based technologies. While LNAs in several HEMT technologies can provide lower NF than InP HBT (as shown in Table I), being able to make a reasonable LNA in the same InP HBT node that is often preferred for PAs is crucial for architectural decisions and system partition for multichip heterogeneous solutions.

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