160-GSa/s-and-Beyond 108-GHz-Bandwidth Over-2-V_{ppd} Output-Swing 0.5-μm InP DHBT 2:1 AMUX-Driver for Next-Generation Optical Communications

R. Hersent, A. Konczykowska, F. Jorge, F. Blache, V. Nodjiadjim, M. Riet, C. Mismer, and J. Renaudier

***Abstract*— This letter reports on a 108-GHz bandwidth 0.5-μm InP DHBT analog-multiplexer-driver (AMUX-driver). To the best of the authors' knowledge, this 2:1 AMUX-driver shows unprecedented 1.9-V_{ppd} 160-GSa/s 160-GBd non-return-to-zero (NRZ) and 2.4-V_{ppd} 100-GSa/s 100-GBd PAM-4 output swings, with very high-quality eye diagrams, without any digital signal processing (DSP) or postprocessing. Up to 3.2 V_{ppd} is obtained in NRZ at 100 GBd. The lumped AMUX-driver also shows record 25.7-dB gain and 2.08-THz gain-bandwidth product with 11.1-dB equalizing capabilities at 86.6 GHz.**

***Index Terms*— Analog multiplexer (AMUX), double-heterojunction bipolar transistor (DHBT), four-level pulse amplitude modulation (PAM-4), indium phosphide (InP), large-swing linear modulator driver.**

I. Introduction

WHILE video streaming, cloud computing, and ramping-up 5G applications massive use generate tremendous data volumes, current optical networks' capacity is heading toward saturation. Among the paths to tackle this challenge, combining a high electrical symbol rate (>100 GBd) with the four-level pulse-amplitude modulation (PAM-4) is now deeply investigated (see [1]–[3]).

However, digital transceivers rely on Si CMOS digital-to-analog converters (DACs), in which bandwidth limitations (<40 GHz) prevent further symbol rate increase [4], [5]. Hence, DACs' bandwidth summation, through analog multiplexing, has gained traction to enhance optical transceivers' capacity (see [6]). Yet, to truly improve the transmitters' performances, bandwidth-limiting interconnections' number must be minimized. Therefore, analog multiplexers (AMUXs) should be monolithically integrated with linear drivers to directly drive the electro-optical (E/O) modulators while providing equalization capabilities for the driver–modulator interconnection losses' compensation. To ensure full compatibility with current digital transceivers, this AMUX-driver should provide an over-20-dB gain, an over-2-V_{ppd} linear swing, and a beyond-100-GHz bandwidth with high equalization capabilities.

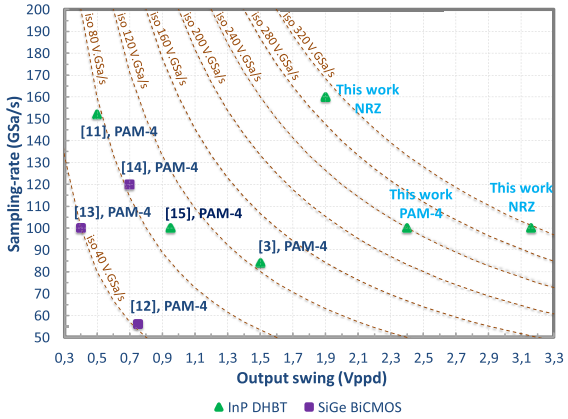

Fig. 1. High-sampling-rate AMUX and AMUX-driver state of the art.

Several AMUX realizations are presented in [7]–[10], yet output swings are not reported. The AMUX and AMUX-driver state of the art are depicted in Fig. 1, where their ability to operate at a very-high sampling rate while providing a large output swing is compared. Among existing implementations, [11] and [3], respectively, show the highest published PAM-4 sampling rate and output swing. However, the resulting eye diagrams' quality and output swings are rather low although heavy DSP was used.

In this letter, we present the design and characterization of a 108-GHz bandwidth 0.5-μm InP double-heterojunction bipolar transistor (DHBT) 2:1 AMUX-driver with unprecedented over-2-V_{ppd} 160-GSa/s 160-GBd and 100-GSa/s 100-GBd output swings and very high PAM-4 and non-return-to-zero (NRZ) eye diagram quality, while neither DSP nor postprocessing has been used. This lumped-architecture AMUX-driver also shows record 25.7-dB gain and 2.08-THz gain-bandwidth product with 11.1-dB equalization capabilities at 86.6 GHz. This AMUX-driver obtains the highest PAM-4 and NRZ sampling rate × output swing product published to date (see Fig. 1).

II. InP DHBT AMUX-Driver Design and Technology

The 2:1 AMUXs' interleaving cells, which perform the critical multiplexing operation, are based on modified *Gilbert*

Manuscript received February 25, 2022; accepted March 15, 2022. Date of publication April 8, 2022; date of current version June 7, 2022. This work was supported by the European Commission through the Photonics Public Private Partnership Initiatives under Grant H2020-ICT-2016-2017 (QAMeleon Project) and Grant H2020-ICT-2019-2 (Twilight Project). *(Corresponding author: R. Hersent.)*

R. Hersent, F. Jorge, F. Blache, V. Nodjiadjim, M. Riet, and C. Mismer are with the III-V Lab, 91767 Palaiseau, France (e-mail: romain.hersent@3-5lab.fr).

A. Konczykowska is with the III-V Lab, 91767 Palaiseau, France, and also with ADesign, 94240 l'Haÿ-les-Roses, France.

J. Renaudier is with Nokia Bell Labs France, 91620 Nozay, France.

This article was presented at the IEEE MTT-S International Microwave Symposium (IMS 2022), Denver, CO, USA, June 19–24, 2022.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2022.3161706.

Digital Object Identifier 10.1109/LMWC.2022.3161706

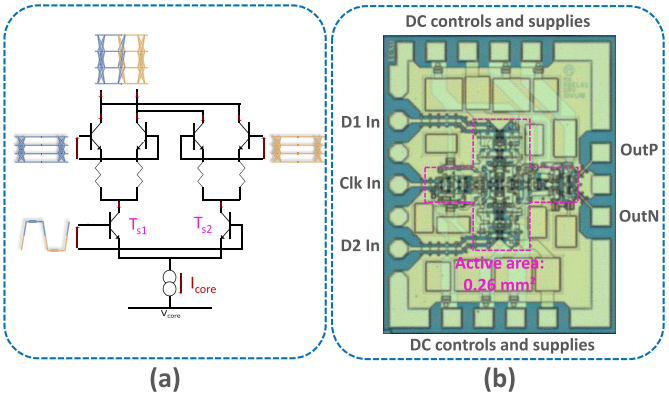

Fig. 2. InP DHBT AMUX-driver interleaving cell and die microphotograph. (a) Interleaving cell schematic and multiplexing operation illustration. (b) AMUX-driver die microphotograph.

cells [see Fig. 2(a)]. Such architecture is used in [3], [11], and [15], whereas, in [12]–[14], two *Gilbert* cells are actively combined through a cascode amplifier. Because, in this last architecture, four differential pairs must be simultaneously driven by the clock signal, it implies higher routing complexity and higher footprint and imposes more stringent clock-alignment requirements, compared to single-*Gilbert*-cell AMUX designs, for a given technology. Moreover, as the clock amplifier's total capacitive load is drastically increased, it is also more sensitive to clock-path bandwidth limitations.

Besides, for a given input clock signal, minimizing the interleaving cell tail current, I_{core}, leads to higher quality (i.e., higher signal-to-noise-ratio) output signals to the output swing and gain detriment (see Section III-B). Indeed, when I_{core} is reduced, the switching transistors, $T_{S1/2}$ on Fig. 2(a), are more rapidly turned on/off, hence preventing intersymbol interferences (ISIs) that occur when $T_{S1/2}$ are simultaneously conducting (i.e., sampling the input signals). Therefore, the switching-mode duration is reduced, while the "track-mode" one is increased, yielding higher horizontal and vertical eye openings. However, this work's originality is to take advantage of I_{core} overshoots to preserve linearity while operating at low I_{core} and, thus, maximizing the output signal quality. Indeed, current overshoots can be generated when $T_{S1/2}$ are overdriven and pushed far into the nonlinear regime by the clock signal. Thus, an optimum I_{core} (quiescent and peak-overshoot values) is determined during the design phase in order to maximize the output signal's quality while preserving linearity and may be adjusted if necessary during measurements according to input signals' characteristics (data and clock) and transistors' performances.

The AMUX-driver is implemented in a 0.5-μm InP DHBT technology, which shows 360-/450-GHz f_T/f_{MAX}, a 45 static-current gain, β, and an over 4-V BV_{CE0} (see [16] and [17]). The AMUX-driver die microphotograph is depicted on Fig. 2(b). It measures 1.2 × 1.5 mm^2, while the active area is 0.26 mm^2. The AMUX-driver dc power consumption is 1.3 W.

The AMUX-driver is based on a lumped architecture for a minimal footprint. Its input–output transmission lines are broadband coplanar waveguides to ensure the minimum loss, even beyond 100 GHz. ON-chip low-ohmic R–C-damped decoupling networks were used for proper biasing and high operation stability. Single-ended input interfaces were designed to ease packaging efforts as the second step, while the differential output allows a direct drive of the E/O modulator. The AMUX-driver data path is composed of a two-stage input linear amplifier, a resistively degenerated *Gilbert* cell [see Fig. 2(a)], which is followed by a two-stage linear output preamplifier and a linear driver. Data input amplifiers provide input impedance matching on a 50-Ω source, single-ended-to-differential conversion, and linear gain to drive the interleaving cell with high-quality differential signals. The output linear preamplifier and driver provide most of the voltage and power gain, an over 2-V_{ppd} linear output swing, high equalization capabilities, and impedance matching on a 100-Ω_{diff} load. To conjugate a very-high gain–bandwidth product and a large-linear-output swing, the driver architecture is based on a resistively degenerated paralleled-transistor cascode differential pair (see [18], [19]). Besides, a two-stage clock-path amplifier was used to ensure proper clock signal single-ended-to-differential conversion. This is highly critical in order to reach a high sampling-operation symmetry of both input data and prevent output signal quality degradations. To ensure a good tradeoff between the clock-path's bandwidth, common-mode rejection, gain, and power consumption, both amplifying stages are composed of emitter followers, cascaded with a low-ohmic-degenerated differential pair that features >100-Ω common-mode resistances. Finally, a double emitter follower stage performs the clock amplifier to switching transistors impedance matching to maximize the clock-path bandwidth and prevent ISI from occurring, especially during ≥100-GSa/s operations, in ensuring that the interleaving cell is driven with a large enough voltage swing.

III. InP DHBT AMUX-Driver Characterization

A. Small-Signal Frequency Measurements

The AMUX-driver on-wafer single-ended S-parameter measurements were conducted from 70 kHz to 110 GHz using a two-port Anritsu ME7808A vector network analyzer (VNA). Fig. 3(a) depicts the single-ended gain, S_{21}, and input reflection, S_{11}, S-parameters. A 19.7-dB (25.7-dB differential) $|S_{21}|$ is obtained at 25 MHz together with a 108-GHz −3-dB bandwidth and 11.1-dB equalization capabilities at 86.6 GHz. Fig. 3(b) shows the output reflection, S_{22}, and the input–output isolation, S_{12}, S-parameters. Apart from few resonances, $|S_{11}|$ and $|S_{22}|$ remain below −10 dB up to, respectively, 110 and 102 GHz. Hence, a good impedance matching is obtained on 50 Ω. $|S_{12}|$ remains below −32 dB over 110 GHz, thus ensuring a good AMUX-driver stability, as depicted on the μ stability factor, as shown in the inset in Fig. 3(a), which remains above 1 across 110 GHz. μ was retrieved from the S-parameters. Besides, Fig. 3 depicts a comparison between measurements and EM-circuit cosimulation (see [16], simulation flow), testifying of a high AMUX-driver-behavior modeling accuracy.

B. Large-Signal Digital Measurements

The AMUX-driver large-signal digital measurements were conducted on the wafer at 100 GBd in PAM-4 and NRZ. To generate high-quality (2^{15}-1)-bit 50-GBd PAM-4 input data, 50 Gb/s signals were fed to an InP DHBT 2-bit active combiner module. The AMUX-driver was connected to one of the combiners' outputs through a passive broadband balun, 20-cm V-connector cables, and 67-GHz V-connector probes.

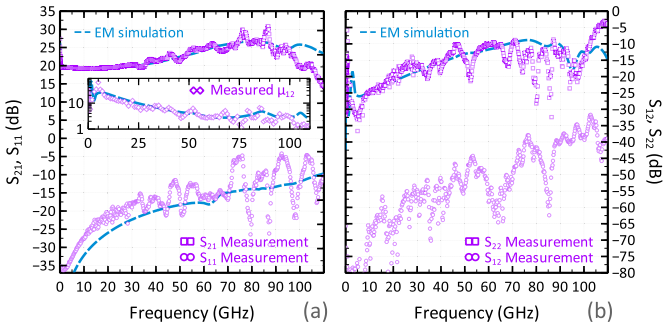

Fig. 3. InP DHBT AMUX-driver single-ended S-parameter measurements. (a) S_{21} and S_{11}, inset: μ stability factor. (b) S_{22} and S_{12}. Measurements are displayed in magenta with symbols and EM-circuit co-simulation in blue broken lines.

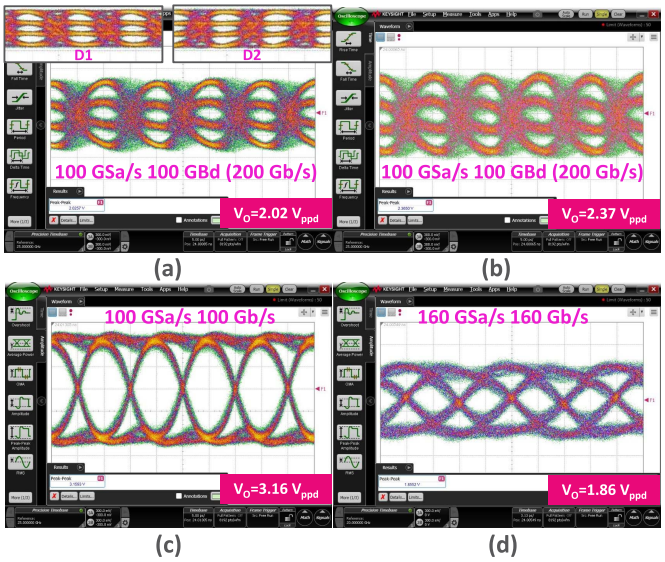

Fig. 4. InP DHBT AMUX-driver large-signal digital measurements. (a) 100-GSa/s 100-GBd 2.0-V_{ppd}-swing PAM-4 output eye diagram. (b) 100-GSa/s 100-GBd 2.4-V_{ppd}-swing PAM-4 output eye diagram. (c) 100-GSa/s 100-Gb/s 3.2-V_{ppd}-swing NRZ output eye diagram. (d) 160-GSa/s 160-Gb/s 1.9-V_{ppd}-swing NRZ output eye diagram. The insets of (a) are the 220-mV_{pp} 50-GBd PAM-4 input data (D1 and D2) used for (a) and (b) eye diagram measurements. Horizontal and vertical scales of (a)–(c) are, respectively, 5 ps/div and 600 mV/div. Horizontal and vertical scales of (d) are, respectively, 3.125 ps/div and 500 mV/div.

A passive adjustable 65-GHz V-connector delay line was connected to one of the balun's outputs to decorrelate the AMUX-driver input data signals. These 50-GBd PAM-4 input signals, D1 and D2, were measured at cables' output prior to connection with the 67-GHz input probe [see the insets in Fig. 4(a)] with about 220-mV_{pp} PAM-4 amplitude. Moreover, the AMUX-driver is clocked with a 50-GHz 300-mV_{pp} low-jitter sine wave. Eye diagrams were captured using a 122-GHz bandwidth sampling oscilloscope, whose remote heads were connected to 67-GHz V-connector output probes, through 65-GHz 10-dB attenuators.

Fig. 4(a) and (b), respectively, depicts the AMUX-driver 100-GSa/s 100-GBd (200-Gb/s) PAM-4 high-quality differential output eye diagrams with 2.0- and 2.4-V_{ppd} output swings, both obtained with the same input signals. In Fig. 4(a), the interleaving cell tail current was reduced to optimize the output signal quality to the gain's and output swing's detriment (see Section II). An 11-ps (198°) clock-phase margin is obtained. Besides, Fig. 4(c) shows the 3.2-V_{ppd}-swing high-quality 100-GSa/s 100-Gb/s NRZ eye diagram measurements, while the AMUX-driver is operated in the saturated regime (320-mV_{pp} inputs). Moreover, AMUX-driver's 160-GBd measurements were conducted using a similar setup, yet an InP DHBT 2:1 selector module was used instead of the combiner to generate 80-Gb/s 200-mV_{pp}-amplitude input data in multiplexing two independent 40-Gb/s NRZ signals (see [20]). An 80-GHz 390-mV_{pp} low-jitter sine wave was used as AMUX-driver's input clock. Fig. 4(d) depicts the AMUX-driver's high-quality 1.9-V_{ppd}-swing 160-GSa/s 160-Gb/s NRZ differential eye diagram with a 4-ps (230°) measured clock-phase margin. In all measurements, 50 waveforms were accumulated.

One should note that neither DSP nor postprocessing was used; hence, the presented results depict the AMUX-driver plus measurement setup raw performances. Besides, no AMUX-driver unstable behavior was observed during small- or large-signal measurements. Based on the obtained signal's quality without DSP and the AMUX-driver ultrahigh bandwidth, higher symbol-rate operations should be possible both in PAM-4 and NRZ. Finally, Table I depicts the AMUX and AMUX-driver detailed state of the art.

TABLE I
AMUX AND AMUX-DRIVER DETAILED STATE OF THE ART

	[14]	[3]	[11]	This work	
Technology	SiGe BiCMOS	InP DHBT	InP DHBT	InP DHBT	
Data-path					
Bandwidth (GHz)	50	>110	>110	108	
Gain (<1GHz) (dB)	-2	10.5	3	25.7	
Gain×bandwidth (GHz)	39.7	>368	>155	2080	
Equalisation (dB/GHz)	-/-	8/85	4/95	11.1/86.8	
Modulation Format	PAM-4	PAM-4	PAM-4	PAM-4	NRZ
Sampling-rate (GSa/s)	120	84	152	100	160
Voltage Swing (V_{ppd})	0.7	1.5	0.5	2.4	1.9
Clock-Phase margin (°)	130	-	-	198	230
Power consumption (W)	2.17	0.99	0.9	1.3	
DSP required	Yes	Yes	Yes	No	
Full die/active areas (mm^2)	1.46/-	4/-	4/0.36	1.8/0.26	

IV. Conclusion

In this letter, we present the monolithic integration of an AMUX and a lumped linear driver in a 0.5-μm InP DHBT technology. The AMUX-driver shows unprecedented 2.4-V_{ppd}-swing high-quality 100-GSa/s 100-GBd PAM-4 eye diagrams with a 198° clock-phase margin, while neither DSP nor postprocessing was used. Record 3.2- and 1.9-V_{ppd}-output-swing high-quality signals are also respectively obtained at 100 GSa/s 100 Gb/s and 160 GSa/s 160 Gb/s in NRZ. Besides, this 108-GHz-bandwidth lumped AMUX-driver shows record 25.7-dB gain and 2.08-THz gain-bandwidth product with 11.1-dB equalization capabilities at 86.6 GHz.

Acknowledgment

The authors would like to thank T. K. Johansen from Danmarks Tekniske Universitet (DTU) for the InP DHBT technology modeling.

References

[1] A. Konczykowska, J.-Y. Dupuy, F. Jorge, M. Riet, V. Nodjiadjim, and H. Mardoyan, "Extreme speed power-DAC: Leveraging InP DHBT for ultimate capacity single-carrier optical transmissions," *J. Lightw. Technol.*, vol. 36, no. 2, pp. 401–407, Jan. 15, 2018, doi: 10.1109/JLT.2017.2760507.

[2] F. Buchali, M. Chagnon, K. Schuh, and V. Lauinger, "Beyond 100 GBaud transmission supported by a 120 GSA/S CMOS digital to analog converter," in *Proc. 45th Eur. Conf. Opt. Commun. (ECOC)*, 2019, pp. 1–4, doi: 10.1049/cp.2019.0843.

[3] M. Nagatani *et al.*, "A 110-GHz-bandwidth 2:1 AMUX-driver using 250-nm InP DHBTs for beyond-1-Tb/s/carrier optical transmission systems," in *Proc. IEEE BiCMOS Compound semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, pp. 1–4, doi: 10.1109/BCICTS45179.2019.8972726.

[4] C. Laperle and M. O'Sullivan, "Advances in high-speed DACs, ADCs, and DSP for optical coherent transceivers," *J. Lightw. Technol.*, vol. 32, no. 4, pp. 629–643, Feb. 1, 2014, doi: 10.1109/JLT.2013.2284134.

[5] T. Drenski and J. C. Rasmussen, "ADC & DAC—Technology trends and steps to overcome current limitations," in *Proc. Opt. Fiber Commun. Conf. Expo. (OFC)*, 2018, pp. 1–3.

[6] F. Buchali, "Beyond 1 Tbit/s transmission using high- speed DACs and analog multiplexing," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, 2021, pp. 1–56.

[7] D. Ferenci, M. Grozing, and M. Berroth, "A 25 GHz analog multiplexer for a 50GS/s D/A-conversion system in InP DHBT technology," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2011, pp. 1–4, doi: 10.1109/CSICS.2011.6062440.

[8] M. Nagatani *et al.*, "A 50-GHz-bandwidth InP-HBT analog-MUX module for high-symbol-rate optical communications systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540042.

[9] M. Nagatani *et al.*, "A 128-GS/s 63-GHz-bandwidth InP-HBT-based analog-MUX module for ultra-broadband D/A conversion subsystem," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 134–136, doi: 10.1109/MWSYM.2017.8058858.

[10] T. Tannert *et al.*, "Analog 2:1 multiplexer with over 110 GHz bandwidth in SiGe BiCMOS technology," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Dec. 2021, pp. 1–4, doi: 10.1109/BCICTS50416.2021.9682492.

[11] M. Nagatani *et al.*, "An over-110-GHz-Bandwidth 2:1 analog multiplexer in 0.25-μm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 655–658, doi: 10.1109/MWSYM.2018.8439317.

[12] T. Tannert *et al.*, "A SiGe-HBT 2:1 analog multiplexer with more than 67 GHz bandwidth," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Oct. 2017, pp. 146–149, doi: 10.1109/BCTM.2017.8112931.

[13] H. Ramon *et al.*, "A 700 mW 4-to-1 SiGe BiCMOS 100 GS/s analog time-interleaver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 214–216, doi: 10.1109/ISSCC19947.2020.9062978.

[14] M. Collisi and M. Moller, "A 120 GS/s 2:1 analog multiplexer with high linearity in SiGe-BiCMOS technology," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4, doi: 10.1109/BCICTS48439.2020.9392970.

[15] R. Hersent *et al.*, "Analog-multiplexer (AMUX) circuit realized in InP DHBT technology for high order electrical modulation formats (PAM-4, PAM-8)," in *Proc. 23rd Int. Microw. Radar Conf. (MIKON)*, Oct. 2020, pp. 222–224, doi: 10.23919/MIKON48703.2020.9253772.

[16] R. Hersent *et al.*, "Design, modelling and characterization of a 3-Vppd 90-GBaud Over-110-GHz-bandwidth linear driver in 0.5-μm InP DHBTs for optical communications," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Dec. 2021, pp. 1–4, doi: 10.1109/BCICTS50416.2021.9682463.

[17] V. Nodjiadjim *et al.*, "0.7-μm InP DHBT technology with 400-GHz f_T and f_{MAX} and 4.5-V BV_{CE0} for high speed and high frequency integrated circuits," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 748–752, 2019, doi: 10.1109/JEDS.2019.2928271.

[18] H. Romain *et al.*, "Over 70-GHz 4.9-vppdiff InP linear driver for next generation coherent optical communications," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, doi: 10.1109/BCICTS45179.2019.8972779.

[19] R. Hersent *et al.*, "106-GHz bandwidth InP DHBT linear driver with a 3-V ppdiff swing at 80 GBd in PAM-4," *Electron. Lett.*, vol. 56, no. 14, pp. 691–693, Jul. 2020, doi: 10.1049/el.2020.0654.

[20] A. Konczykowska *et al.*, "212-Gbit/s 2:1 multiplexing selector realised in InP DHBT," *Electron. Lett.*, vol. 55, no. 5, pp. 242–244, Mar. 2019, doi: 10.1049/el.2018.7545.