A 1–170-GHz Distributed Down-Converter MMIC in 35-nm Gate-Length InGaAs mHEMT Technology

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***Abstract*— This letter demonstrates two distributed down-converter monolithic microwave integrated circuits (MMICs). MMIC1 contains a distributed down-conversion mixer and MMIC2 expands MMIC1 by an eight-cell distributed local oscillator (LO) driver amplifier. The letter includes an investigation of the optimal gate width for each of the transistors in the stack of the source-feedback mixer cells. The MMICs are fabricated in the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg im Breisgau, Germany, 35-nm gate-length metamorphic high-electron-mobility transistor technology. MMIC2 achieves a conversion gain (CG) of better than −4.2 dB over a 1–170 GHz radio frequency (RF) bandwidth (BW) at a fixed intermediate frequency (IF) of 0.1 GHz. The LO power (P_{LO}) of MMIC2 is only −1 dBm. Furthermore, the mixer has a variable gain feature. By adjusting P_{LO}, the CG can be controlled without affecting the RF-input-power-related 1-dB CG compression of −1.7 dBm. To the best of the authors' knowledge, this work demonstrates the largest BW for distributed down-conversion mixers and for distributed mixers (DMs) with a sliding LO.**

***Index Terms*— Distributed amplifiers (DAs), distributed mixers (DMs), high-electron-mobility transistors (HEMTs), metamorphic HEMTs (mHEMTs), millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), thin-film microstrip transmission lines (TFMSLs), traveling-wave amplifiers (TWAs).**

I. Introduction

In RECENT work, we demonstrated distributed amplifiers (DAs) with more than a 300-GHz bandwidth (BW) with a low noise figure and a high output power [1], [2]. Furthermore, other groups and technologies demonstrated BWs of up to 241 GHz [3]–[9]. These results stimulate integrated solutions for various applications, for example, in measurement and sensing equipment. Therefore, not only applications with a close to 200% relative BW can benefit from distributed topologies, but also for banded but still wideband systems, such as full waveguide bands, distributed approaches [10], [11] might be an attractive alternative to standard reactively matched components. However, further developments on several distributed building blocks are needed for integrated systems. Mixers are essential components to make the radio frequency (RF) signal available to baseband and intermediate frequency (IF) post-processing. Thus, mixer circuits with similarly high BWs as DAs are required.

TABLE I
State-of-the-Art DM MMICs

Ref.	BW (GHz)	CG (dB)	P_{LO} (dBm)	$IP_{1\,dB}$ (dBm)	$P_{dc,q}$ (mW)	Topology
[12]	0–194	−4.4–5.7	2	−8	125	up; fixed LO
[13]	0.8–77.5	−9–−4.4	10	−1.5	0	down; slid. LO
[15]	2–67	1.7–4.8	0	−7	17.5	down; slid. LO
[16]	5–45	−13.2–−11	8	n/a	1.4	down; slid. LO
[17]	4–41	3.5–8	10	n/a	100	down; slid. LO
[18]	3–40	3.1–4.1	5	n/a	n/a	down; slid. LO
This work	1–170	>−4.2	−1	−1.7	180	down; slid. LO

In literature, the largest RF BWs for mixers are demonstrated for an up-conversion mixer from 0 to 194 GHz with a fixed local oscillator (LO) frequency at 97.2 GHz [12]. However, for down-conversion mixers and mixers with a sliding LO, the reported BWs do not exceed 100 GHz [13]. In [14], a distributed mixer (DM) with a BW of 5–50 GHz using source-feedback mixer cells is published. Table I summarizes the state-of-the-art DM monolithic microwave integrated circuits (MMICs).

This work presents the design and characterization of distributed down-conversion mixer MMICs. The design targets a 170-GHz BW with an option to extend it to 300 GHz with future work. Therefore, this letter demonstrates a DM [MMIC1, see Fig. 1(a)] as a stand-alone circuit and integrated with a distributed LO driver amplifier [MMIC2, see Fig. 1(b)]. The RF input power for 1-dB gain compression ($IP_{1\,dB}$) should be as high as possible, whereas the required LO power (P_{LO}) for MMIC2 should not exceed 0 dBm. The letter is organized as follows: Section II discusses the design of the DM core including an investigation of the optimal gate width (W_g) for each transistor. Section III presents the on-wafer measurement results and Section IV concludes the letter and compares the results to the state of the art.

II. Distributed Down-Converter MMIC Design

The utilized mixer topology features a distributed concept. A simplified schematic of the mixer is illustrated in Fig. 1(c). The MMICs are designed and fabricated in a 35-nm gate-length metamorphic high-electron-mobility transistor (mHEMT) technology [19] and utilize thin-film microstrip transmission lines (TFMSLs) using the first metal

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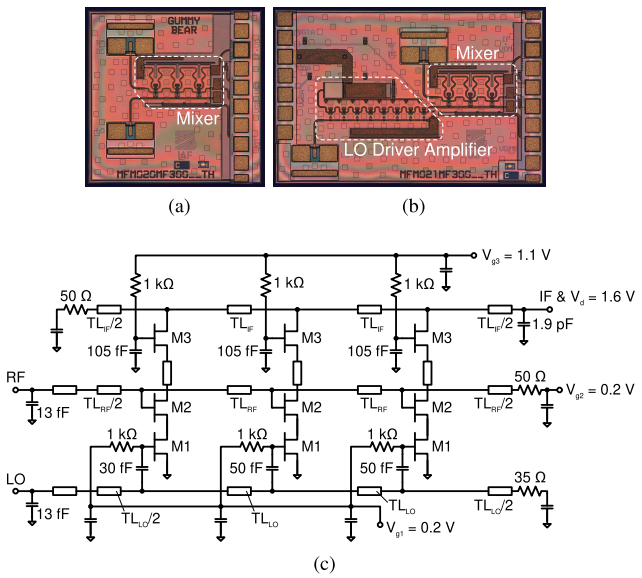

Fig. 1. Chip photographs of the fabricated MMICs with (a) MMIC1: the DM stand-alone and (b) MMIC2: including an integrated distributed LO driver amplifier. The total chip sizes are (a) 1×1 mm^2 and (b) 1.5×1 mm^2. Without RF and dc pads, the circuits occupy an area of (a) 500×260 μm^2 and (b) 1100×370 μm^2. (c) Simplified schematics of MMIC1.

layer as ground plane and the 2.7-μm-thick third metal as signal strips [1].

The unit cell (UC) is based on a source-feedback mixer, which consists, in general, of at least two transistors in a stacked configuration. The lower transistor (M1) operates in the ohmic region. The LO input signal switches M1 ON and OFF and by that modulates the source current of the upper transistor (M2). M2 is biased and operated in an amplifier mode (class AB bias). The RF input signal is injected at the gate of M2 so that M2 is in a common-source (CS) configuration. Occasionally, a third transistor (M3) is stacked on top of M2, mainly to increase CG. Consequently, the upper part of the DM (M2 and M3) can be understood as a DA with a modulated resistive source feedback, realized by M1.

An essential design step of an DM with source-feedback UCs are the gate widths of M1 ($W_{g,M1}$) and M2 ($W_{g,M23}$). Commonly, M3 uses as well $W_{g,M23}$ (due to a symmetric RF-cascode operation of M2 and M3). On the one hand, $W_{g,M1}$ should be considerably large since the ON-resistance of M1 ($R_{ON,M1}$) reduces the effective transconductance of M2 ($g_{m,M23}$). This can be seen by adopting the well-known relation of the intrinsic and extrinsic transconductance of a transistor

$$g_{m,M23} = \frac{g_{m,meas} \cdot W_{g,M23}}{1 + R_{ON,M1} \cdot g_{m,meas} \cdot W_{g,M23}}. \quad (1)$$

On the other hand, the input capacitance of M1 ($C_{in,M1}$) and by that $W_{g,M1}$ limits the achievable BW of this DM since, as it is the case for all distributed circuit topologies, $C_{in,M1}$ adds to an artificial LO transmission line (ATL_{LO}). Consequently, since $C_{in,M1}$ is the largest input capacitance out of the three transistors, the cut-off frequency of this ATL_{LO} limits the BW of this DM. Capacitive division with a series capacitor in front of M1 can help to increase $W_{g,M1}$ for a given BW or vice versa. However, even then the increase of $W_{g,M1}$ or BW runs into practical limitations since, in general, the design rules of minimal MIM capacitors will not allow to go below certain dimensions. Furthermore, reducing the series MIM capacitor more and more lowers as well the power reaching M1, which results in an increased required P_{LO}.

For determining $W_{g,M1}$ and $W_{g,M23}$, the decision criterion is the effective transition frequency (f_T) of M2 ($f_{T,M23}$) if M1 is used as resistive source feedback. This serves as a measure for the available gain of the DA part of the DM. Commonly, f_T as a function of W_g shows a drop toward a small W_g. This is due to a non-scaling capacitance (C_{pad}), whereas the major part of the gate–source capacitance (C_{gs}) scales linearly with W_g. The corresponding equation of the effective f_T of a CS transistor (neglecting C_{gd}) is given as

$$f_{T,eff} = \frac{1}{2\pi} \frac{g_m \cdot W_g}{C_{pad} + C_{gs} \cdot W_g} = \frac{1}{2\pi} \frac{g_m}{C_{gs}} \frac{W_g}{C_{pad}/C_{gs} + W_g} \quad (2)$$

where C_{gs} and the transconductance (g_m) are normalized to W_g. Since, due to the resistive source feedback, $R_{ON,M1}$ limits $g_{m,M23}$, $f_{T,M23}$ exhibits a local maximum. This can be shown by inserting (1) as g_m into (2)

$$f_{T,M23} = \frac{W_{g,M23}}{C_{pad}/C_{gs} + W_{g,M23}} \frac{f_T}{1 + R_{ON,M1} \cdot g_{m,meas} \cdot W_{g,M23}}. \quad (3)$$

Based on measured S-parameters of several two-finger transistors (bias: drain voltage 0.8 V and drain current 300 mA/mm), (2) is fit to the corresponding f_T values. Based on dc measurements at this bias, $g_{m,meas}$ is 2.1 S/mm. The extraction of the parameters of (2) results in a W_g-independent f_T of 412.5 GHz, a C_{gs} of 0.81 pF/mm, and a C_{pad} of 2.96 fF.

The effective input capacitance of the series connection of $C_{in,M1}$ and an MIM capacitor should be approx. 20 fF to enable a Bragg frequency of 300 GHz. When assuming a 50-fF MIM capacitor, the corresponding maximum $W_{g,M1}$ (based on the above-mentioned C_{gs}) is 2×20 μm. This is also the used value in this design. Based on an ON-resistance of the technology of 0.3 $\Omega \cdot$ mm, $R_{ON,M1}$ is 7.5 Ω. Thus, for this design, $f_{T,M23}$ versus $W_{g,M23}$ achieves a maximum at 15–16 μm. Consequently, M2 and M3 use a $W_{g,M23}$ of 2×8 μm.

The DM uses three UCs, which is a trade-off between a higher CG (for more UCs) and a reduced P_{LO} requirement (for fewer UCs). The series capacitor at the LO line of the first UC is reduced to 30 fF so that the transferred P_{LO} to all M1 transistors is approximately identical. The LO, RF, and IF transmission lines are designed in a conventional way to match the corresponding capacitance and to fulfill the synchronism of signals on the artificial RF, LO, and IF lines. The IF output is, in general, considerably wideband as well. However, since this work targets IFs in the range of only 0.1 GHz, a 1.9-pF capacitor is used to block LO and RF signals on the IF line, which improves the LO-to-IF and RF-to-IF isolation. The gate voltage of M2 is fed via the termination resistor of the RF line. For a flat CG down to low frequencies (LFs), the RF line requires an off-chip LF extension as it is described in [20].

A chip photograph of the fabricated MMIC1 (mixer stand-alone) is depicted in Fig. 1(a). MMIC2 includes the DM of MMIC1 and an LO driver amplifier, which is an available building block [1]. The amplifier is based on an eight-cell distributed circuit topology and provides sufficient power to drive the DM at least up to LO frequencies of 170 GHz. A chip photograph of MMIC2 is illustrated in Fig. 1(b).

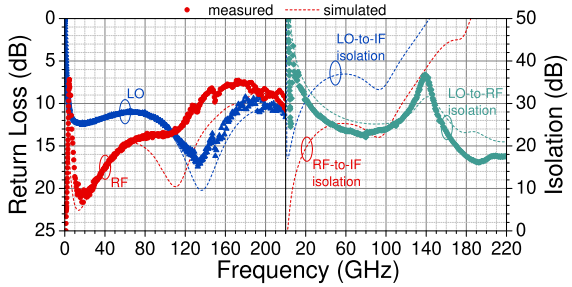

Fig. 2. MMIC1: (left) measured (symbols) and simulated (dashed lines) LO and RF input return loss at 50 Ω and (right) measured and simulated LO-to-RF, LO-to-IF, and RF-to-IF isolation versus operating frequency.

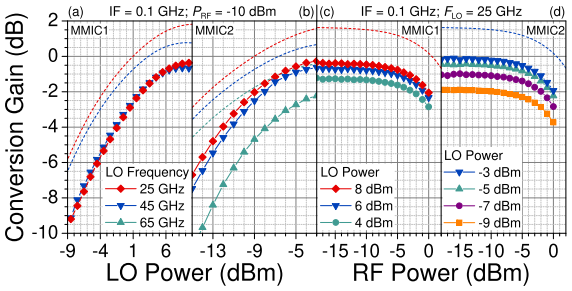

Fig. 3. Measured (symbols) and simulated (dashed lines) CG versus (a)–(b) P_{LO} and (c)–(d) P_{RF} of the presented mixer MMICs. (a) and (c), and (b) and (d) Performance of MMIC1 and MMIC2, respectively.

Simulations are shown and discussed together with the measurements in the following section.

III. Measurement Results

For all on-wafer measurements, the MMICs are biased identically [see Fig. 1(c)]. Under the LO drive, MMIC1 and MMIC2 have a total power consumption of 14.4 and 180 mW, respectively. The input return losses (RLs) at the RF and LO input ports of MMIC1 as well as the LO-to-RF isolation are characterized using an *S*-parameter setup. The corresponding measurements and simulations are depicted in Fig. 2. Up to 170 GHz, the RF and LO RLs are better than 7.8 and 11 dB, respectively. The LO-to-RF isolation is shown in the right graph of Fig. 2 and is better than 20 dB. Fig. 3(a) and (b) shows the CG versus P_{LO} at different frequencies. In saturation, both MMICs achieve a CG of about −0.5 dB at 25 and 45 GHz. Due to the integrated driver DA, MMIC2 requires roughly 9–10 dB less P_{LO} compared to MMIC1. This allows a P_{LO} of less than 0 dBm for MMIC2. In Fig. 4, CG is given versus RF for a fixed IF of 0.1 GHz as a comparison of (left) MMIC1 and (right) MMIC2. Both MMICs obtain a very similar response versus RF, just with a reduced P_{LO} for MMIC2. Furthermore, Figs. 3(c) and (d) and 4 illustrate a variable gain feature of the presented DM. By adjusting P_{LO}, the CG can be controlled without impacting the CG response versus RF. In context to this feature, the measured CG versus RF input power (P_{RF}) is important since for several mixer topologies reducing P_{LO} results also in a degraded compression behavior versus P_{RF}. However, as Fig. 3(c) and (d) illustrates for both MMICs, the measured CG is independent of the available P_{LO} and shows a $IP_{1\,dB}$ of −1.7 dBm. In Fig. 5, the CG is measured for an RF range of up to 220 GHz for a constant P_{LO} and IF of −1 dBm and

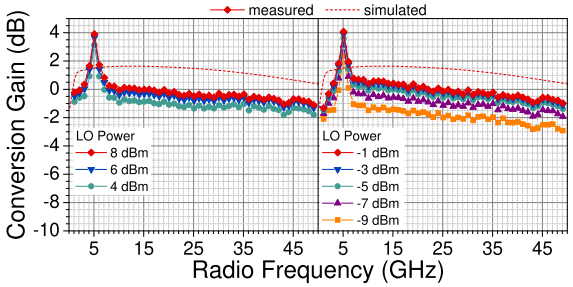

Fig. 4. Measured (symbols) and simulated (dashed lines) CG versus RF of the presented mixer MMICs for different levels of P_{LO}. The IF and P_{RF} are 0.1 GHz and −10 dBm, respectively. The left and right graphs show the performance of MMIC1 and MMIC2, respectively.

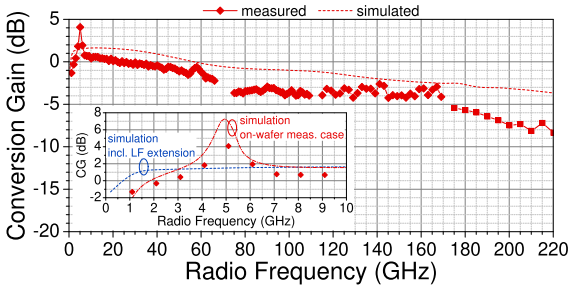

Fig. 5. Measured (symbols) and simulated (dashed lines) CG versus RF of MMIC2 up to 220 GHz. The IF, P_{LO}, and P_{RF} are 0.1 GHz, −1, and −10 dBm, respectively. The inset shows a close up of the CG for an RF from 0 to 10 GHz including an LF extension at the V_{g2} port (blue dashed line) and a simulation of the on-wafer case (red dotted-dashed line).

0.1 GHz, respectively. Up to 170 GHz, the CG is in the range of −4.2 to 1 dB and follows the prediction with only a slight offset, which is expected to originate from an underestimated R_{ON} in the used transistor model. Above 170 GHz, MMIC2 is still functional and provides good performance. However, a dropping slope of CG can be observed, which is mainly caused by a limited P_{LO} to fully saturate the DM for the higher frequencies. The peak in the CG at 5 GHz originates from an interaction with the dc probe, which is only used in the on-wafer measurement. In an assembled situation, a flat CG can be achieved. The inset in Fig. 5 shows the comparison of the simulated and measured CG below 10 GHz in the on-wafer measurement case and the simulation including an LF extension as it would be used in an assembly.

IV. Conclusion

This letter presents distributed down-conversion mixer MMICs with a 1–170-GHz BW and a measured CG of better than −4.2 dB for a fixed IF of 0.1 GHz. Up to 220 GHz, the CG is still above −8.3 dB. The mixer core consists of three source-feedback mixer cells in a distributed topology. Including an eight-cell DA, MMIC2 requires a P_{LO} of only −1 dBm. $IP_{1\,dB}$ is −1.7 dBm and is independent of the provided P_{LO}. Thus, CG can be adjusted by tuning P_{LO}. This variable CG feature, without P_{LO} affecting $IP_{1\,dB}$, demonstrates a beneficial characteristic of the presented down-conversion mixer MMICs for a multitude of applications. Table I compares this work to state-of-the-art DM MMICs. To the best of the authors' knowledge, this work demonstrates the largest BW for DM MMICs with a sliding LO and for down-conversion DM MMICs.

REFERENCES

[1] F. Thome and A. Leuther, "First demonstration of distributed amplifier MMICs with more than 300-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2647–2655, Sep. 2021, doi: 10.1109/JSSC.2021.3052952.

[2] F. Thome and A. Leuther, "A 75–305-GHz power amplifier MMIC with 10–14.9-dBm pout in a 35-nm InGaAs mHEMT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 741–743, Jun. 2021, doi: 10.1109/LMWC.2021.3058101.

[3] T. Jyo *et al.*, "A 241-GHz-bandwidth distributed amplifier with 10-dBm P1dB in 0.25-μm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1430–1433, doi: 10.1109/MWSYM.2019.8700975.

[4] K. Eriksson, I. Darwazeh, and H. Zirath, "InP DHBT distributed amplifiers with up to 235-GHz bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1334–1341, Apr. 2015, doi: 10.1109/TMTT.2015.2405916.

[5] S. Yoon, I. Lee, M. Urteaga, M. Kim, and S. Jeon, "A fully-integrated 40–222 GHz InP HBT distributed amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 460–462, Jul. 2014, doi: 10.1109/LMWC.2014.2316223.

[6] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "A trimmable cascaded distributed amplifier with 1.6 THz gain-bandwidth product," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 6, pp. 1094–1096, Nov. 2015, doi: 10.1109/TTHZ.2015.2482940.

[7] T. Shivan *et al.*, "Performance analysis of a low-noise, highly linear distributed amplifier in 500-nm InP/InGaAs DHBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5139–5147, Dec. 2019, doi: 10.1109/TMTT.2019.2947664.

[8] N. L. K. Nguyen, D. P. Nguyen, A. N. Stameroff, and A.-V. Pham, "A 1–160-GHz InP distributed amplifier using 3-D interdigital capacitors," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 5, pp. 492–495, May 2020, doi: 10.1109/LMWC.2020.2980280.

[9] F. Thome and O. Ambacher, "A 50-nm gate-length metamorphic HEMT distributed power amplifier MMIC based on stacked-HEMT unit cells," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1695–1698, doi: 10.1109/MWSYM.2017.8058967.

[10] O. S. A. Tang and C. S. Aitchison, "A microwave distributed MESFET mixer," in *Proc. 14th Eur. Microw. Conf.*, Oct. 1984, pp. 483–487, doi: 10.1109/EUMA.1984.333361.

[11] O. S. A. Tang and C. S. Aitchison, "A very wide-band microwave MESFET mixer using the distributed mixing principle," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-33, no. 12, pp. 1470–1478, Dec. 1985, doi: 10.1109/TMTT.1985.1133242.

[12] T. Jyo *et al.*, "A DC to 194-GHz distributed mixer in 250-nm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 771–774, doi: 10.1109/IMS30576.2020.9223832.

[13] H.-Y. Yang *et al.*, "Design and analysis of a 0.8–77.5-GHz ultra-broadband distributed drain mixer using 0.13-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 3, pp. 562–572, Mar. 2009.

[14] I. Kallfass, T. Purtova, A. Brokmeier, W. Ludwig, and H. Schumacher, "One single travelling-wave MMIC for highly linear broadband mixers and variable gain amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 97–100, doi: 10.1109/MWSYM.2005.1516530.

[15] Y.-C. Liu, Y.-W. Chang, Y.-C. Yeh, S.-H. Weng, J.-H. Tsai, and H.-Y. Chang, "A 2-to-67 GHz 0-dBm LO power broadband distributed NMOS-HBT Darlington mixer in 0.18 μm SiGe process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540371.

[16] Y.-S. Lin, C.-L. Lu, and Y.-H. Wang, "A 5 to 45 GHz distributed mixer with cascoded complementary switching pairs," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 9, pp. 495–497, Sep. 2013, doi: 10.1109/LMWC.2013.2274992.

[17] F.-C. Chang, P.-S. Wu, M.-F. Lei, and H. Wang, "A 4–41 GHz singly balanced distributed mixer using GaAs pHEMT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 2, pp. 136–138, Feb. 2007, doi: 10.1109/LMWC.2006.890341.

[18] W. Ko and Y. Kwon, "A GaAs-based 3–40 GHz distributed mixer with cascode FET cells," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2004, pp. 413–416, doi: 10.1109/RFIC.2004.1320638.

[19] A. Leuther, A. Tessmann, M. Dammann, H. Massler, M. Schlechtweg, and O. Ambacher, "35 nm mHEMT technology for THz and ultra low noise applications," in *Proc. Int. Conf. Indium Phosph. Rel. Mater.*, May 2013, pp. 1–2, doi: 10.1109/ICIPRM.2013.6562647.

[20] *GaAs MMIC TWA Users Guide (5991-3545EN)*, Keysight Technol., Santa Rosa, CA, USA, Aug. 2014.