High-Gain 670-GHz Amplifier Circuits in InGaAs-on-Insulator HEMT Technology

Laurenz John, Axel Tessmann, Arnulf Leuther, Thomas Merkle, Hermann Massler, and Sébastien Chartier

***Abstract*— In this letter, we report on the development of high-gain WR-1.5 amplifier circuits, utilizing a transferred-substrate InGaAs-on-insulator (InGaAs-OI) high-electron-mobility transistor (HEMT) technology on Si with 20-nm gate length. A six-stage and a nine-stage amplifier circuit are described, which are based on gain cells in cascode configuration. With more than 30 dB of measured gain in the frequency band of 660–700 GHz, the highest frequency of operation of transferred-substrate THz amplifiers is reported. These gain levels in excess of 30 dB, furthermore, correspond to the highest reported gain values and state-of-the-art performance around the targeted 670-GHz frequency band.**

***Index Terms*— Amplifiers, high-electron-mobility transistor (HEMT), InGaAs-on-insulator (InGaAs-OI), silicon, THz.**

I. Introduction

OVER the last decade, high-electron-mobility transistor (HEMT) technologies have demonstrated THz monolithic integrated circuits (TMICs) with high gain and state-of-the-art noise figures at the sub-mm-wave frequency range above 500 GHz [1], [2]. In particular, the frequency band around 670 GHz has been addressed with InP HEMT-based low-noise amplifiers (LNAs) [3] for the integration in radiometer and imaging systems, such as direct-detection receivers for weather satellite applications [4].

This letter describes the development of 670-GHz amplifier circuits that are realized in a 20-nm InGaAs-on-Insulator (InGaAs-OI) HEMT technology, including the transfer to a Silicon substrate after the epitaxial growth of the InGaAs-channel HEMT structure [5]. Previously reported transferred-substrate TMIC amplifiers have demonstrated up to 19 dB of gain around 570 GHz, using a 200-nm InP HBT technology on SiC [6]. By using SiC substrates, improved heat dissipation and increased operating frequencies are targeted in [6]. In this work, on the other hand, the motivation for the transfer of the HEMT devices from the GaAs to a Si substrate is the improvement of single-device dc as well as RF characteristics. This includes an improved pinch-off behavior as well as enhanced device figures such as breakdown voltage, intrinsic gain, and cutoff frequencies. Furthermore, short-channel effects such as drain-induced barrier lowering are possibly reduced and the III-V compound semiconductor material content is cut down by a factor of 10^6 [5].

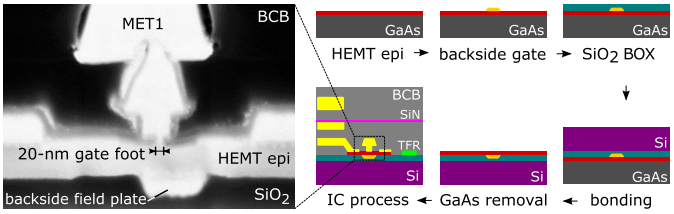

Fig. 1. Process sequence of the InGaAs-OI HEMT technology and SEM image of a 20-nm HEMT device with backside field plate.

Two transferred-substrate TMIC amplifiers are reported, based on devices in cascode configuration. More than 30 dB of gain is measured around 670 GHz, implementing up to nine cascode gain stages. Thus, with an operation frequency in the range of 660–710 GHz, we report the first TMIC amplifiers on a transferred substrate that are operating above 600 GHz.

II. Technology

The TMIC amplifiers described in this letter are implemented in an advanced transferred-substrate InGaAs-channel HEMT technology with 20-nm gate length [5]. The inverted HEMT heterostructure is grown by molecular beam epitaxy (MBE) on 100-mm semi-isolating GaAs wafers and transferred to silicon substrates by using a SiO_2-based wafer bond process with subsequent wafer thinning and removal of the GaAs substrate (see Fig. 1). Thus, only a 100-nm-thick III-V heterostructure layer is remaining on the Si substrate. This advanced transferred-substrate technology also offers the implementation of HEMT devices with backside gate or field plate [5]. This feature, however, is not utilized in the circuits described in this work.

The 20-nm InGaAs-OI HEMT technology features typical values for the OFF-state breakdown voltage and maximum drain-current density of 5 V and 1200 mA/mm, respectively, while achieving a maximum transconductance of 2400 mS/mm. The expected cutoff frequency values f_T and f_{max} are above 500 GHz and 1 THz, respectively.

A fully passivated back-end-of-line (BEOL) process is used, including three metal layers (MET1–MET3), a NiCr 50-Ω/□ thin-film-resistor (TFR) layer, as well as an SiN layer for the implementation of MIM capacitors between MET2 and MET3. Using the lowest metal layer (MET1) as substrate shielding

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The authors are with the Fraunhofer Institute for Applied Solid State Physics (Fraunhofer IAF), 79108 Freiburg im Breisgau, Germany (e-mail: laurenz.john@iaf.fraunhofer.de; axel.tessmann@iaf.fraunhofer.de; arnulf.leuther@iaf.fraunhofer.de; thomas.merkle@iaf.fraunhofer.de; hermann.massler@iaf.fraunhofer.de; sebastien.chartier@iaf.fraunhofer.de).

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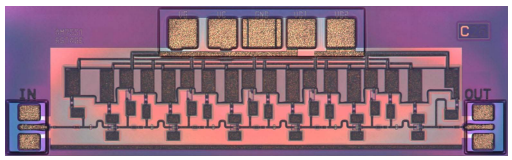


Fig. 2. Chip photograph of a six-stage TMIC amplifier with cascode gain stages. The chip dimensions are 350 μm $\times$ 1250 μm, including dc and RF pads.

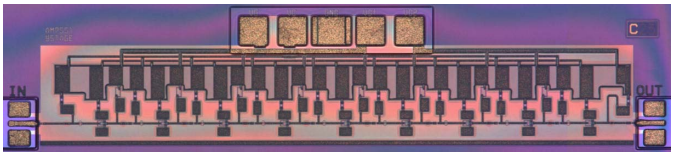


Fig. 3. Chip photograph of a nine-stage TMIC amplifier with cascode gain stages. The chip dimensions are 350 μm $\times$ 1700 μm, including dc and RF pads.

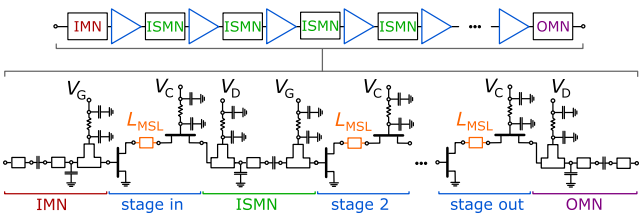
dc and RF ground, thin-film-microstrip lines (TFMSLs) with a MET2 and MET3 signal line are utilized for the routing of the matching and bias insertion networks, independent of the Si substrate. A more detailed description of the BEOL process and possible layer configurations for compact TFMSL networks are, furthermore, given in [7] and [8].

III. 670-GHz TMIC Amplifiers

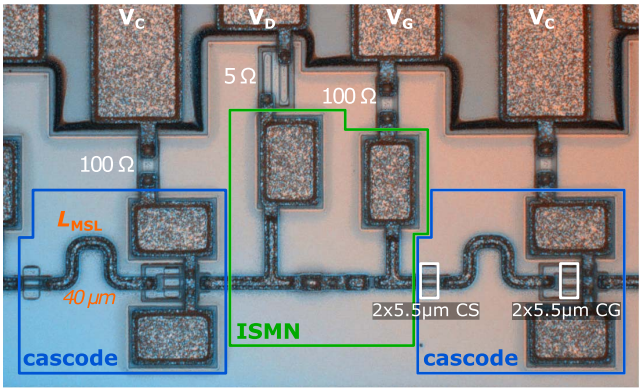
The chip photographs of two TMIC amplifiers with six and nine gain stages—which have been designed for the frequency range around 670 GHz, based on the design considerations discussed in [9]—are depicted in Figs. 2 and 3, respectively. The chip width of the amplifier circuits is 350 μm and the chip length of the TMICs is 1250 and 1700 μm, respectively.

To maximize the achievable small-signal gain per stage, the amplification stages of both amplifier circuits are implemented with two transistors in cascode configuration. The corresponding simplified circuit schematic of the amplifiers is depicted in Fig. 4(a), whereas Fig. 4(b) shows the close-up view of two cascaded stages with interstage matching network (ISMN). Both cascode amplifiers are implemented with TFMSL wiring and identical matching networks. In case of the six-stage TMIC amplifier, 2 $\times$ 5.5-μm two-finger common–source (CS) and common–gate (CG) HEMT devices are used. The nine-stage circuit, on the other hand, is implemented with a slightly larger gate width of 2 $\times$ 6-μm.

Besides the different transistor-finger width and number of stages, the main difference between the two TMIC amplifiers is the length of the TFMSL interconnection, which is connecting the CS and CG transistors in the cascode configuration. The length—or series inductance L_{MSL}—of this transmission line, significantly affects the maximum achievable (stable) gain of the cascode configuration at sub-mm-wave frequencies, as discussed for the THz cascode devices in [9] and [10]. To compensate the de-tuning of the respective source and load impedances between the CS and CG devices with increasing frequency, a transmission line with a length of at least 20 μm is required at 670 GHz. Thus, the six-stage amplifier variant is implemented with a meandered 40-μm long 50-Ω TFMSL between the CS and CG devices, as can be seen in Figs. 2 and 4(b). The nine-stage amplifier variant,



(a)



(b)

Fig. 4. (a) Schematic of the amplifiers with six or nine gain stages in cascode configuration. (b) Close-up view of two cascaded gain stages in cascode configuration. The depicted cascode cells, with 40-μm TFMSL between 2 $\times$ 5.5-μm transistors, are implemented in the six-stage amplifier (see Fig. 2). The nine-stage circuit uses a 30-μm TFMSL and 2 $\times$ 6-μm transistors (see Fig. 3).

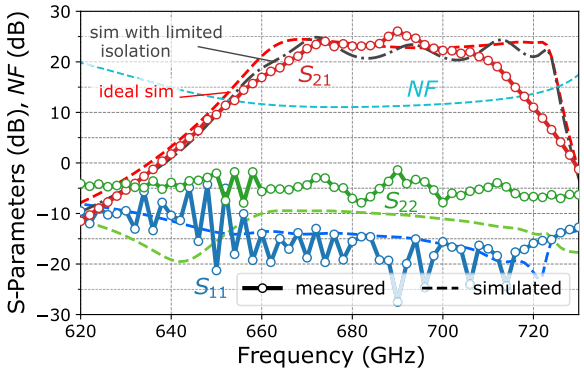
on the other hand, is realized with a straight 30-μm thin-film line between the CS and CG devices, as visualized in Fig. 3. Similar inductive series networks are commonly used in stacked power amplifier topologies and high-gain cascode circuits at mm-wave frequencies [11].

All matching networks and TFMSL components that are depicted in Fig. 4(b) have been designed using fully electromagnetic (EM)-simulated 3-D models that have been implemented in CST Microwave Studio. This is done to accurately describe the compact impedance-transformation networks. Only the two-finger CS and CG transistor structures, which are highlighted in Fig. 4(b), are described and simulated with standard process design kit (PDK) models in Keysight's Advanced Design System (ADS) as discussed in [12] and [13]. The measurement results of the 670-GHz TMIC amplifiers are described in the following.

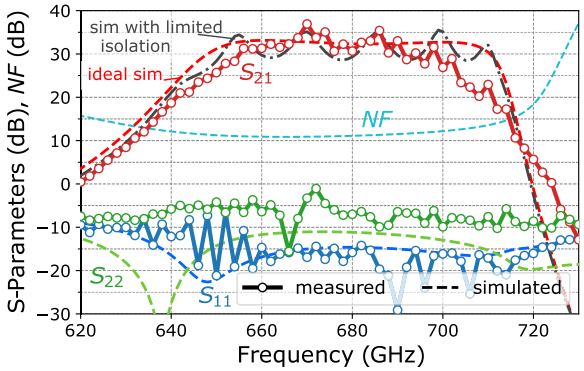
IV. Measurement Results

The WR-1.5 on-wafer S-parameter characterization was done using a Keysight N5224B PNA system and Virginia Diodes, Inc. (VDI) extension modules. The setup was calibrated to the probe tip of the RF-probes by performing a thru-reflect-line (TRL) calibration, using an impedance standard substrate (ISS).

The S-parameter characteristics of the six-stage and nine-stage TMIC amplifiers in the frequency band from 620 to 730 GHz are depicted in Fig. 5. During the on-wafer characterization, the HEMT devices in cascode configuration have been biased at V_D = 2 V (1-V drain–source voltage per device) and 350 mA/mm. Hence, at 2 V and 23 mA, the



(a)



(b)

Fig. 5. S-parameter data and noise figure of (a) six-stage cascode TMIC and (b) nine-stage cascode TMIC. Depicted are the measured (–○–) and simulated (– – –) characteristics of the amplifiers. In addition to the ideal S-parameter simulation data, the simulated S_{21} data for limited output-to-input isolation is depicted (–·–), which is considering the coupling between the input and output port (RF probes).

overall dc-power consumption of the six-stage TMIC amplifier is 46 mW. The required dc power of the nine-stage circuit, on the other hand, is 76 mW—biased at 2 V and 38 mA.

As visualized in Fig. 5(a), the measured small-signal gain of the six-stage cascode TMIC amplifier is in the range of 22–25 dB over the frequency range from 670 to above 700 GHz. This corresponds to 4 dB of gain per cascode stage around the targeted 670-GHz frequency range. The nine-stage TMIC amplifier, on the other hand, achieves at least 30 dB of measured gain from 660 to roughly 700 GHz, which corresponds to a gain per stage below 4 dB. This reduced gain is mainly due to the shorter transmission line of 30 μm in the cascode cells that are implemented in the nine-stage TMIC amplifier, as discussed above. Due to the longer connecting line of 40 μm, the CS and CG devices are matched closer to the respective load- and source-stability circles in the case of the six-stage TMIC amplifier, resulting in a higher gain per cascode cell.

The simulation data shown in Fig. 5 is considering the ideal circuit behavior. To account for the impact of the on-wafer measurement environment, additional data of the simulated S_{21} is shown, which is considering the limited isolation between the output and input port. In simulation, the magnitude of the S_{12} parameter is below −70 dB for the six-stage amplifier and below −110 dB for the nine-stage amplifier, respectively. The measured S_{12}, however, is above −50 dB, resulting in the periodic gain ripple that is observed in the small-signal

TABLE I

COMPARISON OF REPORTED TMIC AMPLIFIERS AROUND 670 GHz

Ref.	Technology	Topology	P_{DC} (mW)	Gain (dB)	Frequency (GHz)
[14]	130-nm InP HBT	9-stage common-base	126	20–22	580–680
[1]	30-nm InP HEMT	10-stage common-source	78	26–30	610–690
[15]	25-nm InP HEMT	10-stage common-source	–	23–29	650–710
[16]	35-nm InGaAs mHEMT	10-stage common-source	25	12–15	660–750
[9]	35-nm InGaAs mHEMT	6-stage cascode	40	25–30	630–690
this work	20-nm InGaAs-OI HEMT	9-stage cascode	76	30–33	660–700

gain of the TMIC amplifiers. By also considering the limited isolation in simulation, the measured S_{21} behavior is described to a very good extend. Only the upper band edge is too optimistically assumed in simulation. Hence, judging from the data of the ideal simulation model, a flat 33-dB gain response is expected for the nine-stage TMIC over the frequency range of 660–700 GHz.

The coupling between the input and output ports is considered in ADS using a variable S-parameter two-port component in parallel to the TMIC simulation model. Using this simple model, the simulated S_{12} magnitude is adjusted to the measured levels above −50 dB and the time delay that can be calculated from the distance between the RF pads is implemented. Yet, since S_{12} values below −60 dB are typically achieved for packaged TMIC amplifiers, an improved gain flatness is expected after assembly [2].

V. DISCUSSION AND CONCLUSION

In this letter, we describe the implementation of high-gain 670-GHz TMIC amplifiers. The circuits are realized in a transferred-substrate 20-nm InGaAs-OI HEMT technology on Si, achieving more than 30 dB of measured gain in the frequency band from 660 to roughly 700 GHz. This is the first time that amplifiers above 600 GHz are reported, which are designed utilizing a transferred-substrate technology.

The expected power density on transistor level is at least 100 mW per 1-mm gate width. Therefore, the predicted output-power level of the reported TMIC amplifiers at 5-dB gain compression ($OP_{5\,dB}$) is around 0.5–0.6 mW (50 mW/mm) on circuit level. Table I, furthermore, shows a comparison of high-gain TMIC amplifier results around 670 GHz, based on different III-V transistor technologies. In comparison to similar 670-GHz cascode circuits in our standard 35-nm mHEMT technology [9], which is processed on GaAs substrate, less amplification per cascode stage is achieved. Thus, with NF values around 11 dB, the simulated noise figure is slightly above the 35-nm mHEMT simulation results reported in [9]. However, with gain levels in excess of 30 dB, state-of-the-art small-signal gain is achieved in this frequency range. Hence, the transferred-substrate HEMT technology demonstrates the potential for the realization of high-gain LNA TMICs around and above 700 GHz.

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