An 820-GHz Down-Converter With Fourth Subharmonic Mixer in 40-nm CMOS Technology

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***Abstract*— In this letter, an 820-GHz down-converter based on the subharmonic mixer and low noise amplifier (LNA) with low conversion loss and noise figure is proposed. To reduce the frequency of local oscillation (LO) signal, a fourth subharmonic architecture is adopted for the mixer implementation. Meanwhile, to improve the isolation of the mixer, a low-loss matching network based on λ/4 resonators with ground shields is introduced in the terahertz (THz) signal path. Then, the four-stage common-source LNA is utilized to amplify the down-conversion IF signal. Using conventional 40-nm CMOS technology, the implemented THz down-converter exhibits 9.9-dB conversion loss and 39.2-dB noise figure with −6-dBm LO input power at 820 GHz. The core chip occupies only 0.74 × 0.25 mm^2 while dissipating 28.6 mW from a 1.1-V voltage supply.**

***Index Terms*— CMOS, down-converter, low noise amplifier (LNA), subharmonic mixer, terahertz (THz).**

I. Introduction

TERAHERTZ (THz) bands are promising for the imaging, remote sensing, and radio astronomy applications [1]–[3], which require THz down-converters and mixers with low noise figures and conversion loss. Due to the high performance of Schottky diodes at THz frequency, the Schottky-based THz mixers with high metrics are widely utilized in size-easing systems [4]–[8]. However, the integration level is still not suitable for size-constraint applications, especially for THz complex systems. Then, to decrease the size, integrated circuit mixers and down-converters based on CMOS [9]–[15] and SiGe [16]–[21] technologies are introduced. In these technologies, the operation frequency of a mixer is usually higher than the cutoff frequency of devices. Thus, the passive mixing architecture is utilized. Meanwhile, the subharmonic mixing architecture is adopted to decrease the frequency of local oscillation (LO) signals, especially at high mixing frequencies. Then, a high-power LO signal is required for an acceptable conversion loss. Thus, the design of a compact THz down-converter based on silicon technology with low conversion loss and noise figure under low LO signal input power remains a great challenge.

In this letter, a compact 820-GHz down-converter is proposed for the THz application. The down-converter is mainly composed of a fourth subharmonic mixer and a four-stage low noise amplifier (LNA). A single MOSFET under a linear region is utilized to achieve the core mixer. THz and LO signals are injected into the source and gate terminals of the MOSFET, respectively. To improve the isolation and keep the ground connection, two λ/4 resonators are introduced in the THz path. Then, the down-conversion IF signal is generated at the drain terminal. Meanwhile, the IF signal is amplified by the four-stage LNA for low conversion loss. Inductors and capacitors are utilized for the impedance matching among the LNA stages. The implemented THz down-converter based on a conventional 40-nm CMOS technology exhibits low conversion loss and noise figure with low LO signal input power.

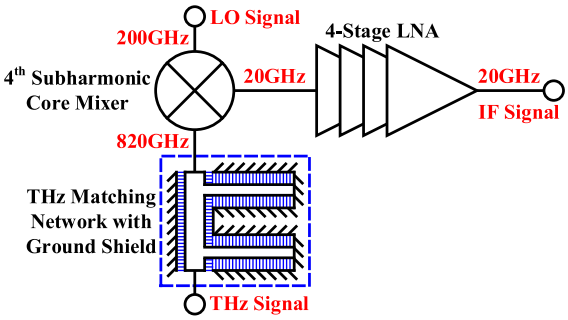

Fig. 1. Block diagram of the proposed THz down-converter.

II. Schematic and Operation

Fig. 1 shows the block diagram of the proposed THz down-converter, which consists of three parts: a fourth subharmonic core mixer, a THz matching network, and a four-stage LNA circuit. The THz and LO signals are fed to the core mixer circuit to generate the down-conversion IF signal. Then, the IF signal is amplified by the four-stage LNA circuit. The detailed mechanisms are investigated as follows.

A. Fourth Subharmonic Mixer

1) Core Mixer: The fundamental mixing architecture shows the lowest conversion loss in mixer-first design. However, the output power of the available 800-GHz LO signal is low (around −10 dBm), which is insufficient to drive the THz mixer. Thus, a fourth subharmonic mixing architecture is chosen in this work. The circuit schematic of the fourth subharmonic mixer is shown in Fig. 2. A single MOSFET M_1 with the optimized size is utilized to implement the core mixer for low parasitism. The THz signal (820 GHz)

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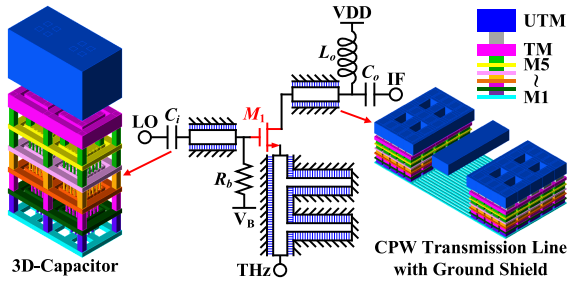

Fig. 2. Circuit schematic of the fourth subharmonic mixer (design parameters: M_1: 7.5 μm/40 nm and L_o: 920 pH).

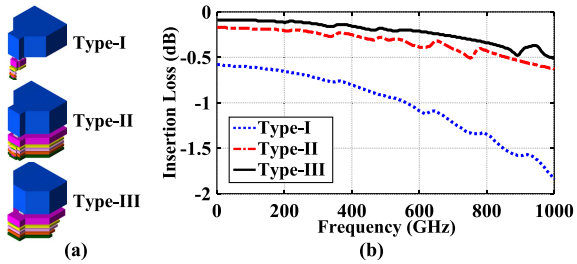

Fig. 3. (a) Configurations of the three types of terminal interconnections. (b) Simulated results.

is injected into the source terminal of M_1 through a low loss matching network. Meanwhile, the LO signal (200 GHz) is injected into the gate terminal of M_1. Ground shields using the metal M1 are introduced under the coplanar waveguide (CPW) transmission line of THz and LO paths to decrease the loss from the substrate and coupling effect. A bias voltage is set at the gate terminal through a poly resistor (i.e., R_b) to keep the MOSFET working in a linear region. In addition, a 3-D-capacitor (i.e., C_i) [22] with a value of 9.9 fF and quality factor of 99 at 200 GHz is utilized in the LO path for dc-block. Then, the IF signal (20 GHz) is generated at the drain terminal and filtered by an inductor-and-capacitor matching network (i.e., L_o and C_o). Three types of terminal interconnection for the MOSFET are investigated, as shown in Fig. 3. To decrease the parasitic capacitor between metal and ground, the smallest metal meeting the process design kit (PDK) design rule is utilized (i.e., Type-I). However, a large ohmic loss exists, which would cause a high insertion loss. Then, the regular interconnection with identical-size metal (i.e., Type-II) is introduced to decrease the ohmic loss. Nevertheless, the parasitic capacitor would increase. Thus, the interconnection considering the tradeoff among parasitic resistor, inductor, and capacitor (i.e., Type-III) features the lowest insertion loss.

2) Low Loss THz Matching Network: To improve the isolation between the THz and LO/IF terminals and keep the ground connection of the source terminal, a low loss matching network is introduced in the THz path. The 3-D-view of the matching network is shown in Fig. 4(a). To reduce the THz signal to ground, two CPW shorted stubs are utilized for the matching network. The equivalent transmission-line model is depicted in Fig. 4(b). To achieve low loss at 820 GHz and high suppression at 200 and 20 GHz, respectively, the electronic lengths of the CPW shorted stubs (i.e., θ_1) are designed as

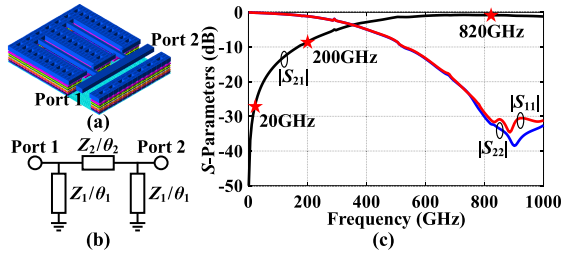

Fig. 4. (a) Configurations of the low loss THz matching network. (b) Transmission-line model. (c) Simulated results.

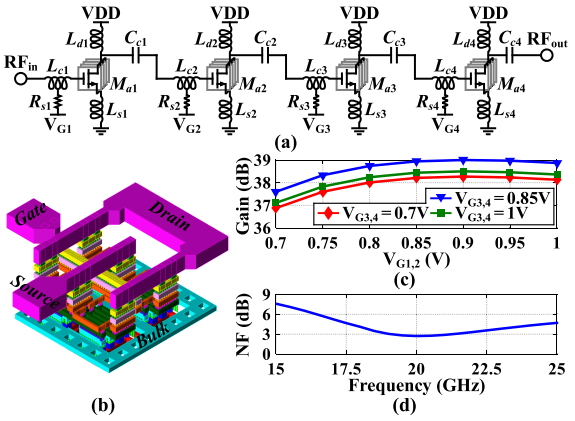

Fig. 5. (a) Schematic of the four-stage LNA. (b) Configurations of the core nMOS transistor. (c) Simulated gain results at 20 GHz. (d) Simulated noise figure under peak gain. (Design parameters: M_{a1}: 5 μm/40 nm × 4, $M_{a2,3}$: 6.25 μm/40 nm × 4, M_{a4}: 7.5 μm/40 nm × 4, $L_{d1,2,3,4}$: 465 pH, $L_{s1,2,3,4}$: 70 pH, $L_{c1,3}$: 480 pH, L_{c2}: 760 pH, and L_{c4}: 380 pH).

90° at 820 GHz. The electronic length of the connection line (i.e., θ_2) is optimized as 50° at 820 GHz to enhance the operational bandwidth and avoid the influence of frequency shift in practical implementation. The impedances of the stubs and connection line (i.e., Z_1 and Z_2) are both 50 Ω. The layout is simulated in a 2.5-D electromagnetic (EM) solver environment of Advanced Design System (ADS) momentum. The postlayout simulation, shown in Fig. 4(c), exhibits that the insertion loss and suppression levels are 0.8 and 8.4 dB/27.3 dB at 820 and 200 GHz/20 GHz, respectively.

B. Four-Stage LNA

To decrease the conversion loss of the down-converter, a four-stage LNA is utilized, as shown in Fig. 5(a). The common-source architecture with high power gain is adopted in LNA implementation. The transistor is constructed using 2 × 2 parallel nMOS transistors, whose 3-D-view is shown in Fig. 5(b). The gate resistance could be decreased by four gates connecting together. Inductors and metal-oxide-metal (MOM) capacitors are utilized for the input–output, and interstage impedance matching networks. Meanwhile, the inductors (i.e., L_s) are introduced in the source terminal of transistors to optimize the noise and power linearity [23]. Four bias voltages are supplied through the poly resistors (i.e., R_s). The postsimulation results, depicted in Fig. 5(c), exhibit the relationship between power gain and bias voltages at 20 GHz. The variation of bias voltages has a small influence on the power gain. Besides, the simulated noise figure is 2.7 dB at 20 GHz.

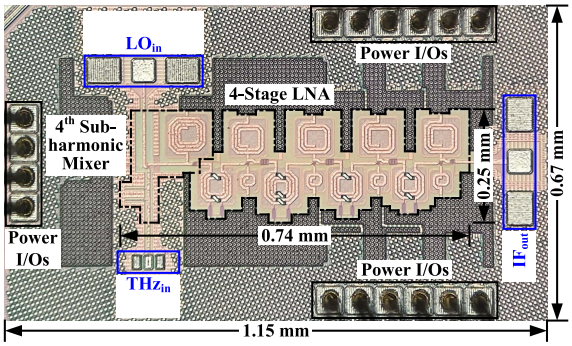

Fig. 6. Chip microphotograph of the proposed THz down-converter.

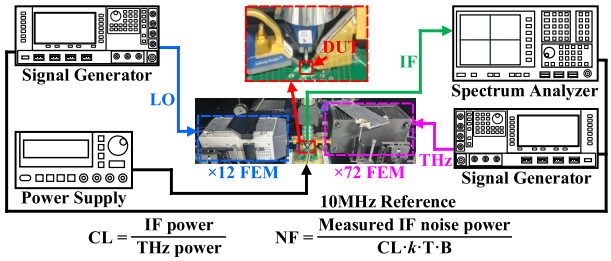

Fig. 7. Measurement setup.

III. Fabrication and Measurement

Based on the mechanisms mentioned above, a compact THz down-converter is implemented and fabricated in 40-nm CMOS technology. The microphotograph of the chip is shown in Fig. 6. The total chip size is 1.15×0.67 mm^2 including all pads, while the core size is only 0.74×0.25 mm^2. The measurement setup is shown in Fig. 7. The chip is mounted on a printed circuit board (PCB) for dc biasing and power supply. The THz and LO signals are injected into the chip through two ground-signal-ground (GSG) probes. Meanwhile, the THz and LO signals (i.e., 820 and 200 GHz) are generated by the microwave signal generators with $\times$ 72 and $\times$ 12 frequency extension modules (FEMs), respectively. IF signal (i.e., 20 GHz) is measured by the spectrum analyzer through a GSG probe. All the losses of the probes, waveguide, and cables are deembedded from the measurement results. The conversion loss and noise figure are estimated by the methods introduced in the work [15].

The maximum output power of the 200-GHz LO FEM is -2 dBm. Considering the loss of the waveguide connector and GSG probe (i.e., 1.5 and 2.5 dB, respectively), the maximum input LO signal power for the down-converter is -6 dBm. The simulated and measured conversion loss and noise figure of the down-converter are shown in Fig. 8. The measured conversion loss is 9.9 dB at 820 GHz, while the conversion loss is 9.9–11.4 dB from 800 to 840 GHz with a fixed 20-GHz IF signal. The measured noise figure is 38.8–47.5 dB from 800 to 840 GHz. Meanwhile, the influence of bias voltages of core mixer V_B and LNA V_G on the conversion loss is depicted in Fig. 9. It is notable that the bias voltage V_B has a great influence on the conversion loss, while V_G has a small influence. The overall power consumption of the down-converter is 28.6 mW from a 1.1-V voltage supply. Table I summarizes and compares the performance of the proposed THz down-converter with the state-of-the-arts. It is notable that the proposed down-converter with a subharmonic mixer features low conversion loss and noise figure with low LO input power.

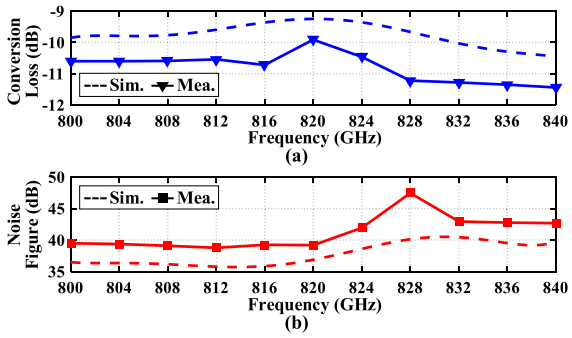

Fig. 8. Simulated and measured (a) conversion loss and (b) noise figure versus frequency.

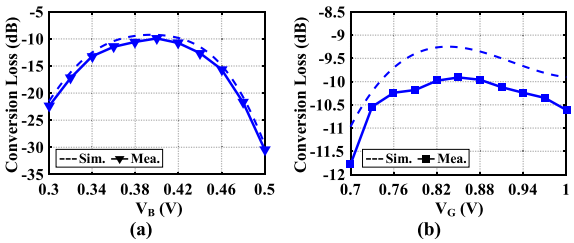

Fig. 9. Simulated and measured conversion losses versus (a) bias voltages of core mixer V_B and (b) LNA V_G($V_{G1,2,3,4} = V_G$).

TABLE I
Comparisons With the State-of-the-Arts

Ref.	**This work**	[15]	[18]	[16]	[14]	[13]
Technology	**40-nm CMOS**	65-nm CMOS	250-nm SiGe	130-nm SiGe	65-nm CMOS	65-nm CMOS
RF (GHz)	**820**	810	820	650	490	426
LO (GHz)	**200**	131.6	164	162.5	245	142.2
Mixing Order	**4**	6	5	4	2	3
P_{LO} (dBm)	**–6**	14	—	–18⋆	–3	—
CL* (dB)	**9.9#**	25#	18	13	—	38.3
NF** (dB)	**39.2**	45	45	42	25.8**	54.3
Consumption (mW)	**28.6**	—	—	433	26	69
Size (mm^2)	**0.77**	0.8	1.32	0.72	0.62	0.48

*: Conversion Loss; **: Noise Figure.
⋆: Need on-chip LO driver; **: Simulated results; #: With amplifier.

IV. Conclusion

In this letter, a compact 820-GHz down-converter employing the combination of the fourth subharmonic mixer and four-stage microwave LNA circuits is proposed for the THz application. Utilizing two $\lambda/4$ resonators in the THz signal path, the isolation between THz and LO/IF terminals is enhanced. Meanwhile, different interconnections of the MOSFET are studied for low transmission loss. Implemented in a conventional 40-nm CMOS technology, the measured results exhibit that the THz down-converter features 9.9-dB conversion loss and 39.2-dB noise figure with applying -6-dBm LO input power. The whole down-converter dissipates 28.6 mW under 1.1-V supply voltage.

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