Power-Optimized Digitally Controlled Oscillator in 28-nm CMOS for Low-Power FMCW Radars

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***Abstract*— This work presents the design of a 24-GHz digitally controlled oscillator (DCO) in an advanced 28-nm bulk CMOS technology for short-range frequency-modulated continuous-wave radar system-on-chip for mobile and Internet-of-Things devices. The power minimization is therefore the primary focus. The oscillator consumes a record low power of 1.2 mW at a 0.65-V supply voltage. It achieves a very large frequency tuning range (TR) of 5.8 GHz (27%) and a 150 kHz resolution without significantly degrading the phase noise (PN). The proposed design methodology results in a state-of-the-art −193 dBc/Hz FoM_T.**

***Index Terms*— Digitally controlled oscillator (DCO), frequency-modulated continuous wave (FMCW), LC oscillator, low-power, low-voltage, millimeter-wave (mm-wave), radar, remote sensing, wide range.**

I. Introduction

THE larger available bandwidth and the less crowded spectrum have made the millimeter-wave (mm-wave) frequency band highly attractive over the past decade. In particular, frequency-modulated continuous wave (FMCW) radars greatly benefit from the high carrier frequency and multigigahertz bandwidth available for improvement of angular and radial resolution [1]. The automotive application in the 77-GHz band has been one of the main drivers for research in this field [2]. However, the short-range sensing applications in the license-free industrial, scientific and medical (ISM) band between 57 and 66 GHz, such as vital signs' monitoring [3] and gesture recognition [4], have recently been drawing a lot of attention as well [5].

Highly integrated radar system-on-chip (SoC) embedded in mobile devices and Internet-of-Things (IoT) nodes require the use of an advanced CMOS technology and set a strong constraint on the power budget. Developing an efficient design methodology in these advanced technology nodes to reach the lowest power at low voltage becomes of paramount importance. Within the phase-locked loop (PLL), the oscillator is clearly the most power-hungry building block, particularly at mm-wave frequency. The objective is therefore to minimize the power consumption while ensuring a very large tuning range (TR) without significantly degrading the phase noise (PN). In addition, the novel design methodology for mm-wave oscillators needs to overcome the challenges posed by the ultralow voltage, the large gate resistance, the highly resistive metal lines and vias, and strong layout constraints of advanced nodes.

A system study shows that operating the digitally controlled oscillator (DCO) at a frequency of 20 GHz followed by an efficient frequency multiplier to generate the 60-GHz carrier is optimum for achieving the lowest power compared with a direct synthesis of a 60-GHz signal [6].

The letter is organized as follows. Section II describes the design choices about the oscillator topology, frequency tuning. and layout techniques, Section III shows the measurements, and Section IV draws the conclusions of this work.

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II. Description of the Circuits

The oscillator design is focused on the minimization of power consumption. The strategy to achieve this goal is twofold: 1) making the circuit as efficient as possible and able to work also at reduced voltage supply and 2) optimizing the resonator to maximize the overall quality factor Q across a very large frequency range. Two versions of the DCO were implemented: in one of them the decoupling capacitors are placed under the inductor instead of the metal filling for area reuse [7].

A. Low-Power and Low-Voltage Oscillator Structure

Fig. 1 shows the DCO schematic: the negative resistance is provided by a complementary cross-coupled (CC) pair structure which allows to increase the transconductance for the same bias current through current reuse achieving higher efficiency. Voltage-biasing is an obvious choice dictated by the limited supply voltage: four diode-connected devices $M_{1\text{B}-4\text{B}}$ provide $V_{\text{G1}-4}$ to impose the bias current $I_\text{B} = NI_\text{ref}$, where I_ref is a programmable current produced by a proportional to absolute temperature (PTAT) circuit and a current digital to analog converter (DAC). I_B is chosen such that the all the transistors work in moderate inversion for best efficiency [8].

After startup, the oscillation amplitude grows and it is sensed by $M_{1\text{B}-4\text{B}}$. Due to the nonlinear $I_\text{D}(V_\text{G})$ MOSFET characteristic, the sinusoidal voltage around the bias point does not produce a sinusoidal current, but a distorted waveform whose dc component should become larger than I_ref. However, the dc current cannot increase since it is imposed equal to I_ref by the current source. Consequently, $V_{\text{G1}-4}$ decreases such that the dc component of the distorted current in the presence of oscillation is exactly equal to I_ref [9]. The benefits of this biasing scheme are multiple: it allows to control the oscillation

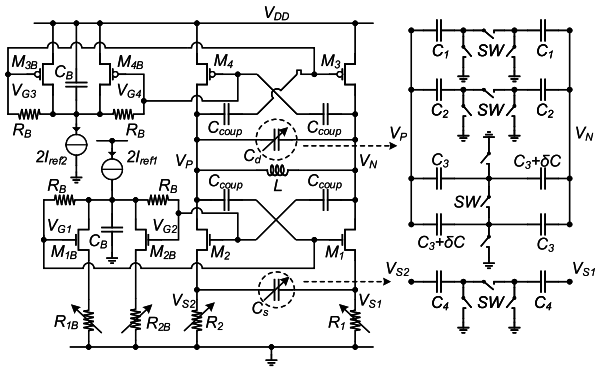

Fig. 1. Oscillator schematic with detailed biasing approach and capacitor banks.

TABLE I

PERFORMANCE OF THE CAPACITOR BANKS

	No. TE	C (fF)	ΔC (fF)	Q_C	C_{on}/C_{off}
Coarse	32	18.4	5.9	20	2.8
Intermediate	32	1.9	0.6	22	2.2
Fine	32	1.1 / 1.7	0.036	240	1.04
Super fine	16	6	0.004	20	3.1

amplitude while keeping a fixed current consumption, it brings the oscillator to work in class-C, and it provides a reliable startup, thanks to the larger initial V_{G1-4} [10]. To keep good control on the bias point, V_D of M_{1B-4B} has to be constant limiting the interference coming from the oscillator differential signal and its harmonics: it is achieved, thanks to the shared V_D nodes and the low-pass filtering provided by $R_B = 14\ k\Omega$ and $C_B = 70$ fF.

Some transistors biased in the linear region are placed between the sources and the ground of the nMOS CC pair to implement two variable resistors, R_1 and R_2, which decouple the two nodes and allow to fine-tune the frequency through a modified version of the capacitive degeneration technique as explained in Section II-B. The contribution of $R_{1,2}$ to the total PN is assessed by getting their impulse sensitivity function (ISF) and cyclostationary noise from simulation as shown in [11]. The latter simulations show that their impact is negligible compared with the CC pairs in the $1/f^3$ and $1/f^2$ regions.

B. Inductor and Capacitor Banks

The inductor used in the tank is differential with a single turn. To obtain the best quality factor, it is implemented using the layer with lowest resistivity. However, no shield is used, allowing to layout the oscillator partially under the inductor. The parameters are determined with a planar electromagnetic (EM) simulator leading to $L = 130$ pH with $Q_L = 25$ at 20 GHz. The placement of decoupling capacitor under the inductor in the middle of the loop where the magnetic field is minimum has a marginal impact on Q_L and the self-resonance frequency, as emerged from EM simulations (1% for both parameters).

The digital tuning in the DCO is composed of four capacitor banks which implement tuning steps of decreasing size. This approach allows to achieve both a large TR and high-frequency resolution with a reasonable number of tuning elements (TEs). The banks are matrices of identical TE composed of metal-oxide-metal (MOM) capacitors and switches controlled by binary to thermometer decoders. The thermometric approach is chosen over the binary to ensure monotonicity in spite of a larger number of control lines. Table I reports the performance of each capacitor bank.

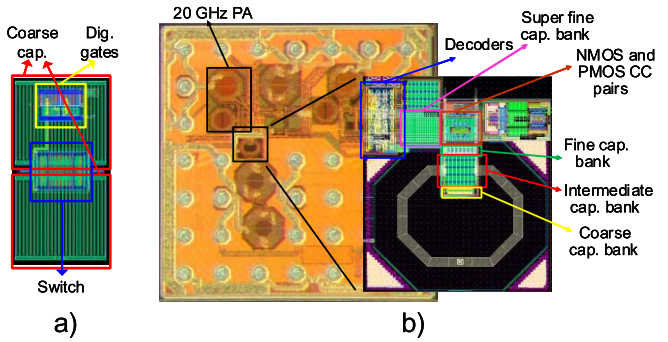

Fig. 2. (a) Detailed layout of a TE. (b) Circuit micrograph and oscillator layout.

In Fig. 1, C_1 and C_2 represent the coarse and intermediate TE banks, respectively. On top of the proper sizing of the capacitors and the switches, the optimization of the TE layout is crucial to get the best tradeoff between the TR and the quality factor [Fig. 2(a)]. The metal lines between the capacitors and the switch terminals both increase the parasitic capacitance and especially the series resistance. Switches and digital gates, which are part of the decoder, are placed under the capacitors, making their connection easier and achieving a very compact layout for the TE, and consequently also for the matrices.

Fig. 1 shows the structure of the fine TE bank C_3. When the technique presented in [12] is applied at mm-wave, the capacitors' absolute value is very small and the parasitic capacitance $C_{par,3}$ in parallel to the switch is significant. When the switch turns on, the capacitance changes by $\Delta C_3 = \delta C^2/(4(C_3 + C_{par,3}) + 2\delta C) \cong \delta C^2/(4(C_3 + C_{par,3}))$ if $\delta C \ll C_3$. The layout is implemented with the same approach as for the coarse and intermediate arrays.

The super fine bank C_4 is composed of TE with the same structure as the coarse and intermediate bank but it is placed at the source of the nMOS CC pair. This technique, called capacitive degeneration, is presented in [13] and [14] and it is implemented differently here. It relies on the property of the CC pair: any capacitance placed at the source appears as a negative capacitance at the drain multiplied by a factor $K \ll 1$ [15]. Nevertheless, instead of two current sources that would require a large V_{DD} for proper strong inversion operation giving good current matching and low noise, two transistors biased in the linear region are used for the chosen low voltage supply and voltage-biased topology. At high frequency, the impedance toward ground is low and factor K becomes

$$K = \frac{G_m^2}{\left(G_m + \frac{1}{R}\right)^2 + (4\pi f_0 C_{4,tot})^2} \tag{1}$$

where G_m is the transconductance of the transistors in the nMOS CC pair, f_0 is the oscillation frequency, and $C_{4,tot}$ is the total capacitance between the sources, obtained by summing a fixed and a variable portion. Since K is inversely proportional to $C_{4,tot}$ and f_0, it is possible to obtain a linear tuning only in a small frequency range.

The coarse capacitor bank is the biggest contributor to the total capacitance: since Q_{C1} is comparable to Q_L, it is the dominant factor in the degradation of the overall Q. For this reason, it is placed as close as possible to the inductor. Fig. 2(b) shows the layout of the DCO, which occupies only 0.026 mm^2.

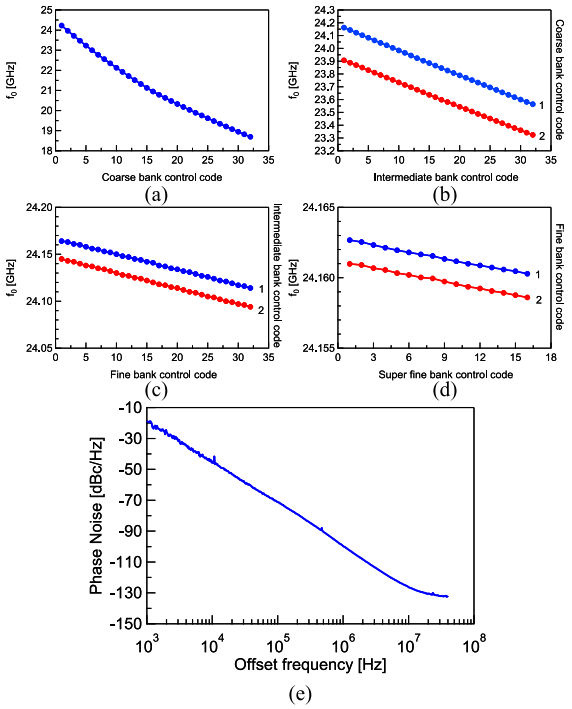

Fig. 3. Measured DCO performance: TR with (a) coarse, (b) intermediate, (c) fine, (d) super fine banks, and (e) PN at $f = 22$ GHz and 1 MHz offset.

III. Measurements

Integrated in the TSMC 28-nm bulk CMOS technology, the oscillator performance is measured after a 20-GHz two-stage power amplifier (PA), which consumes 15 mW at V_{DD}= 0.9 V to output 0 dBm. The DCO achieves an overall TR from 18.4 to 24.2 GHz (27.2%). The modified DCO shows a TR slightly shifted to higher frequencies, namely from 18.7 to 24.4 GHz (26.5%). The impact of devices inside the inductor does not influence noticeably the maximum achievable frequency (f_{max}) and the TR. The frequency range covered by the coarse bank is shown in Fig. 3(a): the step is around 250 MHz at the maximum frequency. Fig. 3(b) shows the frequency tuning of the DCO versus the intermediate bank control code in two consecutive coarse bands: the intermediate frequency step is around 20 MHz. The DCO fine tuning shown in Fig. 3(c) achieves a frequency resolution of 1.6 MHz, while the super fine in Fig. 3(d) around 150 kHz. For all the capacitor banks, the overlap between consecutive bands is larger than 50% as shown in the graphs. The modified DCO shows frequency steps similar to the standard DCO.

The current consumption and the PN are compared at 22 GHz. When optimized for the FoM, both the standard and the modified DCO consume 2.6 mW at V_{DD}= 0.9 V. The PN is measured after a division by 4 and then referred back to the output frequency of the oscillators [Fig. 3(e)]. At 1 MHz offset, the PN is -99 dBc/Hz for the standard DCO and -98 dBc/Hz for the modified DCO. f_{1/f^3} is around 400 kHz. Moreover, the PN is also measured at the two extremes of the frequency TR. At 1 MHz offset for the maximum frequency of 24.2 GHz, the PN is 0.2 dB higher than the one reported at 22 GHz. For the minimum frequency of 18.4 MHz, the PN shows an increase of 6 dB at 1 MHz offset. This increase is due to the reduced overall Q when all the TEs are switched on. The same behavior is observed in the modified DCO. This result confirms that the placement of decoupling capacitors under the inductor does not have any detrimental effect on the DCO performance in this technology and it allows to reuse large areas across the chip normally not exploited.

TABLE II
Performance Comparison to State-of-the-Art

	This work	[6]	[16]	[17]	[18]	[19]	[20]
Osc. Type	DCO	VCO	DCO	VCO	DCO	VCO	DCO
Tech (nm)	28	130	28	65	65	65	65
V_{DD} (V)	0.65	1	1	0.55	1	1	1
P_{DCO} (mW)	**1.2**	4.1	13	6.6	10	18	4.8
P_{PA} (mW)	8.3	10.3[e]	10	N/A	N/A	9	N/A
P_{out} PA (dBm)	-5	-28[e]	N/A	N/A	N/A	-2	N/A
f_{max} (GHz)	24.4	17.9	31.2	29.5	24.6	29.6	23.7
TR (%)	**27.2**	17	14	16	17	7.3	24.4
PN[a] (dBc/Hz)	-97[d]	-109	-104	-108	-102	-106	-106.6
FoM[a,b] (dBc/Hz)	-184[d]	-188	-183	-189.6	-180	-182.3	-187.2
FoM_T[a,c] (dBc/Hz)	**-193**[d]	-192.5	-186	-193	-184	-179.6	-194.9
Area (mm^2)	**0.026**	N/A	0.15	0.083	0.08	0.15	0.046

[a] at $\Delta f = 1$ MHz
[b] $\text{FoM} = \text{PN} - 20\log(f/\Delta f) + 10\log(P_{DCO}/1\,\text{mW})$
[c] $\text{FoM}_T = \text{FoM} - 20\log(\text{TR}/10\%)$ [d] at $f = 22$ GHz [e] at $f = 53$ GHz

The oscillator is also measured at reduced V_{DD} for low-voltage operation. At $V_{DD} = 0.65$ V, the standard DCO consumes approximately 1.2 mW, while the PN at 1 MHz offset increases to -97 dBc/Hz. The PA consumes 8.3 mW for an output power of -5 dBm. Table II reports the performance of the DCO at $V_{DD,min}$ and compares it with the state-of-the-art DCOs and voltage-controlled oscillators (VCOs), including the traditional oscillator FoM and the FoM_T calculated at 22 GHz. The presented design in an ultrascaled node achieves the largest continuous frequency TR and the lowest power consumption with a state-of-the-art FoM_T. Both the FoM and the FoM_T benefit from the lower V_{DD}: the power consumption is by far the best among the oscillators found in the literature at this frequency and it compensates for the PN degradation. Note that in spite of the ultralow power consumption, the DCO provides an output swing which is suitable for driving the following blocks without a voltage buffer. Moreover, the continuous TR is the largest reported as well and it brings additional benefits from the radar perspective. Note that the PA also consumes the lowest power while operating at $V_{DD} = 0.65$ V.

IV. Conclusion

The letter describes a DCO targeting on-chip radar applications, where the constraint on autonomy and voltage supply are key. The proposed design methodology allows to achieve the lowest power consumption of 1.2 mW at 24 GHz in an advanced 28-nm technology node with a very large TR of 5.8 GHz (27.2%), a 150 kHz frequency resolution, and a reasonable impact on the PN. The oscillator achieves by far the lowest power consumption resulting in a -193 dBc/Hz FoM_T and satisfying all the given radar specifications. In addition, area is saved by the use of decoupling capacitors as metal filling under the inductor without impact on the DCO performance. This technique can be extended to reuse large areas across the chip for low-dropout regulator's (LDO's) capacitive loads.

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