Low-Phase-Noise High-Efficiency Power Oscillator With Digitally Controlled Output Power

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***Abstract*— This letter proposes a low-phase-noise high-efficiency power oscillator with digitally controlled output power and frequency. The transformer-based matching network resonator is implemented to balance the quality factor and matching efficiency. The active core and the transformer are jointly optimized to achieve the required output power while achieving the low phase noise and high power efficiency. Besides, the digitally controlled cross-coupled pair array is utilized to tune the output power. To verify the mechanism mentioned above, the power oscillator is fabricated using conventional 40-nm CMOS technology with an active area of 0.19 mm^2. The proposed power oscillator exhibits a 21.7% tuning range from 2.30 to 2.86 GHz. The maximum output power is 4.5 dBm with a peak system efficiency of 25.1%. Meanwhile, the measured phase noise at a 3-MHz offset is −140.36 dBc/Hz at 2.79 GHz. The corresponding figure of merit (FoM) is 189.2 dBc/Hz, and FoM$_T$ is 196 dBc/Hz.**

***Index Terms*— Matching network, oscillator, output power, phase noise, transformer.**

I. Introduction

With the increasing requirements of low-cost and high-efficiency wireless systems, simplified transmitters, such as power oscillators [1]–[5], are getting more attention in recent years. The conventional transmitters [6]–[10] can be realized with a phase-locked loop (PLL) [11], [12] followed by a power amplifier (PA) [13]–[15], where oscillator [16]–[22] is critical in PLL. However, such transmitters consume a significant amount of power or occupy a large chip size. A PA-voltage-controlled oscillator (PA-VCO) described in [2] stacks the PA on top of the VCO for current re-use enhancing system efficiency. Nevertheless, it has limited maximum output power due to the reduced voltage headroom, while the need for an off-chip output matching network raises the system cost. To enhance the output power and achieve the on-chip matching, the digital-controlled oscillator-PA (DCO-PA) is introduced in [3] and [5]. However, the phase noise performances of such DCO-PAs are limited, and the output power cannot be digitally controlled. Therefore, the design of a power oscillator with the merits of digitally controlled output power, high-efficiency, and good phase noise performance is still a great challenge.

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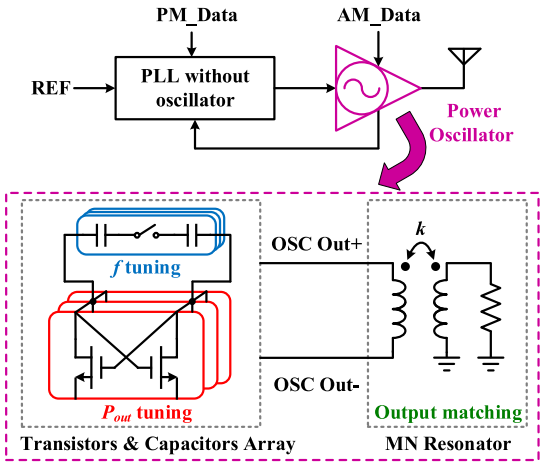

Fig. 1. Concept of the power oscillator-based PLL (top) and architecture of the proposed power oscillator (bottom).

In this letter, a low-phase-noise high-efficiency power oscillator with the digitally controlled output power and frequency is proposed. The transformer-based matching network resonator is implemented to balance the quality factor and matching efficiency. The active core and the transformer are jointly optimized to achieve the required output power while achieving the low phase noise and high power efficiency. Meanwhile, the digitally controlled cross-coupled pair array is utilized to tune the output power. Then, based on the aforementioned mechanisms, the proposed power oscillator is implemented and fabricated using a 40-nm CMOS process.

II. Power Oscillator

The concept of the power oscillator-based PLL is shown at the top of Fig. 1. Such PLL could directly support the phase and amplitude modulation of the output signal, where the power oscillator is critical to control the output frequency and amplitude. The architecture of the proposed power oscillator is depicted at the bottom of Fig. 1. The matching network resonator is implemented for signal generation and output matching. Meanwhile, the digitally controlled cross-coupled pair array and the switch capacitors array are utilized to control the output power and frequency, respectively.

A. Matching Network Resonator

Fig. 2(a) shows the schematic of a transformer tank with a loaded resistor (R_L). The input impedance of the loaded transformer ($Z_{11,L}$) is expressed as (1), which is shown at

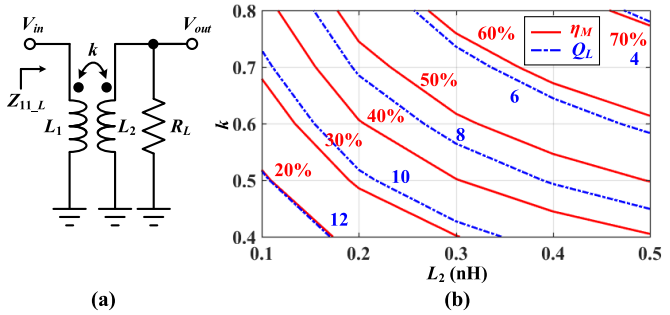

Fig. 2. (a) Schematic of the transformer tank. (b) Contour plot for different values of η_M and Q_L as a function of L_2 and k at 2.5 GHz ($L_1 = 0.8$ nH and $Q_1 = Q_2 = 15$).

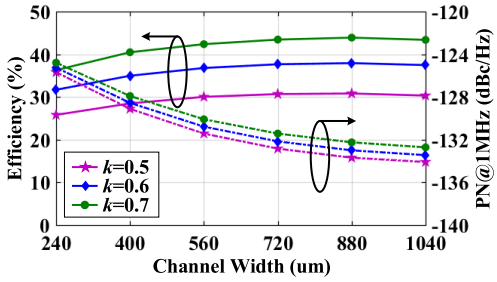

Fig. 3. Simulated efficiency and phase noise under different channel widths of cross-coupled transistors and k at 2.5 GHz ($L_2 = 0.3$ nH).

the bottom of the next page, where r_{L1} and r_{L2} are the resistive losses from the primary (L_1) and secondary (L_2) coils, respectively. k is the magnetic coupling coefficient. Thus, the loaded quality factor (Q_L) of the transformer could be obtained by $Q_L = \text{imag}(Z_{11,L})/\text{real}(Z_{11,L})$ [23]. The transformer also serves as the output matching network, and the efficiency of the loaded transformer (η_M) can be expressed as

$$\eta_M = \frac{R_L}{\left|\frac{r_{L2}+R_L+j\omega L_2}{j\omega k\sqrt{L_1 L_2}}\right|^2 r_{L1} + r_{L2} + R_L}. \tag{2}$$

Fig. 2(b) shows the contour plot for different values of η_M and Q_L as a function of L_2 and k. Note that there is a tradeoff between η_M and Q_L. Thus, lower k is preferred to obtain a good phase noise performance. To compensate for the reduction of efficiency caused by the reduced k, the size of the transistor is optimized. As shown in Fig. 3, different combinations of k and channel width could obtain the same efficiency level. Therefore, for the same output power and efficiency level, k and transistor size are jointly optimized for low phase noise.

B. Digitally Controlled Cross-Coupled Pair Array

The digitally controlled cross-coupled pair array is utilized for digitally controlled output power. Fig. 4(a) and (b) shows the simulated voltage waveform at the oscillation output and the load resistor, respectively. Here, the 3-bit digitally controlled cross-coupled pair is used as a prototype. It can be

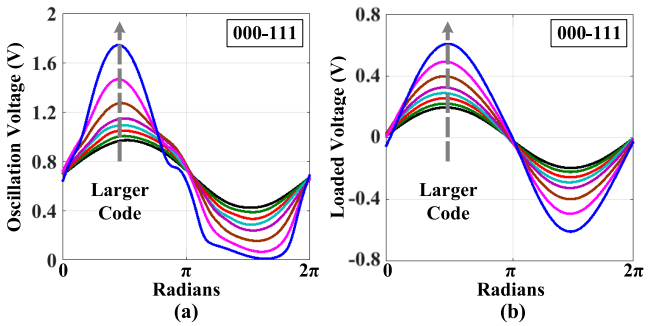

Fig. 4. Simulated voltages waveforms at (a) oscillation tank and (b) loaded resistor under 3-bit digitally controlled.

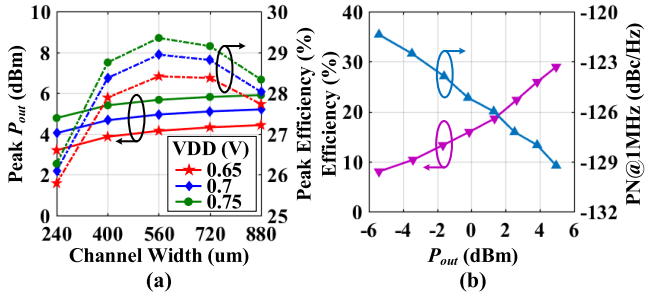

Fig. 5. (a) Simulated peak P_{out} and efficiency of the power oscillator under different channel widths of cross-coupled transistors and V_{DD}. (b) Simulated efficiency and phase noise versus P_{out} at 2.5 GHz.

seen that the output voltage could be controlled by changing the digital code, which achieves the controlled output power. Fig. 5(a) shows the simulated peak output power and efficiency of the power oscillator under different channel widths of cross-coupled transistors and the supply voltage V_{DD}. Note that, for required output power, different combinations of V_{DD} and channel width could lead to different efficiency. Under a constant V_{DD}, an optimized efficiency could be observed with a specific channel width, where the parasitic parameters and operation condition of the cross-coupled pair achieve a good matching. Therefore, V_{DD} and sizes of the cross-coupled pair should be chosen carefully to obtain good power efficiency. For a required peak output power of 5 dBm, a 0.7 V V_{DD} and 560 μm of transistor channel width are chosen to achieve the optimized efficiency. The simulated efficiency and phase noise versus P_{out} at 2.5 GHz with the optimized parameters are depicted in Fig. 5(b).

III. Circuit Implementation

Fig. 6 illustrates the structure of the proposed power oscillator, which is implemented in conventional 40-nm CMOS technology. Here, V_{DD} of 0.7 V is chosen. For the transformer design, the electromagnetic simulated Q_L is 8.6 with $Q_1 = 15$ and $Q_2 = 10$, while k is 0.55 at 2.5 GHz; 16 switch capacitors (i.e., five binary control bits, B_0–B_4) and one pair of varactors (i.e., C_{V1}) are used to introduce the frequency coarse tune and fine tune, respectively. Besides, the normally

$$Z_{11,L} = r_{L1} + j\omega(L_1 - k\sqrt{L_1 L_2}) + \frac{-\omega^2 k L_2\sqrt{L_1 L_2} + \omega^2 k^2 L_1 L_2 + j\omega k(r_{L2}+R_L)\sqrt{L_1 L_2}}{r_{L2}+R_L+j\omega L_2}. \tag{1}$$

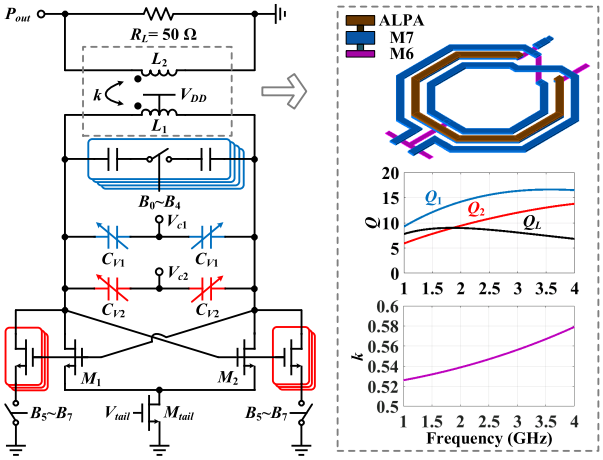

Fig. 6. Schematic of the proposed power oscillator with transformer layout and EM-simulated results.

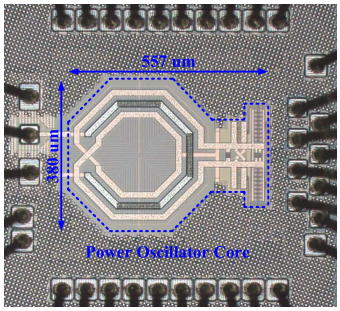

Fig. 7. Chip micrograph.

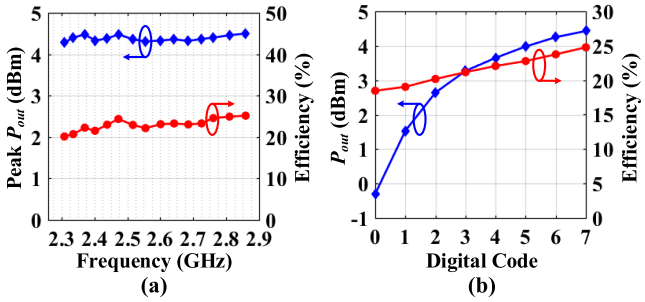

Fig. 8. (a) Measured peak P_{out} and efficiency variation while tuning frequency. (b) P_{out} and efficiency under 3-bit digitally control at 2.79 GHz.

open cross-coupled transistors M_1/M_2 are 70 μm/40 nm to ensure the startup condition. Another seven switchable cross-coupled transistors (i.e., three binary control bits, B_5–B_7) with the optimized size of 70 μm/40 nm are utilized to tune the output power. Note that the parasitic would be changed with the switching of transistors, which leads to the shifting of the oscillator frequency. The pair of varactors C_{V2} are implemented to keep the frequency constant. The frequency tuning range of C_{V2} is demanded to cover the maximum frequency shifting.

IV. Measurement Results

Fig. 7 shows the chip micrograph of the proposed power oscillator. The active area is 0.19 mm^2. As depicted in Fig. 8(a), the oscillator exhibits a 21.7% tuning range from 2.30 to 2.86 GHz. The maximum output power and the peak efficiency versus different frequencies are 4.1–4.5 dBm and 20%–25.1%, respectively. Here, the loss (including connector, cable, and so on) of 2 dB is taken into consideration. Fig. 8(b) shows the output power tuning at 2.79 GHz. The measured output power is −0.3–4.43 dBm, and the efficiency is 18.4%–24.7% under 3-bit digitally control. At 4.43-dBm output power, the second harmonic is −36.64 dBm, and the third harmonic is −25.99 dBm. Fig. 9 shows the measured phase noise at 2.79 GHz under maximum output power. The phase noise is −140.36 dBc/Hz at 3-MHz offset under an 11.2-mW power consumption, which exhibits a figure of merit (FoM) of 189.2 dBc/Hz. Measured results are summarized and compared with the relevant state of the arts in Table I. Note that the proposed power oscillator achieves digitally controlled output power and exhibits a competitive phase noise, FoM, and efficiency.

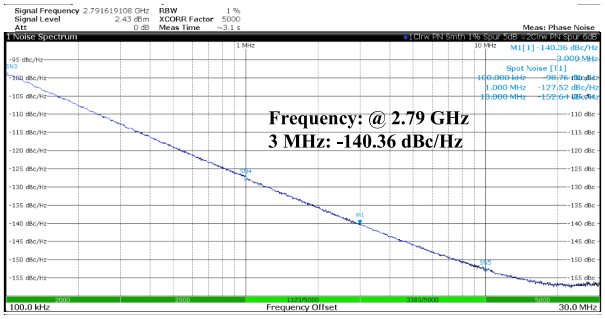

Fig. 9. Measured phase noise at 2.79 GHz under maximum output power.

TABLE I
Performance Summary and Comparison

Ref.	JSSC 2016 [2]	JSSC 2017 [3]	JSSC 2020 [5]	**This Work**
Technology	130-nm CMOS	65-nm CMOS	65-nm CMOS	**40-nm CMOS**
Supply Voltage (V)	1.2	0.3–0.7	0.3–0.7	**0.7**
Freq. Range (GHz)	2.26–2.58	2.37–2.41	2.2–2.5	**2.30–2.86**
Tuning Range	13.2%	1.3%	12.8%	**21.7%**
Peak P_{out} (dBm)	−1	6	0	**4.5**
Digitally P_{out} Control	No	No	No	**Yes**
Peak Efficiency	17.5%	26.1%	20.8%	**25.1%**
DC Power (mW)	4.56	15.3	4.8	**11.2**
PN@Peak P_{out} (dBc/Hz)	−129 @ 2.5 MHz	−128.5 @ 3.5 MHz	−126.4 @ 2.5 MHz	**−140.36 @ 3 MHz**
FoM (dBc/Hz)	182.2	173.3	179.2	**189.2**
FoM$_T$ (dBc/Hz)	184.7	155.6	181.4	**196**
Active Area (mm^2)	0.2	0.39	0.17	**0.19**

V. Conclusion

In this letter, a low-phase-noise high-efficiency power oscillator is proposed to achieve the output power and frequency tuning. The active core and the transformer are jointly optimized to achieve the required output power while achieving the low phase noise and high power efficiency. Besides, the digitally controlled cross-coupled pair array is utilized to tune the output power. The measurement exhibits a 21.7% tuning range from 2.30 to 2.86 GHz. The maximum output power is 4.5 dBm with a peak system efficiency of 25.1%. Meanwhile, the measured FoM is 189.2 dBc/Hz, and FoM$_T$ is 196 dBc/Hz at a 3-MHz offset. With such good performance, the proposed power oscillator is attractive for RF front-end applications.

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