A 17.3–20.2-GHz GaN-Si MMIC Balanced HPA for Very High Throughput Satellites

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***Abstract*— This letter presents the design and experimental characterization of a *K*-band high power amplifier (HPA) monolithic microwave-integrated circuit (MMIC) for the next generation of very high throughput satellites (vHTS). The MMIC is a three-stage balanced amplifier realized on a commercial 100-nm gate length gallium nitride on silicon (GaN-Si) technology. The design is compliant with space reliability constraints and, despite the larger thermal resistance and losses shown by the silicon (Si) substrate with respect to the more common silicon carbide (SiC), the realized HPA delivers, in pulsed condition, a peak output power larger than 41 dBm in the operative band from 17.3 to 20.2 GHz, with an associated power added efficiency (PAE) and gain up to 40% and 26 dB, respectively. In continuous wave (CW) operative conditions and with a backside temperature of 85 °C, the MMIC delivers a minimum output power and PAE of 39.4 dBm and 28%, respectively. Moreover, a 24-h test at saturated power has shown almost negligible performance degradations, thus providing confidence in the selected GaN-Si technology's robustness.**

***Index Terms*— Gallium nitride (GaN), GaN on silicon (GaN-Si), high power amplifier (HPA), *Ka*-band, satcom.**

I. Introduction

CONNECTING anything to internet anytime and everywhere is already the technological leitmotif of our daily life. To face such unprecedented request, both commercial and research initiatives in this field are more and more focused on the development of solutions to boost network performances [1]. However, relying upon terrestrial infrastructures only could not be sufficient to satisfy all the requirements at sustainable cost [2]. As a solution, the synergy between underlying and satellite networks is pursuit [2]. Indeed, Satcom systems can efficiently complement 5G and beyond generations in either urban underserved or rural areas, thus paving the way for a true ubiquitous coverage [2], [3]. Moreover, since their capacity can be allocated where it is provisionally needed, they can support emergency area as well as data traffic peaks and other contingency situations [3].

To this end, constellations of very high throughput satellites (vHTS) will be deployed around the globe and integrated with the terrestrial networks through satellite-to-ground links, mostly in *K*-band [4]. Such spacecraft will be embarked with multiple-beam active antennas offering communication volumes even larger than 1 Tb/s per satellite. At spacecraft level, this implies an increasing number of embarked components; thus, a subsequent need of miniaturization leads to the demand of subcircuits with lower mass and volume, better thermal management, and, of course, reliability. These breakthroughs are tightly dependent to the adopted power amplifier (PA). Traveling wave tube amplifiers are still the predominant and preferred solution for space-borne PAs. However, solid state PAs (SSPAs) are quickly rising up thanks to the availability of reliable gallium nitride technologies and the development of low lossy space combining techniques [5].

The monolithic microwave-integrated circuit (MMIC) PA discussed in this letter represents the building block of a space-borne SSPA for vHTS covering the 17.3–20.2-GHz frequency band [5]. The MMIC, based on a three-stage balanced architecture, was implemented on a 100-nm gate length gallium nitride on silicon (GaN-Si) technology available at OMMIC foundry [6]. In continuous wave (CW) operative conditions and with a backside temperature of 85 °C, the high PA (HPA) delivers a minimum output power and power-added efficiency (PAE) of 39.4 dBm and 28%, respectively. Moreover, a 24-h test in CW at saturated power has shown negligible performance variations, thus providing confidence in the selected GaN-Si technology's robustness.

II. Design

Table I reports the MMIC requirements as derived from a top to bottom power budget analysis of the SSPA under development [5].

A three-stage balanced architecture with input and output Lange coupler was selected. The use of the latter leads to a twofold benefit as compared to a more standard corporate topology [7]. First, the HPA return losses are minimized being almost coincident with those of the Lange structure. Second, the synthesis of the optimum output load of the devices in the last stage is easier, since the load transformation ratio to be accomplished is halved.

To identify the most appropriate gate periphery of each stage, a series of load-source pull simulations on different

Manuscript received October 26, 2020; revised December 2, 2020; accepted December 22, 2020. Date of publication January 12, 2021; date of current version March 11, 2021. This work was supported by the European Union's Horizon 2020 Space Research and Innovation Programme under Grant 821830. *(Corresponding author: Rocco Giofrè.)*

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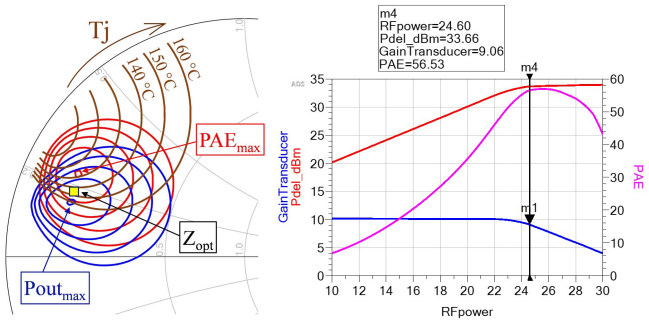
Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2020.3047211.

Digital Object Identifier 10.1109/LMWC.2020.3047211

TABLE I
MMIC HPA REQUIREMENTS

Feature	Symbol	Spec	Unit
Bandwidth	BW	17.3-20.2	GHz
Output power	Pout	$\geqslant 40$	dBm
Gain	G	$\geqslant 22$	dB
Power Added Efficiency	PAE	$\geqslant 30$	%
Return Losses	RL	$\geqslant 15$	dB
Baseplate Temperature	T_{BP}	-5 to 85	°C
Junction Temperature	T_j	$\leqslant 160$	°C

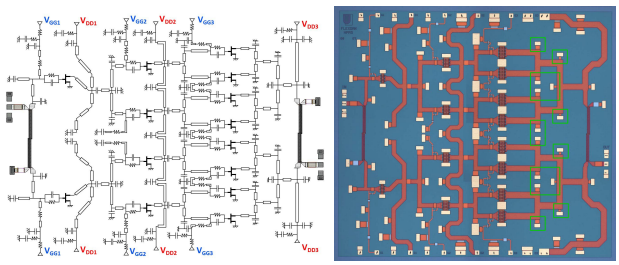


(a) (b)

Fig. 1. Simulated (a) load pull contours and (b) performance on the optimum load of the 8 μm $\times$ 100 μm at $f_0 = 18.75$ GHz.

device geometries was carried out. This task was accomplished carefully accounting for power and thermal requirements, as well as space reliability constraints (i.e., derating rules). In particular, drain and gate bias voltages were fixed to $V_{\rm DD} = 10$ V and $V_{\rm GG} = -1.4$ V ($I_D = 100$ mA/mm), respectively, whereas the base plate temperature of the electrothermal model was fixed to $T_{\rm BP} = 85$ °C (worst case condition). The contour levels of output power, PAE, and junction temperature (T_J) at 1 dB of gain compression were superimposed and the optimum load ($Z_{\rm OPT}$) to be synthesized with the matching networks was selected. As an example, Fig. 1(a) shows the registered results for the 8 μm $\times$ 100 μm device at center frequency ($f_c = 18.75$ GHz). Notably, $Z_{\rm OPT}$ was chosen along the trajectory between the maximum output power and PAE levels, carefully accounting for the T_J contours. In particular, to leave some margins for the following design steps, the contour level of 155 °C was assumed as the boundary condition in this preliminary analysis. Fig. 1(b) shows the simulated performance of the 8 μm $\times$ 100 μm device when terminated onto $Z_{\rm OPT} = 9.6 + j \cdot 7.5\ \Omega$. Ideally, it delivers about 33.5 dBm of output power with 9 dB of gain and 56% PAE, at 1 dB of gain compression. It is worth noting that the second harmonic load pull reveals that close to the short circuit loading condition there is a severe drop in the performance. Thus, such a region was prevented in the design of the matching networks.

Relying upon this kind of analysis, the HPA architecture was chosen. It includes, eight 8 μm $\times$ 100 μm devices in the final stage, four 6 μm $\times$ 100 μm in the driver stage, and two 6 μm $\times$ 50 μm devices in the predriver stage. Each active device was stabilized using an RC-parallel network connected in series to the gate, together with a resistor in the gate bias line. All stages are biased with the values mentioned above, whereas the matching networks were designed



(a) (b)

Fig. 2. (a) Schematic and (b) chip photograph of the designed MMIC.

following a semilumped strategy, to minimize the ohmic losses inherently higher for silicon (Si) substrates with respect to silicon carbide (SiC). Fig. 2 shows the schematic (a) and photograph (b) of the realized circuit, whose size is 5.0 $\times$ 4.5 mm^2. Notably, during the electromagnetic (EM) analysis of the layout, differences with respect to the circuit-level simulations were observed, especially in the output combiner network. In particular, even if the Lange shows a wideband coupling performance, the impedances at its input ports are slightly different from each others, which in turn introduces unbalancing among the loads synthesized across each device in the last stage of the HPA. As a solution to mitigate this drawback and also the unavoidable coupling among adjacent components, we introduce physical asymmetries (i.e., slightly different values) among the symmetric lumped components, like the capacitors highlighted in green boxes in the picture. Among others, we preferred this solution because it allows to recover the electrical symmetry of the network without requiring significant geometry modifications. Finally, it is worth mentioning that, being the fingers of the Lange narrow (i.e., 10 μm) and very close to each others (i.e., 4 μm), its design was accomplished carefully evaluating the foundry's current and voltage maximum ratings and their derating rules for space reliability.

III. EXPERIMENTAL RESULTS

The realized MMIC was measured first on wafer in pulsed condition and then in CW after mounted on a proper test-jig. The former were carried out on all the realized MMICs at the nominal bias condition ($V_{\rm DD} = 10$ V and $V_{\rm GG} = -1.4$ V ($I_D = 0.94$ A), with a pulse repetition time of 10 μs and 1% of duty cycle. Fig. 3 compares such results with the original simulations (red lines with circle symbols) carried out using the process design kit (PDK) version 1.2.4. Notably, a frequency shift of roughly 800 MHz was present. After a reverse engineering work, it was recognized that such an effect was related to the accuracy level of both the active device models and the EM stack used in simulation. Indeed, recently the foundry has released a new version of the PDK (i.e., version 1.3), which updates both active device model and EM stackup. The simulation of the realized HPA with the latter PDK matches with the measured results, as shown by the green lines with triangle symbols in Fig. 3. In the second iteration, this HPA will be fine-tuned using the new PDK, which has shown excellent prediction capability. Nevertheless, the actual HPA delivers an output power up to 41.5 dBm

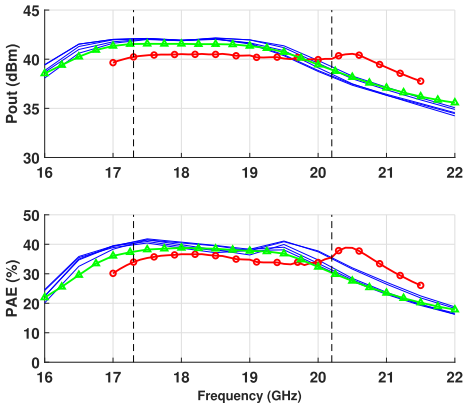
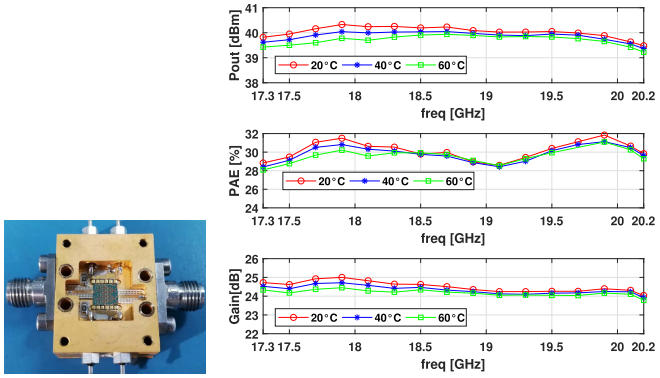


Fig. 3. Comparison between on-wafer pulsed measurement (continuous lines) and simulated counterparts (red with circle symbols for original design, green with triangles for new PDK) at 14 dBm of available input power.



(a) (b)

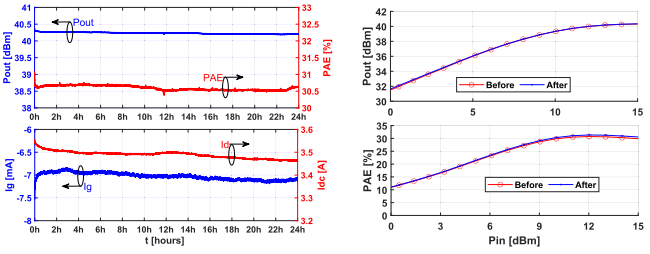
Fig. 4. (a) Picture of the packaged MMIC and (b) measured performances of the packaged MMIC at nominal bias point and for different temperature.

together with a PAE above 30% and a gain larger than 27 dB in the frequency range from 17.3 to 20.2 GHz, also showing a limited spreading among samples. A PAE peak above 40% has also been registered at the center of the bandwidth.

On the basis of the on-wafer characterization, a MMICs with average performance was selected and mounted in a preliminary (i.e., not optimized) copper-tungsten test-jig, as shown in Fig. 4(a). It includes input–output 50-Ω transmission lines to accommodate the coaxial-to-MMIC transition, as well as top/bottom biasing networks together with four dc feedthrough (i.e., one for drain and gate voltages on each side). The packaged HPA was subjected to an extensive CW test campaign, after carrying out a rapid dc burn-in.

Fig. 4(b) shows the PAE, output power, and gain behaviors as functions of the frequency when the temperature at the bottom of the package is fixed to 20 °C, 40 °C, and 60 °C using a Peltier cell. Accounting for the material stack along the Z-axis, this implies a T_{BP} at the backside of the MMIC of roughly 45 °C, 65 °C, and 85 °C, respectively. Notably, at $T_{\mathrm{BP}} = 85$ °C the minimum output power is better than 39.4 dBm with a minimum PAE of 28%. It is worthy to mention that these performances refer to the packaged MMIC, thus accounting for the losses of the bond wires, 50-Ω transmission lines, and the coaxial connectors, which have not been optimized at all.

Fig. 5(a) shows the registered behaviors of output power, PAE, drain, and gate currents during a 24-h CW test. This



(a) (b)

Fig. 5. (a) 24-h CW test results. (b) Measured power sweep at center frequency before and after the 24-h test.

TABLE II
COMPARISON WITH OTHER GAN MMICS PAS

Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Tech. (SiC/Si)	Ref
18.5–19.5	40	37.5	28	SiC	[8]
17–21	40,3	35.5	22	SiC	[9]
17–20	40	38	20	SiC	[10]
18.5-24	36.5	40	25	SiC	[11]
17.3-20.2	**39.5**	**28**	**24**	**Si**	**T.W.**

characterization was performed at an ambient temperature, fixing the frequency and the input power at $f_c = 18.75$ GHz and $P_{\mathrm{in}} = 14$ dBm, respectively. The measurements were acquired every 30 s. Over the entire test, a quite stable behavior of the performance was observed. In particular, the output power and PAE diminished of only 0.1 dB and 0.5%, respectively, with a negligible increase in the gate current, thus revealing a significant maturity of the technology. This is further confirmed looking at Fig. 5(b), where is reported the measured power sweep at $f_c = 18.75$ GHz before and after the 24-h test. Variations are very minimal.

The CW performances of the MMIC are compared with the state-of-the-art results in Table II. Notably, in the same frequency range, all previously reported MMICs were realized using GaN-SiC, and typically without accounting for space derating and temperature constraints, which clearly pose severe challenges during the design phases. Despite this, the performance of the realized MMIC is not too far from the others, indicating that GaN-Si technology could represent a possible alternative to the GaN-SiC counterpart, even for space applications.

IV. CONCLUSION

The design and measurements of a K-band balanced amplifier for satellite applications have been presented. The MMIC, realized on 100-nm gate length GaN-Si technology, delivers more than 10-W output power with an associated PAE and gain better than 28% and 24 dB, respectively, in the operative band from 17.3 to 20.2 GHz. Moreover, a 24-h test at saturated power has shown negligible performance degradations, thus providing confidence in the selected GaN-Si technology's robustness.

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