1.2–2.8-GHz 32.4-dBm Digital Power Amplifier With Balance-Compensated Matching Network

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***Abstract*— In this letter, a wideband watt-level digital power amplifier (DPA) with a balance-compensated matching network is proposed for polar transmitters. The balance response of the differential to the single-ended transformer is enhanced by a series-loaded compensation capacitor, which leads to the improvement of the DPA efficiency. To verify the mechanisms, a prototype DPA is fabricated in conventional 40-nm CMOS technology. The proposed DPA operates over 1.2–2.8 GHz and exhibits a peak output power of 32.4 dBm at 2 GHz and a peak drain efficiency of 53.8% at 1.8 GHz. It supports 50-MHz 64-quadratic-amplitude modulation (QAM) with average output power (P_{avg}) of 25.37 dBm, error vector magnitude (EVM) of −26.97 dB, adjacent channel power ratio (ACPR) of −29.61 dBc, and 10-MHz 1024-QAM with P_{avg} of 22.14 dBm, EVM of −35.75 dB, and ACPR of −35.37 dBc, respectively.**

***Index Terms*— Balance-compensated matching network, digital power amplifier (DPA), efficiency enhancement, watt-level, wideband.**

I. Introduction

With the ever-development of wireless communication, power amplifiers (PAs) with high power, high efficiency, low supply, and low cost are dramatically demanded. Compared with III–V technologies, the CMOS technology becomes a competitive candidate with multifunction and low cost. CMOS analogy PA techniques with good power and linearity are highly developed, such as the distributed active transformer [1], power-combining scheme [2]–[5], and stacked transistors [6]. However, the conventional transmitter (TX) with analog PA requires extra modules, including the digital-to-analog converter (DAC), mixer, and so on. Therefore, the system efficiency and integration level of conventional TX are relatively low. Compared with analog PAs, digital PAs (DPAs) [7]–[16] exhibit enhanced efficiency and medium output power. Recently, to implement watt-level DPAs, topologies of voltage-combining [17], [18] and current-combining [19]–[21] are developed. However, compact watt-level CMOS DPAs with merits of wideband, high efficiency, and low supply remain challenges.

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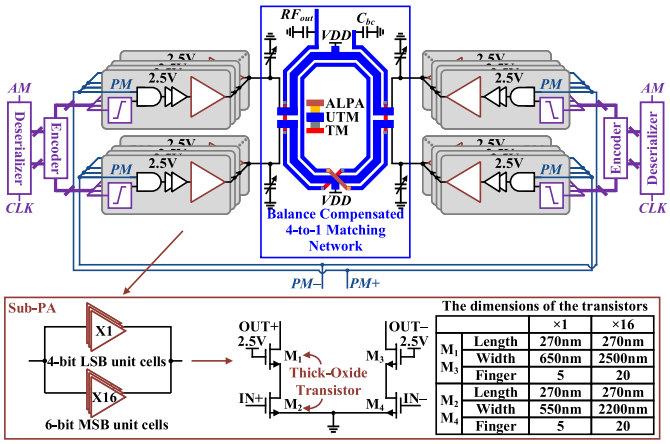

Fig. 1. Block diagram of the proposed watt-level DPA.

In this letter, a 1.2–2.8-GHz watt-level DPA with a balance-compensated matching network is proposed. Such matching topology consists of a 4-to-1 transformer with a compensated series-loaded capacitor, which enhances the output power and efficiency, simultaneously. A prototype DPA is implemented and fabricated using a conventional 40-nm CMOS technology, which exhibits 32.4-dBm peak output power and 53.8% peak drain efficiency (DE) under a 1.1-/2.5-V supply.

II. Circuit Design

The block diagram of proposed wideband watt-level DPA based on a balance-compensated matching network is shown in Fig. 1. A four-way series combining architecture is adopted to reduce the voltage stress on transistors and impedance transform ratio of the matching network compared with the parallel combining type. Each switch array of the DPA consists of 6-bit unary MSB cells and 4-bit binary LSB cells. Cascode circuit with 2.5-V thick-oxide transistors is used to implement both MSB and LSB unit cells for high output voltage swing, while 2.5-V digital AND gates and buffers combine the phase-modulated signal and amplitude codes. Meanwhile, the matching network performs the four-way power combining, differential to single conversion, wideband impedance matching, and balance compensation, simultaneously. Besides, two sets of parallel high speed 5:1 deserializer and encoder are used to convert the serial baseband signals to the thermometer and binary codes, while level shifters convert the 1.1 V signals to 2.5 V.

A. Matching Network With 4-to-1 Transformer

One of the challenges for watt-level wideband DPA design is the output matching network. The transformer is usually

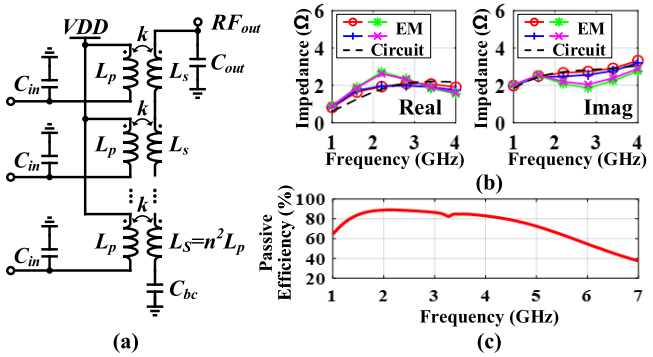

Fig. 2. (a) Simplified circuits of the proposed N-way combining matching network with imbalance compensation. (b) Calculated Z_{in} and simulated Z_{in} with EM module and (c) passive efficiency once $N = 4$.

used due to its nature with multiresonance to extend the bandwidth. Higher output power is achieved with increased drain current, i.e., smaller Z_{in} of the transformer once the voltage swing remains the same. Such operation leads to a larger inductance ratio of the transformer. However, the ratio is limited due to Q degradation. To address the issue, a series power combining scheme is used. As shown in Fig. 2(a), the N-way series power combining matching network is exhibited. The input impedance Z_{in} of matching network using the N-way series combining with balance compensation is expressed as follows:

$$Z_{\text{in}} = \frac{a\frac{1}{j2\pi f C_{\text{in}}}}{a + \frac{1}{j2\pi f C_{\text{in}}}} \tag{1}$$

$$a = \frac{jb2\pi f k^2 L_p}{b + j2\pi f k^2 L_p} + j2\pi f(1-k^2)L_p \tag{2}$$

$$b = \frac{k^2}{n^2 N}\left(\frac{R_L\frac{1}{j2\pi f C_{\text{out}}}}{R_L + \frac{1}{j2\pi f C_{\text{out}}}} + \frac{1}{j2\pi f C_{\text{bc}}}\right) \tag{3}$$

where R_L, n, k, L_p, C_{in}, and C_{out} are the load resistance, inductance ratio, coupling factor, inductance of primary windings, parallel capacitors at primary windings, and load capacitor, respectively. Note that C_{bc} is a compensation capacitor, which is introduced to decrease the imbalance of the transformer. The calculated Z_{in} according to (1) under the case of $N = 4$ is compared with the electromagnetic (EM)-simulated impedance in Fig. 2(b), which is not identical to each other. Note that this simplified model is given to design the matching network with targeted impedance quickly, which does not include the parasitic capacitors of the transformer. The imbalance effect of the four inputs introduced by the parasitics will be analyzed in Section II-B. The EM-simulated passive efficiency of the implemented transformer in Fig. 3(a) is shown in Fig. 2(c), which achieves more than 70% efficiency from 1.2 to 5 GHz.

B. Imbalance Compensation Technique

The asymmetry of differential to single-ended transformer shows a significant effect on the efficiency and output power of PAs, especially for the large impedance transformation ratio [22]–[24]. The simplified circuits of conventional and proposed four-way power combiners are depicted in Fig. 3(a) and (b), respectively. As shown in Fig. 3(a), I_{out} in the secondary coil partially flows into the parasitic capacitors

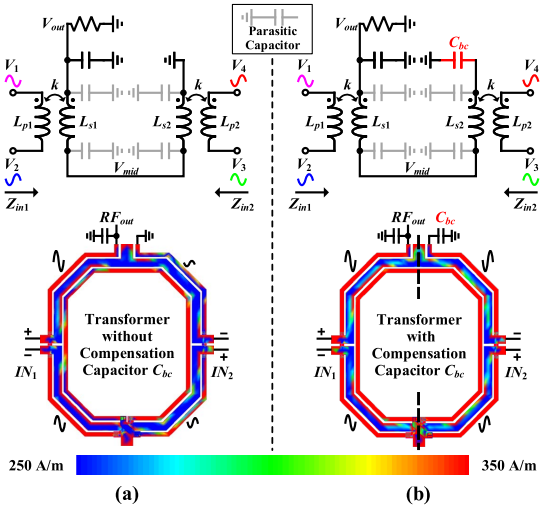

Fig. 3. Simplified circuit and current density of the transformers (a) without and (b) with a compensated capacitor C_{bc}.

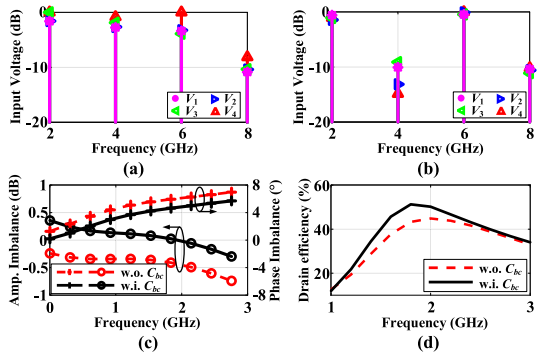

Fig. 4. Normalized drain voltage spectrum (a) without compensation and (b) with compensation at 2 GHz in decibel scale. Effects of C_{bc} (i.e., 5.6 pF) on (c) amplitude and phase imbalances (Amp.: amplitude) and (d) DE.

at the middle point, which leads to a larger current density at L_{s1} than L_{s2}. Here, the transformer without C_{bc} has a high current density near the output terminal and low current density near the grounded terminal, which implies a relatively large impedance imbalance for the four inputs. Such imbalance will increase at higher operating frequency since the parasitic effect becomes more significant. In addition, the limited quality factor of the parasitic capacitor leads to a lower passive efficiency. To reduce loss and improve the balance characteristic of the transformer, a capacitor C_{bc} marked in red is introduced to compensate for such imbalance, as shown in Fig. 3(b). It is notable that the balance-compensated transformer exhibits uniform current distribution for the entire secondary coil, which leads to enhanced impedance balance. Since the active circuit is identical, such impedance difference can be demonstrated with the variation of drain voltages (i.e., V_1, V_2, V_3, and V_4). The simulated spectrums of drain voltages at 2 GHz are shown in Fig. 4(a) and (b). It is seen that the imbalance of harmonic voltages is decreased based on the proposed imbalance-compensated matching network with C_{bc}. C_{bc} could be predicted according to (1)–(3) once other elements are chosen. Meanwhile, considering the practical implementation (i.e., routing with transistors and passive circuits) with parasitic, Q, and so on, the estimated C_{bc} is optimized within the practical circuits to achieve enhanced amplitude- and phase-balance responses. Here, an example is

TABLE I

COMPARISON WITH THE STATE-OF-THE-ART WATT-LEVEL CMOS PAS

	This Work			JSSC2019 [25]		ISSCC2019 [26]	ISSCC2019 [27]	JSSC2012 [28]
CMOS Tech.	**40-nm**			28-nm		65-nm	40-nm	0.18-μm with IPD technology
Architecture	**Digital Polar with Balance Compensated matching**			Digital Polar	Digital Quadrature	Phase-interleaved SCPA	Single-supply Class-G SCPA	Analog with Triple-mode
Resolution	**10-bit**			10-bit	9-bit	N/A	13-bit	N/A
Supply (V)	**1.1/2.5**			1.1/2.2		2.4/3.6	2.2	3.4
Frequency (GHz)	**1.2–2.8**			2–2.7		1.5–2.3	0.699–0.915	1.95
Peak Power (dBm)	**32.4**			28.8	26.3	30	27.1	28.4
Peak Efficiency	**53.8% DE 43.8% PAE**			30.8% PAE	22.9% PAE	45.9% DE	33.3% PAE	40.7% PAE
Modulation	**64-QAM 50 MHz**	**256-QAM 25 MHz**	**1024-QAM 10 MHz**	256-QAM 20 MHz	256-QAM 20 MHz	16-QAM OFDM	Cat-M1 16-QAM 1.4 MHz	3-GPP
Avg. Power	**25.37 dBm**	**24.13 dBm**	**22.14 dBm**	21.40 dBm	16.76 dBm	22.8 dBm	22.6 dBm	16.5 dBm
EVM	**–26.97 dB**	**–31.67 dB**	**–35.75 dB**	–30.7 dB	–30.2 dB	–24.7 dB	–30.2 dB	N/A
Area (mm^2)	**2.898**			0.5625*		7.2	5	2.12 + 0.66**

*: Core size; **: Whole circuit size + integrated passive device (IPD) size

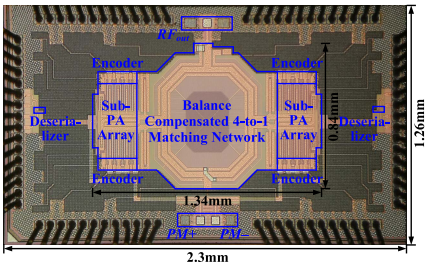

Fig. 5. Chip photograph of the proposed DPA.

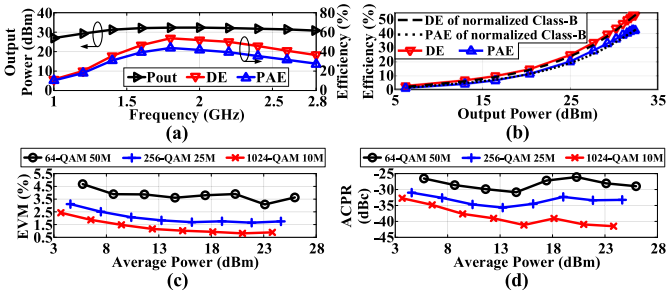

Fig. 6. Measured (a) output power, DE, and PAE, (b) DE and PAE versus output power, (c) EVM, and (d) ACPR versus average output power.

exhibited, where C_{bc} is chosen as 5.6 pF. As depicted in Fig. 4, the amplitude and phase imbalances are decreased by about 0.5 dB and 2°, respectively. Meanwhile, peak DE is enhanced by about 8%.

III. FABRICATION AND MEASUREMENT

A watt-level wideband DPA is fabricated using 40-nm CMOS technology, as shown in Fig. 5. The chip size is 2.3 mm × 1.26 mm, including all I/O pads, while the core size is 1.34 mm × 0.84 mm. The supply is 1.1 V/2.5 V. A vector signal generator is used to generate the phase-modulated signal. An arbitrary waveform generator is utilized to feed the amplitude data into the DPA. The output signal is measured with a spectrum analyzer after 20-dB attenuation. As depicted in Fig. 6(a), the DPA achieves 3-dB bandwidth larger than 80%, while the peak output power, DE, and power-added efficiency (PAE) are 32.4 dBm, 53.8%, and 43.8%, respectively. Here, the PAE includes power consumptions from drivers, encoders, and deserializers. The 1-D digital predistortion (DPD) is used to improve the linearity covering the power back-off region. As shown in Fig. 6(b)–(d), the measured 6-dB

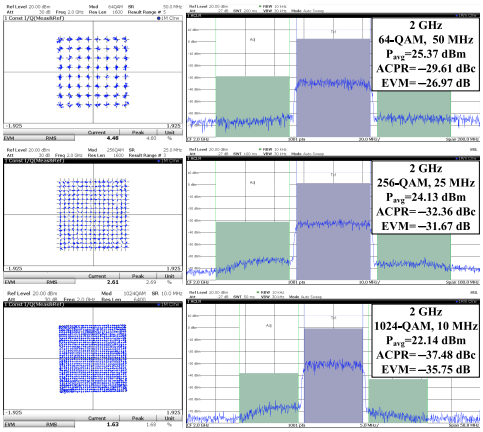

Fig. 7. Measured constellation diagram constellation diagrams and spectrum under different modulations at 2 GHz.

back-off DE and PAE are 29% and 24%, while error vector magnitude (EVM) and adjacent channel power ratio (ACPR) for a 25-MHz 256-quadratic-amplitude modulation (QAM) signal are 1.7% and −32 dBc, respectively. The back-off DE and PAE are similar to a normalized efficiency of Class-B PA. The modulation measurements for high-order QAM signals are shown in Fig. 7. The 50-MHz 64-QAM, 25-MHz 256-QAM, and 10-MHz 1024-QAM signals are tested at 2 GHz, which exhibits EVM of −26.97, −31.67, and −35.75 dB, respectively. In Table I, the proposed DPA has merits of wide bandwidth with competitive efficiency and output power compared with the state-of-the-art watt-level CMOS PAs.

IV. CONCLUSION

In this letter, a wideband watt-level high-efficiency DPA based on a balance-compensated matching network is proposed. To achieve high output power with a compact size, the 4-to-1 combining transformer is introduced. Meanwhile, to decrease the imbalance of the differential to single-ended 4-to-1 combining transformer, the imbalance compensation capacitor is utilized, which leads to enhancement of DPA efficiency. The proposed DPA shows the merits of watt-level output power, high efficiency, and wide operation bandwidth, which are attractive for applications of wireless communication and radar systems.

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