# InGaAs MOSHEMT *W*-Band LNAs on Silicon and Gallium Arsenide Substrates

Fabian Thome, Felix Heinz, and Arnulf Leuther

***Abstract*— This letter presents the design, performance, and analysis of four low-noise amplifier (LNA) monolithic microwave integrated circuits (MMICs) operating in *W*-band. Two LNA designs were fabricated in two variations of a 20-nm gate-length metal–oxide–semiconductor high-electron-mobility transistor (MOSHEMT) technology each. While for the first technology version the heterostructure is directly grown on the final gallium arsenide (GaAs) wafer, the second version uses direct wafer bonding to transfer the III–V heterostructure after the epitaxial growth to a silicon (Si) substrate. Based on the measured noise figure (NF) of the four MMICs over a comprehensive set of bias conditions, the impact of short-channel effects on the RF performance and possible improvements are analyzed. The first LNA covers an octave bandwidth with more than 15 dB of gain and an average NF (75–105 GHz) of 3.5 dB on a Si substrate. At 80 GHz, the second amplifier exhibits minimal NFs of 2.3 and 2.5 dB on GaAs and Si substrates, respectively. Compared to previously reported MOS- or Si-based technologies, the presented LNAs demonstrate state-of-the-art noise performance emphasizing the importance of electron confinement for highly scaled transistor technologies.**

***Index Terms*— *E*-band, high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), metal–oxide–semiconductor HEMTs (MOSHEMTs), millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), MOSFETs, silicon, *W*-band.**

## I. Introduction

In RECENT years, the gate-length scaling of Schottky-based high-electron-mobility transistor (HEMT) technologies reached fundamental limitations with feature sizes of 20–25 nm [1], [2] where a further performance improvement seems hardly feasible. A major challenge of the gate-length scaling is the simultaneously inevitable reduction of the Schottky barrier thickness to keep control over the 2-D electron gas (2DEG). This provokes an exponential increase of the gate-leakage current. Due to a larger barrier height, thin oxide barrier layers counteract increased gate-leakage currents while still facilitating effective channel control. Thus, metal–oxide–semiconductor HEMTs (MOSHEMTs) are promising candidates for further scaling of III–V technologies.

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In [3], we demonstrated a 20-nm gate-length MOSHEMT technology that reduces gate-leakage currents for an on-state bias by six orders of magnitude (<10 nA/mm) compared to our conventional 20-nm gate-length Schottky-contact HEMT technology. Still, short-channel effects, such as drain-induced barrier lowering, are major challenges since the electron confinement of the 2DEG is limited for conventional back barriers. The electron confinement is, therefore, improved by employing direct wafer bonding of the III–V heterostructure to a silicon (Si) substrate. The results are compared to a similar heterostructure which was directly grown on gallium arsenide (GaAs).

In this letter, we further investigate the electron confinement of a 20-nm gate-length MOSHEMT technology by comparing the low-noise performance of MOSHEMTs on Si and GaAs substrates. Therefore, two *W*-band (75–110 GHz) low-noise amplifier (LNA) monolithic microwave integrated circuits (MMICs) are designed and fabricated demonstrating state-of-the-art performance when compared to MOS-based technologies. Extensive noise-figure (NF) measurements are the basis for a subsequent discussion and conclusion.

## II. 20-nm InGaAs MOSHEMT Technology

The presented work is based on two variations of a 20-nm gate-length InGaAs MOSHEMT technology [3]. The electrons are confined in an $In_{0.8}Ga_{0.2}As$ channel with an $In_{0.52}Al_{0.48}As$ barrier layer toward the substrate. For the technology version on GaAs substrates, the heterostructure is directly grown by molecular-beam epitaxy on 100-mm GaAs wafers. For the version on silicon, the heterostructure is first grown on GaAs wafers in an inverted layer sequence. Afterward the III–V heterostructure is transferred to a 100-mm high-resistivity Si wafer by using direct wafer bonding. Therefore, a bonding oxide is deposited and chemical mechanical polishing is used to planarize the surface. Directly on top of the InGaAs channel, a bi-layer $Al_2O_3/HfO_2$ gate dielectric is deposited by atomic layer deposition. A detailed description of the MOSHEMT process is given in [3].

The technologies feature a maximum oscillation frequency of 640 GHz while having maximum transition frequencies of 200 and 275 GHz on Si and GaAs substrates, respectively. The dc transconductances ($g_m$) versus drain current ($i_d$) are depicted in Fig. 1. Both versions achieve clearly more than 2 S/mm. However, one of the major differences is that, up to 2 S/mm, MOSHEMTs on Si require only approximately half the current for a comparable $g_m$. Especially for low-noise technologies, this is an important characteristic [4].

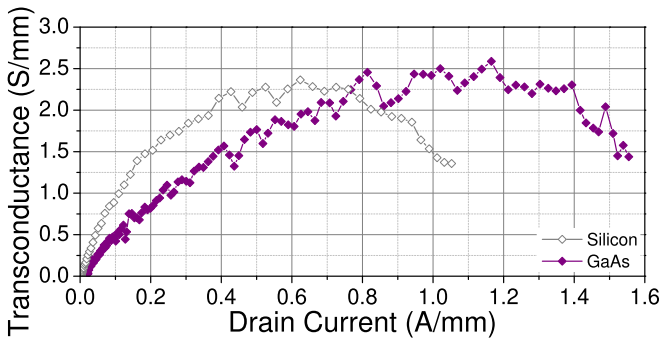



Fig. 1. Measured dc transconductance versus drain current (normalized to the gate width) of a 20-nm gate-length MOSHEMT on GaAs and Si substrates. The measurements are given for a drain voltage of 0.6 V.

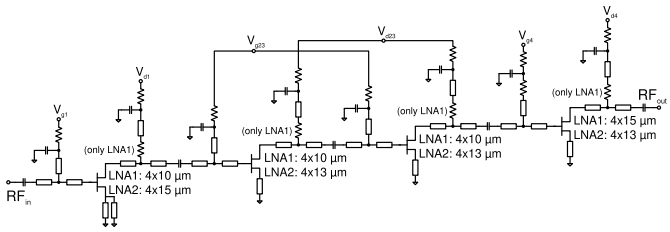


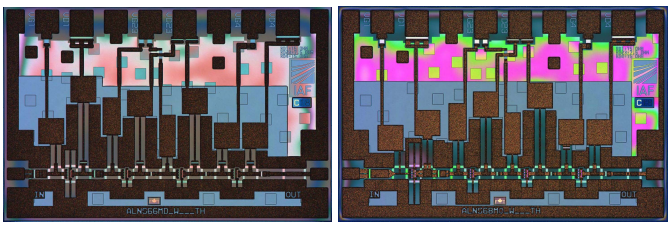

Fig. 2. Simplified schematic of the presented LNA MMICs.

## III. LNA MMIC Design

In this section, two *W*-band LNA designs are presented. Both circuits utilize a similar topology with four common-source stages. The first amplifier (LNA1) targets a wideband frequency response with a coverage of the entire WR-10 waveguide band and a minor compromise on the NF. The second amplifier (LNA2) is optimized for a minimum achievable NF in the lower *W*-band (up to 90 GHz). Both circuits use well-established design strategies for LNAs, including inductive source degeneration in the first stage for an improved simultaneous input noise and power matching. Furthermore, inductive source degeneration and high-impedance shorted bias stubs at gate, drain, and source are utilized in all stages for a wideband frequency response. The gate widths of the MOSHEMTs are mainly chosen for good small-signal performance and range between $4 \times 10$ $\mu$m and $4 \times 15$ $\mu$m. A simplified schematic of the amplifiers is illustrated in Fig. 2. For each technology version, the layout of the individual LNA designs is identical. Thus, a compromise is chosen offering good performance on GaAs and Si substrates. A well-proven passive design kit is already available for the GaAs technology. Hence, the LNAs are designed on GaAs and are subsequently verified for the Si version. Even though high-resistivity Si substrates are used, a slightly increased NF of a few tenth of decibel is expected. Photographs of the fabricated MMICs are shown in Fig. 3.

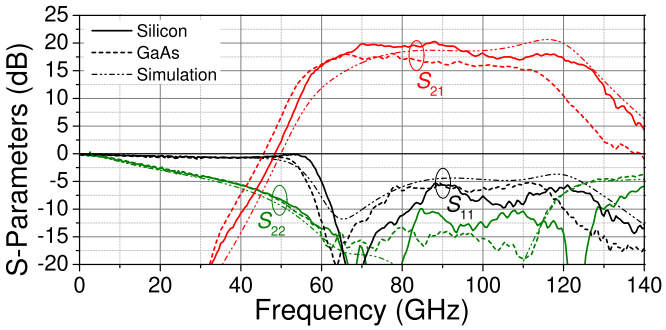
## IV. Measurement Results and Discussion

The fabricated MMICs are characterized on wafer. Each of the four MMICs is individually biased for an optimum NF. The S-parameter measurements are carried out from 0.01 to 140 GHz with an Anritsu VectorStar system. The S-parameters of LNA1 for both substrates are given in Fig. 4(a). LNA1 exhibits at least 15 dB of gain for more than

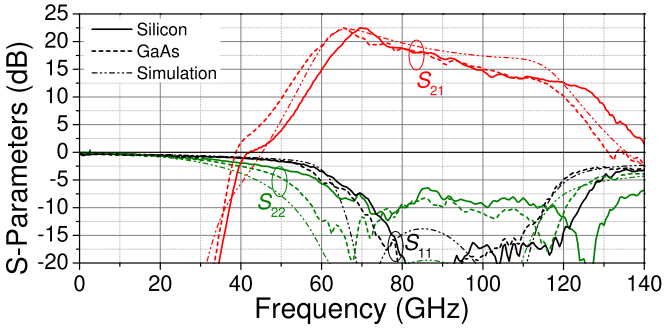


(a) (b)

Fig. 3. Chip photographs of the fabricated (a) LNA1 and (b) LNA2. In both cases, the chip size is $1.5 \times 1$ mm$^2$.




(a)




(b)

Fig. 4. Measured and simulated S-parameters of (a) LNA1 and (b) LNA2. The simulations are given for the MMICs on a GaAs substrate. The voltage at the drain of all HEMTs is 0.7 V. The gate voltage of all stages is identical and controlled so that LNA1 draws an $i_d$ in the first stage of 200 and 450 mA/mm on Si and GaAs substrates, respectively. For LNA2, $i_d$ of the first stage is controlled to 200 and 300 mA/mm on Si and GaAs substrates, respectively.

the WR-10 waveguide band. On Si, the covered bandwidth exceeds an octave. Fig. 4(b) shows the S-parameters of LNA2. Over a bandwidth of approximately 40 GHz, LNA2 exhibits more than 15 dB of gain with a peak value of 22.5 dB at the lower part of the band. The noise measurements are performed with an ELVA-1 WR-10 noise source, a commercially available mixer module (that limits the bandwidth to 75–105 GHz), and a Keysight NF analyzer. The measurement results are depicted in Fig. 5. LNA1 achieves an NF (75–105 GHz) of 3.3 and 3.5 dB on GaAs and Si, respectively. At 80 GHz, the measured NF of LNA2 is as low as 2.3 and 2.5 dB with an average NF (75–100 GHz) of only 2.8 and 3 dB on GaAs and Si, respectively. The measured noise performance shows minor deviations from simulations which is believed to be due to a slight imprecision of the noise matching predicted by the transistor model. A detailed summary of the measured performance of the four LNA MMICs is given

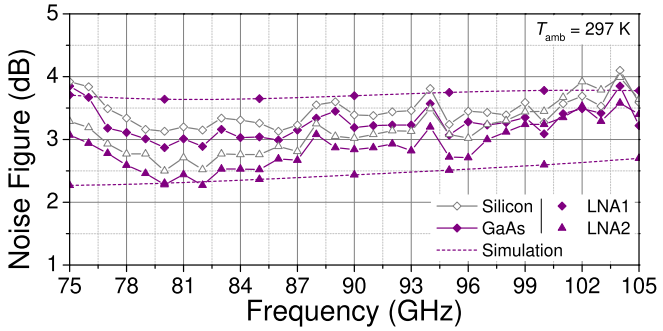


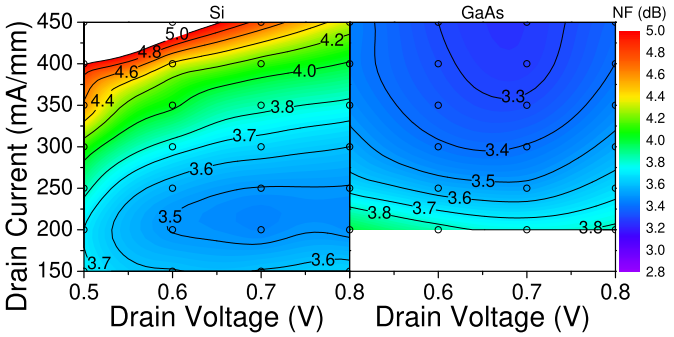

Fig. 5. Measured (solid lines) and simulated (dashed lines) NF of the presented LNA MMICs. The bias is similar as for the S-parameter measurements. For Si and GaAs substrates, the data are illustrated by open, gray and closed, purple symbols, respectively.

TABLE I
STATE-OF-THE-ART LNA MMICS

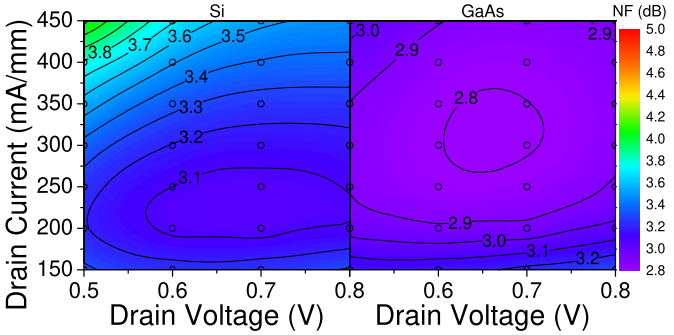
| Ref. | Technology | Freq. (GHz) | $P_{dc}$ (mW) | Gain (dB) | *NF* (dB) |
|---|---|---|---|---|---|
| [5] | 35-nm InGaAs mHEMT | 52–126 | 40.8 | 23–28 | 1.6–2.2* (avg. 1.9) |
| [6] | 50-nm InGaAs mHEMT | 60–124 | 30.3 | 25–33 | 1.6–2.6† (avg. 1.9) |
| [7] | 35-nm InP HEMT | 75–90 | 6.9 | 22.5–29 | 1.6–2.5 |
| [8] | 100-nm GaN HEMT | 86–98 | 128 | 20–24 | 3–5.1 |
| [9] | 22-nm FinFET CMOS | 67–79 | 10.8 | 17–20 | 3.7–4.5 |
| [10] | SiGe BiCMOS | 75–105 | 5.1 | 13.5–16.4 | 4.1–6 |
| [11] | 22-nm FDSOI | 77–108 | 16 | 15.2–18.2 | 5.8–6.6$ |
| This work (LNA1) | 20-nm InGaAs MOSHEMT | 58–112$^G$ | 51.6$^G$ | 15–18$^G$ | 2.9–3.9#G (avg. 3.3) |
| | | 59–127$^S$ | 33.3$^S$ | 15–20.3$^S$ | 3.1–4.1#S (avg. 3.5) |
| This work (LNA2) | 20-nm InGaAs MOSHEMT | 55–100$^G$ | 69.7$^G$ | 15–22.5$^G$ | 2.3–3.2§G (avg. 2.8) |
| | | 60–99$^S$ | 29.5$^S$ | 15–22.5$^S$ | 2.5–3.5§S (avg. 3) |

* 75–110 GHz; † 75–108 GHz; $ 94–96 GHz; # 75–105 GHz; § 75–100 GHz; $^G$GaAs substrate; $^S$Si substrate.

in Table I. For an advanced analysis of the different technology versions, the NFs of the four MMICs are measured for various bias conditions. Corresponding contour plots are illustrated in in Fig. 6. The first important observation is that both LNAs on Si yield a minimum of NF at a much lower $i_d$ (approx. 200 mA/mm) as the LNAs on GaAs. This directly affects the power consumption ($P_{dc}$) of the MMICs for which reason the LNAs on Si exhibit an optimum NF for a reduced $P_{dc}$. In our interpretation, for pinching off MOSHEMTs on GaAs, the electron concentration of the 2DEG shifts toward the back barrier. For MOSHEMTs on Si, the improved pinch-off behavior is due to an increased barrier height of the closely located interface of the bond oxide on the Si substrate. This means that the behavior of $g_m$, as shown in Fig. 1, is in line with the presented noise performance. A transfer of a similar process might be appealing also for other III–V technologies. A second important observation is that for MOSHEMTs on Si the NF depends less on the drain voltage as compared to MOSHEMTs on GaAs. For instance, at an $i_d$ of 200 mA/mm both LNAs on Si exhibit a variation of only 0.04 dB (0.6–0.8 V) which is two to three times higher for the versions on GaAs. This can




(a)




(b)

Fig. 6. Contour plots of the measured NF versus bias of (a) LNA1 and (b) LNA2. The MMICs on Si and GaAs substrates are shown on the left- and right-hand side, respectively. The bias points where the NF is measured and averaged from (a) 75 to 105 GHz and (b) 75 to 100 GHz are marked by circles.

be explained by short-channel effects, such as drain-induced barrier lowering, that are as well reduced by an improved electron confinement of MOSHEMTs on Si substrates.

## V. CONCLUSION

This letter presents the analysis and performance of four *W*-Band LNA MMICs that are fabricated in two variations of a 20-nm gate-length InGaAs MOSHEMT technology. The major highlights of this work are, first, as Table I illustrates, the demonstrated MMICs obtain state-of-the-art performance among MOS- and Si-based technologies. To the best of the authors' knowledge, these are the first MOSFET-based results with an NF of better than 3 dB in *W*-Band. Second, we demonstrate that bonding MOSHEMTs on a silicon substrate clearly improves short-channel effects which potentially allows a further gate-length scaling below feature sizes of 20 nm for RF applications. Therefore, we showed that improved dc characteristics are confirmed by a comprehensive set of measured NFs indicating a similar behavior. We believe that this opens new beneficial possibilities for an integration of MOSHEMTs and other III–V technologies with Si CMOS.

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