Low-Loss Millimeter-Wave SPDT Switch MMICs in a Metamorphic HEMT Technology

Fabian Thome, Arnulf Leuther, and Oliver Ambacher

Abstract—**This letter presents the design and performance of two single-pole double-throw (SPDT) switches operating in *V*-band (50–75 GHz) and *W*-band (75–110 GHz). The millimeter-wave (mmW) integrated circuits (MMICs) are fabricated in a 50-nm gate-length metamorphic high-electron-mobility transistor technology. Special attention was paid to the reduction of the insertion loss (IL). Thus, both switch MMICs achieve an IL of 1–1.6 dB (average 1.2 dB), covering the entire *V*-band and *W*-band, respectively. The isolation (ISO) of the switches is better than 31.6 and 28.5 dB, respectively. The input power for 1 dB of IL compression is at least 22 and 19 dBm, respectively. A wafer mapping of both circuits exhibits a high yield and low spread of IL and ISO. Based on the given results, the presented SPDT switch MMICs demonstrates state-of-the-art performance.**

Index Terms—**High-electron-mobility transistors (HEMTs), millimeter wave (mmW), mmW integrated circuits (MMICs), single-pole double-throw (SPDT), switch, *V*-band, *W*-band.**

I. Introduction

In a multitude of applications, RF switches are key building blocks. Especially, the transceivers where switches are the first and last semiconductor circuits in the receive and transmit paths, respectively, benefit from a low insertion loss (IL) and high isolation (ISO). For a receive path, the IL of a switch directly affects the system noise figure, whereas for a transmit path, the reduction in the output power can be a major issue. At millimeter-wave (mmW) frequencies, a low IL is even more challenging, e.g., due to the chip assembly. A monolithic integration can help to reduce such losses. Therefore, it is appealing to demonstrate low-loss switches in technologies with cutting-edge low-noise amplifiers (LNAs) and power amplifiers (PAs) [1], [2] in the same frequency range.

In the past, state-of-the-art single-pole double-throw (SPDT) switches, operating at mmW frequencies, were demonstrated using the well-known quarter-wave transformation shunt switch approach. Best results exhibit an IL as low as 1.1 dB utilizing gallium arsenide (GaAs) Schottky diodes or high-electron-mobility transistors (HEMTs) [3], [4], respectively. However, for the former, a monolithic integration with amplifiers seems hardly possible, and for the latter, the ISO is only about 20 dB.

Therefore, this letter investigates the design and performance of two full-waveguide-band SPDT switches for *V*-band (50–75 GHz) and *W*-band (75–110 GHz), which are realized in a 50-nm gate-length metamorphic HEMT (mHEMT) technology. In Section II, small- and large-signal considerations of shunt transistors are discussed. Major aspects of the loss reduction and the design of mmW switches are given in Section III. The small- and large-signal measurement results of the fabricated switch mmW integrated circuits (MMICs) are shown in Section IV. Section V concludes this letter and compares the results with the state of the art.

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II. Metamorphic Switch HEMTs

The presented work is based on the Fraunhofer IAF 50-nm gate-length InAlAs/InGaAs mHEMT technology [5]. For operation at mmW frequencies, an optimization of parasitic effects is important. The ON-resistance (R_{ON}) and OFF-capacitance (C_{OFF}) of switch devices are well-known parameters and strongly determine the achievable ISO in combination with the bandwidth. For the given technology, R_{ON} and C_{OFF} are $0.35\ \Omega \cdot$ mm and 0.24 pF/mm for control voltages (V_c) of 0.6 and −1 V, respectively. Furthermore, the inductance of a shunt transistor should be minimized since it increases the effective impedance of a switched-ON device and by that reduces the achievable ISO. Therefore, a coplanar-waveguide layout is used where the transistor fingers are placed between the signal strip and the ground plane. Thus, the inductances of through-substrate via holes are eliminated. The remaining inductance of the connection between the signal strip and ground plane is only minimal.

For shunt devices, the RF power handling is given by [6]

$$P_{max} = \frac{(V_{bd} - V_{th})^2}{2Z_0} \tag{1}$$

where V_{bd} is the gate-to-drain breakdown voltage, V_{th} is the threshold voltage, and Z_0 is the characteristic impedance at device level. For the utilized 50-nm mHEMT technology, V_{th} is about −0.3 V. The measured gate-leakage current for reverse bias is depicted in Fig. 1. When using a normalized gate current (normalized to the gate width) of 10 mA/mm as a limit, V_{bd} is about −4 V. Hence, an optimum control voltage for large-signal operation is about −2 V, which predicts a power handling of about 21.4 dBm. A simplified cross section of the utilized MMIC process is illustrated in Fig. 2(a).

III. Switch Design

The used design approach for the presented *V*-band and *W*-band switches is similar, as presented in [7]. In this letter,

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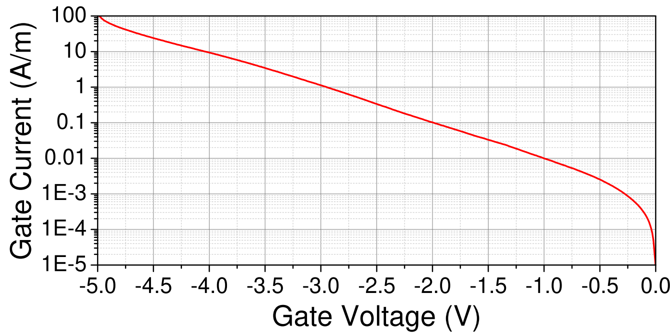


Fig. 1. Absolute value of the measured gate current versus gate voltage of a 50-nm mHEMT when biased with a drain-to-source voltage of 0 V.

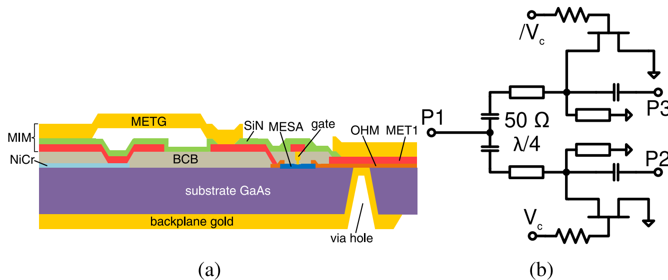
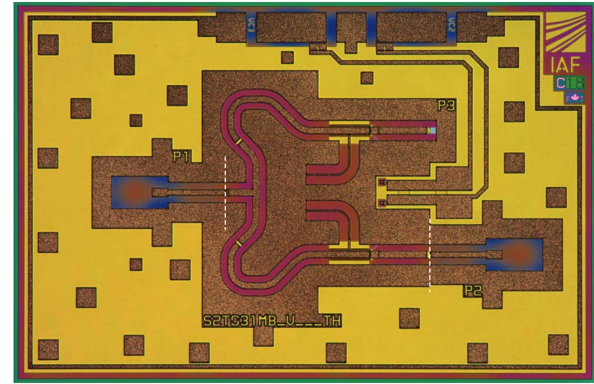


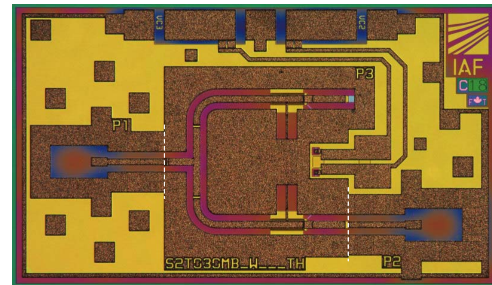
Fig. 2. (a) Simplified cross section of the layer stack of the utilized mHEMT technology [2]. (b) Simplified schematic of the presented SPDT switches.

special attention is paid to the IL reduction. A simplified schematic of the SPDT switches is shown in Fig. 2(b). The quarter-wave transformation transmission lines are chosen for the center of the dedicated waveguide band (V-band: 500 μm and W-band: 305 μm) and feature a characteristic impedance of 50 **Ω**. To increase the bandwidth, C_{OFF} is compensated by a shorted stub with a high characteristic impedance of about 81 **Ω**. All RF ports have a series metal–insulator–metal (MIM) capacitor as dc block.

For the IL reduction, three optimizations are important. First, the shorted stub is connected in the center of the shunt transistor. This avoids losses due to series transmission lines or T junctions that would be necessary to connect the stub outside the transistor. Hence, the shorted stub is connected to the shunt transistor by an air bridge. Second, a high ISO is important also for a low IL. Based on equations that are given in [7], the fraction of the IL that is due to signal leaking into the isolated branch can be calculated. Thus, the reduction of the IL of an SPDT switch is already 0.3 dB if the ISO is 30 dB instead of 20 dB. Therefore, this letter targets an ISO of about 30 dB, which requires a total gate width per shunt transistor of about 0.2 mm. Consequently, the V-band switch utilizes 2×100 μm shunt HEMTs. Since the transistor fingers should be considerably small compared to the quarter-wave line, it was decided to use 2×80 μm shunt HEMTs for the W-band switch. Third, to avoid additional transmission lines for the dc blocking at the common RF port, the series MIM capacitor is integrated into the T junction and the subsequent quarter-wave transformer. For an accurate description, the circuits are directly simulated in a 3-D EM simulator (CST Microwave Studio). The small-signal simulations are given together with the measurement results shown in Fig. 4. Based



(a)



(b)

Fig. 3. Chip photographs of the fabricated (a) V- and (b) W-band SPDT switch MMICs. In (a) and (b), the total chip size is 1.5×1 and 1.25×0.75 mm^2, respectively. Without RF and dc pads, the occupied chip area is 0.57×0.61 and 0.46×0.47 mm^2, respectively.

on simulations, the time span for switching ON or OFF a branch is below 1 ns.

Photographs of the fabricated MMICs are illustrated in Fig. 3. For test purposes, the layout of the MMICs is implemented for inline two-port measurement setups at which the third port is terminated on wafer.

IV. Measurement Results

The switches were measured with an Anritsu VectorStar from 0.01 to 150 GHz. The two-port S-parameters are calibrated to reference planes that are illustrated by white dashed lines in Fig. 3 with on-wafer calibration standards and a line-reflect-reflect-match (LRRM) calibration routine. The small-signal measurement results are given in Fig. 4 and show very good agreement with experiment. Both switches exhibit an IL of 1–1.6 dB (average 1.2 dB) over the corresponding waveguide bands. The return loss (RL) and ISO of the V-band switch are better than 10.8 and 31.6 dB, respectively. The W-band switch yields values of better than 12 and 28.5 dB, respectively. In Fig. 5, the average IL and ISO of both switches are depicted as a scatterplot for a wafer mapping. The mean values are indicated in Fig. 5 by black lines.

The large-signal measurements are also done on a wafer level. The input signal is provided by a chain of a signal generator, a frequency multiplier (V-band: x4 and W-band: x6), and in-house built PAs. For referencing the input power, 20-dB waveguide couplers are used, and the signal is measured at the coupled port by a Keysight spectrum analyzer and smart harmonic waveguide mixers. To prevent compression of the

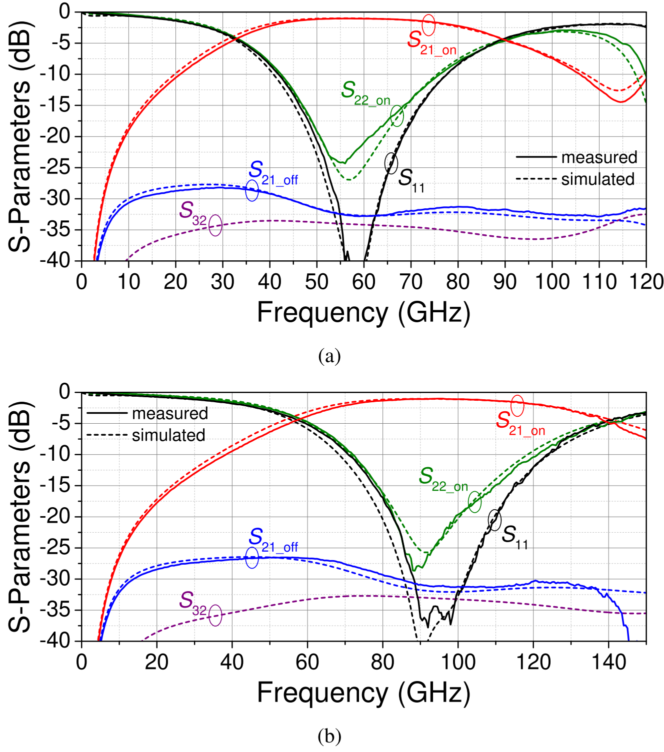


Fig. 4. Measured and simulated S-parameters of the presented (a) V-band and (b) W-band SPDT switches. The control voltages for switched-ON and switched-OFF HEMTs are 0.6 and −1 V, respectively.

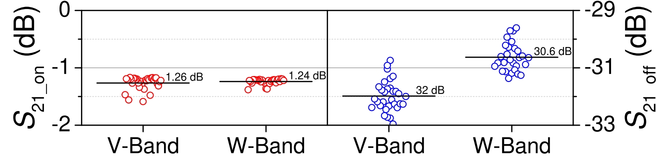


Fig. 5. Wafer mapping of the V- and W-band switches, including 31 and 29 measured cells, respectively, out of 37 cells on a wafer. For the scatterplot, S_{21} for ON- and OFF-states is averaged over the corresponding waveguide bands.

TABLE I
STATE-OF-THE-ART LOW-LOSS mmW SPDT SWITCHES

Ref.	Techn.	Freq. (GHz)	RL (dB)	P_{1dB} (dBm)	ISO (dB)	IL (dB)
[8]	InGaAs pHEMT	50–70	>9	>10	32–41.3	1.3–1.8
[9]	GaAs pHEMT	40–85	>10	n/a	>31	1.2–2
[10]	GaN HEMT	60–90	>12	>29	22.5–25.5	1.5–1.8
[3]	GaAs Diode	75–110	>9.7	n/a	>31	1.1–1.6
[4]	GaN HEMT	72–131	>10	>25	18.5–21.5	1.1–2
[11]	SiGe Diode	77–133	>10	>24	19–22	1.4–2
[7]	InGaAs mHEMT	143–305	>7	n/a	13.5–22.8	1.5–2.5
This work (switch 1)	InGaAs mHEMT	50–75 42.5–76	>10.8 >10	>22	31.6–32.8 29.7–32.8	1–1.6 1–1.7
This work (switch 2)	InGaAs mHEMT	75–110 72–120	>12 >10	>19	28.5–31.4 28–31.4	1–1.6 1–1.9

mixers, an additional 10-dB attenuator is used before the smart mixers. The PAs limit the input drive at 60 and 94 GHz to 22 and 19 dBm, respectively. At the output, the signal is damped by a 10-dB attenuator and is measured by a waveguide power meter. The signals are calibrated with respect to the

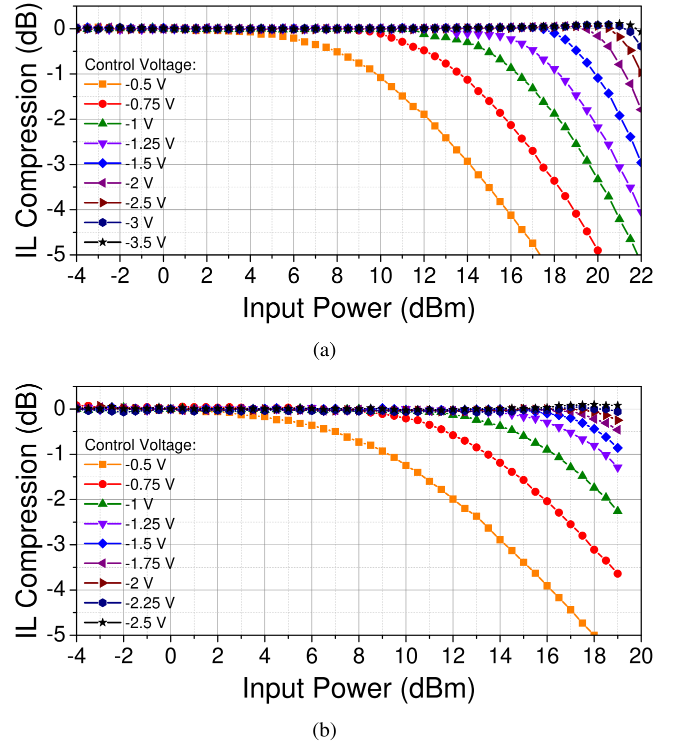


Fig. 6. IL compression versus continuous-wave input power at port 1 of the presented (a) V- and (b) W-band SPDT switches. The control voltage of the switched-ON HEMT at port 3 is kept constant at 0.6 V, whereas the bias of the switched-OFF HEMT at port 2 is varied from (a) −0.5 to −3.5 and (b) −0.5 to −2.5 V, respectively. The test frequencies are (a) 60 and (b) 94 GHz.

RF probe tips. The single-tone large-signal measurements are shown in Fig. 6 for various control voltages of the switch-OFF HEMT. At −1 V, the input power for 1-dB compression (P_{1dB}) for both switches is approximately 16 dBm and can be pushed above 22 and 19 dBm (limited by the setup), respectively, by adjusting V_c for the switched-OFF HEMT. The variation of S_{21_on} for the given bias sweep is below 0.08 dB.

V. CONCLUSION

In this letter, the design and performance of V- and W-band SPDT switches are presented. The results of the demonstrated MMICs are summarized in Table I and compared with state-of-the-art results. As the comparison highlights, the presented switch MMICs exhibit state-of-the-art performance with regard to IL, isolation, and bandwidth. One should keep in mind that, in general, there is a tradeoff between low IL and high ISO. Thus, to the best of our knowledge, this is the lowest IL for SPDT switches in the frequency range from 50 to 110 GHz, where only [3] achieves comparable performance. A major benefit, compared to diode-based circuits, is that the presented circuits can be easily integrated with state-of-the-art LNAs and PAs on a single MMIC.

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