A 4-W Doherty Power Amplifier in GaN MMIC Technology for 15-GHz Applications

Roberto Quaglia, *Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE*, Jorge Julian Moreno Rubio, Marco Pirola, *Member, IEEE*, and Giovanni Ghione, *Fellow, IEEE*

***Abstract*— This letter presents an integrated Doherty power amplifier (PA) in 0.25-μm GaN on SiC process. Designed for 15-GHz point-to-point radios, the PA exhibits an output power of 36 ± 0.5 dBm between 13.7 and 15.3 GHz, while at 14.6 GHz, it shows a 6-dB output back-off efficiency higher than 28%. Modulated signal measurements applying digital predistortion demonstrate the compatibility of the amplifier with point-to-point radio requirements. To the best of our knowledge, this PA has the highest back-off efficiency for the 15-GHz band, and is the first GaN Doherty in the Ku-band.**

***Index Terms*— Doherty, gallium nitride, microwave monolithic integrated circuit (MMIC).**

I. Introduction

INCREASING the power amplifier (PA) efficiency is crucial in high-capacity microwave radios, where the thermal issues are critical due to the compact radio module configuration. The adoption of high peak-to-average power ratio (PAPR) modulated signals forces the PA to operate at large output backoff (OBO) to maintain an acceptable linearity, limiting the efficiency of the PAs commonly adopted for microwave radios well below 10% and 20% for GaAs and GaN-based examples, respectively. This letter presents the first example of design, for the 15-GHz point-to-point radio band, of a microwave monolithic integrated circuit (MMIC) Doherty PA (DPA) [5] based on 0.25-μm GaN HEMTs. This technology has already been exploited for the state-of-the-art DPAs up to the *C*-band, while has never been tested at 15 GHz for the design of an advanced PA. Table I compares the proposed MMIC with similar DPAs in terms of frequency band, maximum output power, and drain efficiency at saturation and 6-dB OBO. The DPA of [2], thanks also to the use of a more advanced technology (0.15-μm GaN) and of distributed networks and a large area, shows similar performance at higher frequency. On the other hand, it can be observed that the proposed DPA compares well with the reported examples, despite the use of a technology at the limit of its capabilities.

TABLE I
COMPARISON WITH SIMILAR MMIC DPAs

Ref.	Tech.	Freq. (GHz)	P_{OUT} (W)	Gain (dB)	η_{SAT} (%)	η_{OBO} (%)	Area (mm^2)
[1]	GaAs	17	0.3	8	44	30	n.a.
[2]	GaN	21-24	4	17	43	26	6.8
[3]	GaAs	23-25	1.2	12.5	38	20	4.29
[4]	GaN	10	4	9.2	57	48	8.74
This	GaN	14.6	4	7	40	28	4.96

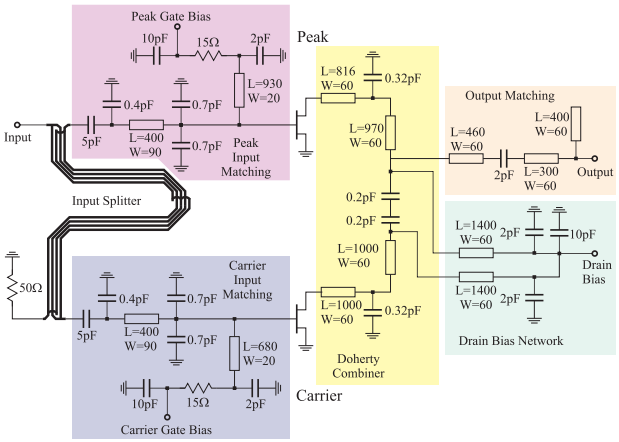

Fig. 1. Schematic of the integrated 15-GHz DPA. Lengths and widths in μm.

II. Design

The designed DPA is based on the united monolithic semiconductor (UMS) 0.25-μm GaN HEMT process (SiC substrate and two metal layers), characterized by a power density of 4 W/mm at the foundry suggested drain bias voltage of 25 V. Given the target output power of 4 W, and considering reasonable margins, the selected total periphery is of 1.2 mm. An even DPA configuration has been adopted, with the same device for carrier and peak stages. According to the foundry recommendations on maximum gate width and number of fingers, the 8×75 μm device has been chosen. At 15 GHz, the power gain on the optimum power load is around 11 dB, meaning an ideal DPA gain of around 8 dB. Accounting for the additional losses, it is clear that the design constraints are rather close to the limits of this technology. Fig. 1 shows the circuit schematic of the MMIC. Given the small area

Manuscript received December 20, 2016; accepted January 6, 2017. Date of publication March 22, 2017; date of current version April 6, 2017. This work was supported by the EU Horizon 2020 research and innovation Marie Skłodo wska Curie programme under Grant 654987.

R. Quaglia is with the Centre for High Frequency Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: quagliar@cardiff.ac.uk).

V. Camarchia, M. Pirola, and G. Ghione are with the Department of Electronics, Politecnico di Torino, 10129 Torino, Italy (e-mail: vittorio.camarchia@polito.it).

J. J. Moreno Rubio is with the Department of Electronics, Universidad Pedagógica y Tecnológica de Colombia, Sogamoso 150003, Colombia (e-mail: jorgejulian.moreno@uptc.edu.co).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2017.2678440

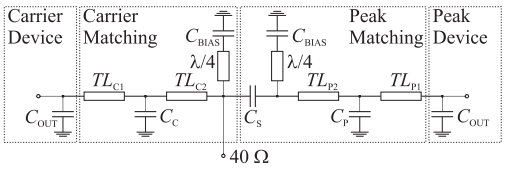

Fig. 2. Adopted topology of the DPA output combiner.

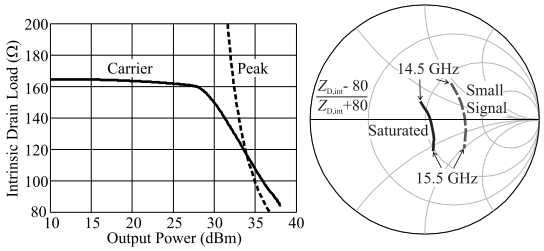

Fig. 3. Simulated loads at the intrinsic plane. Left: versus output power; carrier (solid line), peak (dashed line). Right: versus frequency, for carrier device.

available, no driver stage has been included in the MMIC. The limited area also forced to use semilumped matching networks, with higher losses and sensitivity with respect to a distributed approach employed for example in [2] and [4]. An optimum intrinsic load of 80 Ω, estimated with simple load-line considerations and refined through large signal simulations, has been chosen. In a DPA optimized for first efficiency peak at 6-dB OBO, the common node load results of 40 Ω then transformed to the external 50-Ω load by the output matching network. The carrier output matching network absorbs the device reactive effects and synthesizes an impedance inverter with characteristic impedance of 80 Ω. The peak output matching compensates for the reactive effects only, since it results loaded with an equivalent 80-Ω load at saturation. The output combiner uses a semilumped topology, see details in Fig. 2. Small capacitances, resulting critical from a sensitivity point of view, are realized by a pair of series capacitors. Fig. 3 (left) shows the simulated intrinsic drain impedance $Z_{D,\text{int}}$ versus output power at 15 GHz for the carrier and peak devices, respectively, demonstrating the correct load modulation. Fig. 3 (right) shows the carrier device $Z_{D,\text{int}}$ versus frequency at back off and at saturation, on a Smith chart normalized to R_{opt}, suggesting a rather good-frequency behavior of the network.

A Lange 3-dB coupler has been used as input splitter. Simulations with Keysight momentum, used for its optimization, show good amplitude (±0.35 dB) and phase (±2°) balance at the output ports. Lange couplers guarantee good input return loss (IRL) when the output ports are loaded with similar terminations. Thus, in order to provide matching at higher power, where the two devices show similar gate impedance, the same input networks for carrier and peak have been adopted. On the other hand, in low-power conditions, the different bias point of peak and carrier will lead to a worse IRL. Broadband stabilization, empirically assessed through linear loop simulations, has been enforced through gate resistors.

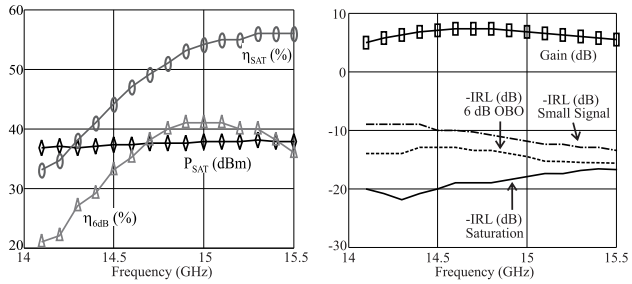

Fig. 4. CW simulations of the DPA versus frequency. Measurements in Fig. 7.

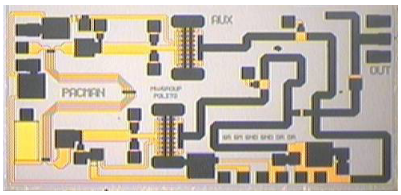

Fig. 5. Microscopic picture of the fabricated MMIC. Size is 3.1×1.6 mm^2.

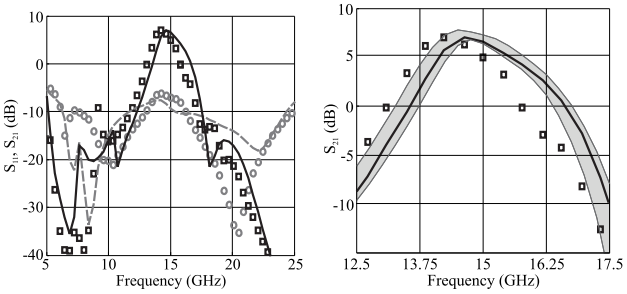

Fig. 6. Scattering parameters versus frequency. Simulated: S_{11} (gray dashed line) and S_{21} (black solid line). Measured: S_{11} (gray circles) and S_{21} (black squares). Right: Monte Carlo results (± standard deviation) on S_{21}: gray area.

Fig. 4 shows the simulated CW behavior versus frequency of the DPA in terms of output power and drain efficiency at 3-dB gain compression, 6-dB OBO drain efficiency, small signal gain, together with IRL at three different drive levels.

III. Experimental Characterization

The fabricated MMIC DPA (Fig. 5) has been characterized on-wafer in small-, large-, and under-modulated signal. DC bias has been provided with a dc-probe, with external surface mount by-pass capacitors to enhance low-frequency stability and isolation. The bias point has been set to $V_{\text{DD}} = 25$ V, with a carrier current $I_{\text{DD}} = 40$ mA, and peak stage biased at $V_{\text{GP}} = -4.8$ V. No oscillation issues have been experienced, both at small- and large-input drive. Fig. 6 reports a comparison between the measured and simulated scattering parameters. The agreement, generally satisfactory in the 5–25 GHz band, is good in the operative band around 15 GHz, apart for a shift of 400 MHz toward lower frequency of S_{21}. The S_{11} results, in band, are a few dB worse than simulated, but still acceptable, also considering that the design was optimized to ensure good matching in large signal operation. Monte Carlo simulations considering the foundry statistical distribution of passive elements have been carried

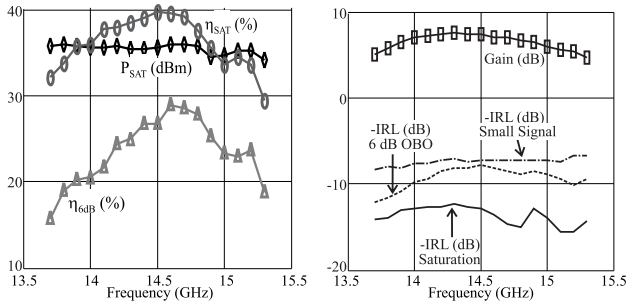

Fig. 7. CW measured results versus frequency.

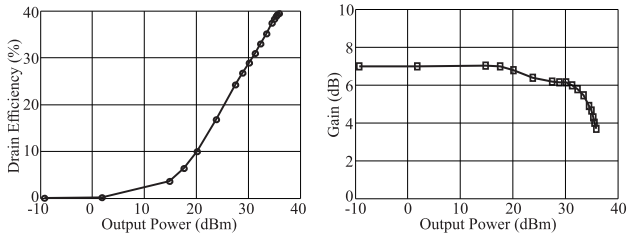

Fig. 8. CW characterization. Drain efficiency (left) and gain (right) versus output power at 14.6 GHz.

out, and the results on S_{21} are reported in Fig. 6. The S_{21} shift must be partly ascribed to process deviations on passive structures, and partly to active device deviations and EM simulation inaccuracies. Single tone CW measurements have been carried out on the 13.7–15.3 GHz band, i.e., where the PA shows a gain higher than 5 dB. Fig. 7 shows the CW measured results versus frequency. An output power of 36 ± 0.5 dBm at 3-dB gain compression is achieved on the full bandwidth, with a corresponding drain efficiency higher than 29%. The 6-dB output back-off efficiency is higher than 16% on the full bandwidth, with the best result at 14.6 GHz, where it stands above 28%. With respect to the simulated results shown in Fig. 4, a lower drain efficiency is generally achieved. This deviation is partly due to the foundry device model that, to the best of our knowledge, has not been completely tested in class C at this frequency. In fact, to obtain a satisfactory flat gain versus drive response, the peak bias point has been properly retuned, thus reducing efficiency and maximum output power. Regarding the IRL, as expected from the previously drawn considerations on the input matching network design, it improves for increasing power drive. Fig. 8 reports the CW power sweep at 14.6 GHz, showing the gain and drain efficiency trends versus output power. A reasonably flat gain versus drive behavior can be observed.

To test the linearizability of the DPA, system level characterization has been performed [3]. Adopting a microwave arbitrary waveform generator (ESG4433B of Keysight), a typical point-to-point 256-quadrature amplitude modulated signal, with 28-MHz channel bandwidth and PAPR of 7.4 dB is applied to the DPA. The DPA output signal is collected with a vector signal analyzer (MXA9020A of Keysight), and elaborated to evaluate the spectrum and to extract the

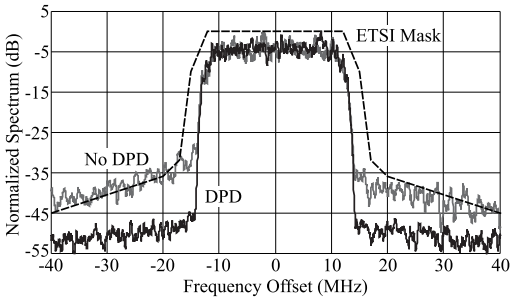

Fig. 9. Measured spectrum versus frequency with modulated signal (256-QAM, 28-MHz channel) at average power of 29 dBm. Gray trace: without DPD. Black trace: with DPD. Dashed line: ETSI mask.

predistortion model. The predistorted signal is then fed into the generator, and the output collected to verify the compliance with the system linearity specifications. Fig. 9 compares the PA output spectra with and without predistortion, for center frequency of 14.6 GHz and average output power of 29 dBm. Applying a simple memory polynomial predistortion of the sixth odd order with two memory taps [6], the adjacent channel power can be reduced, and the mask compliance (reference mask for a 6LA system [7]) achieved with an average drain efficiency of 28%. This suggests that the adoption of 0.25-μm GaN technology is compatible with advanced PA design in the Ku-band, and that the proposed MMIC design could be applied to product development.

IV. Conclusion

Design and characterization of a Ku-band MMIC DPA have been presented, showing an output power of around 4 W and 6-dB back-off efficiency of 28%. Modulated signal measurements show that the device is compatible with linearity requirements after applying a simple predistortion.

References

[1] C. F. Campbell, "A fully integrated Ku-band Doherty amplifier MMIC," *IEEE Microw. Guided Wave Lett. (until)*, vol. 9, no. 3, pp. 114–116, Mar. 1999.

[2] C. Campbell *et al.*, "A K-band 5W Doherty amplifier MMIC utilizing 0.15 μ m GaN on SiC HEMT Technology," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Oct. 2012, pp. 1–4.

[3] R. Quaglia, V. Camarchia, T. Jiang, M. Pirola, S. D. Guerrieri, and B. Loran, "K-Band GaAs MMIC Doherty power amplifier for microwave radio with optimized driver," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2518–2525, Nov. 2014.

[4] M. Coffey *et al.*, "A 4.2-W 10-GHz GaN MMIC Doherty power amplifier," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Oct. 2015, pp. 1–4.

[5] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, Feb. 2015.

[6] R. Quaglia *et al.*, "Real-time FPGA-based baseband predistortion of W-CDMA 3GPP high-efficiency power amplifiers: Comparing GaN HEMT and Si LDMOS predistorted PA performances," in *Proc. Eur. Microw. Conf.*, Oct. 2009, pp. 342–345.

[7] *Fixed Radio Systems; Characteristics and Requirements for Point-to-Point Equipment and Antennas; Part 2-2.*, document ETSI EN 302 217-2-2, 2012.