Current Shared Cascade Structure for the Driver Stages of Switching Mode RF Power Amplifiers

Hoyong Hwang, *Student Member, IEEE*, and Changkun Park, *Member, IEEE*

***Abstract*—In this work, we propose a current shared cascade (CSC) structure for the driver stages of switching mode RF power amplifiers (PAs); this CSC is designed using a differential structure. The CSC structure is composed of a first driver stage stacked on top of a second driver stage. The first and second driver stages share a dc current and the effective supply voltages of each driver stage become approximately half the value of the supply voltage of the power stage. The CSC structure enhances the power efficiency because no additional regulator, usually required for the supply voltage of the driver stages, is necessary. We designed the PA to prove the feasibility of the proposed CSC structure. From the measured results, we successfully verify the feasibility of the proposed topology.**

***Index Terms*—Amplifier, cascade, efficiency, supply voltage.**

I. Introduction

RECENTLY, efficiency improvement methods for RF CMOS power amplifiers (PAs) have been studied vigorously [1]–[3]. The main stream of the studied methods can be decomposed into modifications of the structure and optimization of the design parameters. However, the modification techniques lead to requirements of additional circuit elements and increasing complexity of the PA and the optimization techniques require device models with very high accuracy; hence, several revisions are needed. Additionally, most studies related to efficiency improvements have focused on the power stage of the PA because most dc power is dissipated in the power stage [4]. Although most of the power consumption is known to occur in the power stage, reducing power consumption in the driver stage can also be seen as an essential task in the improvement of the efficiency of PAs. Recently, some studies have focused on reducing power consumption in the driver stages in order to improve the overall efficiency [5], [6].

In this work, we propose a current shared cascade (CSC) structure that can reduce the power consumption in the driver stages. To verify the feasibility of the proposed CSC structure, we designed a switching mode RF CMOS PA for polar transmitter applications.

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The authors are with the School of Electronic Engineering, College of Information Technology, Soongsil University, Seoul 156-743, Korea (e-mail: pck77@ssu.ac.kr).

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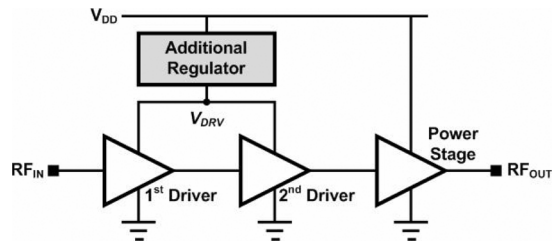


Fig. 1. Conceptual block diagram of a typical PA with a regulator.

II. Typical Switching Mode RF CMOS Power Amplifier

In general, typical switching mode RF CMOS PAs use an identical supply voltage, V_{DD}, in the driver and power stages in order to avoid increasing the complexity of the PA. However, if V_{DD} is optimized in the power stage in order to obtain high maximum output power, V_{DD} is generally higher than the optimum value of the supply voltage for the driver stage. An unnecessary amount of dc power is therefore dissipated in the driver stages.

In order to avoid unnecessary power consumption in the driver stage, V_{DRV}, which is the supply voltage of the driver stage, must differ from V_{DD}, as shown in Fig. 1. From the results of earlier work [5], [6], it is known that the optimized value of V_{DRV} is approximately half that of V_{DD}. With an optimized value of V_{DRV}, the efficiency of the PA can be elevated. However, in reality, an additional regulator is required to separate V_{DRV} from V_{DD}. Accordingly, if we include the power consumption in the regulator, the efficiency improvement effects are degraded.

III. Proposed Current Shared Cascade Structure

A. Principle of the Current Shared Cascade Structure

In this work, unlike the topology shown in Fig. 1, we propose a CSC structure in order to improve the efficiency of the PA without an additional regulator. The simplified topology of a PA using a CSC structure in the driver stages is shown in Fig. 2(a). The first driver stage is stacked on top of the second driver stage. The PA is designed using a differential structure. I_1 and I_2 in Fig. 2(a) indicate the differential current and $I = I_1 + I_2$. The current I is constant for fundamental and odd harmonics frequencies. Accordingly, the V_X node shown in Fig. 2(a) becomes a virtual ground for fundamental and odd harmonics frequencies. If the first and second driver stages are designed using the same size transistors, the on-resistances of the driver stages, R_{DRV1} and R_{DRV2}, are identical, as depicted in Fig. 2(b). Additionally, I_{DRV1} and I_{DRV2} are identical because R_{DRV1} and

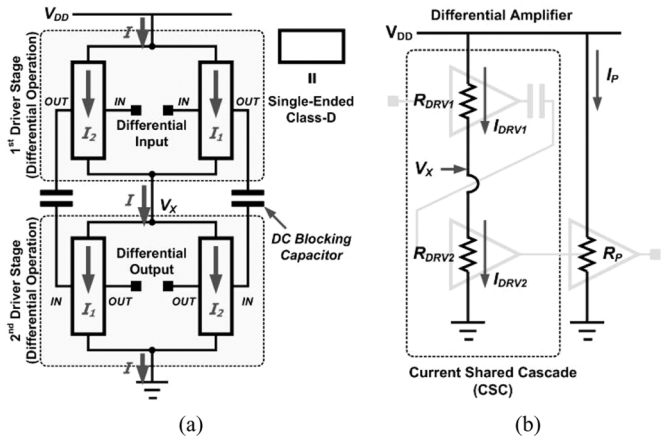


Fig. 2. Conceptual diagram of the proposed current shared cascade structure: (a) block diagram and (b) simplified equivalent circuit under dc condition.

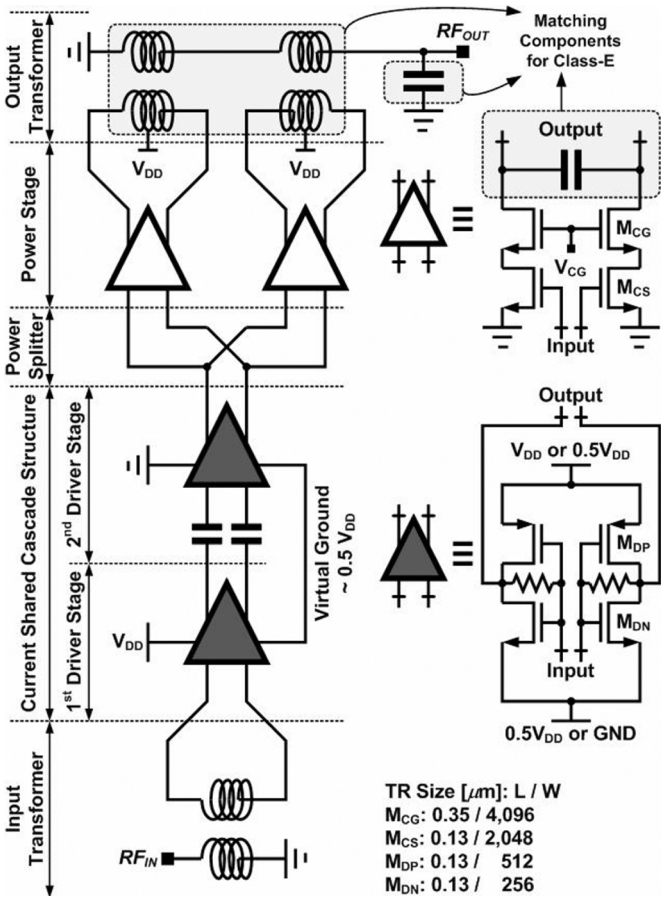


Fig. 3. Simplified schematic of PA using the proposed CSC structure.

R_{DRV2} are connected in series. Hence, V_X is naturally determined as approximately half of V_{DD}. The V_X node simultaneously becomes the ground for the first driver stage and the supply voltage for the second driver stage. The effective supply voltages of the first and second driver stages are $V_{DD} - V_X$ and V_X, respectively.

The dc voltage drop in the first driver stage becomes nearly identical to that in the second driver stage. Thus, in spite of the absence of a regulator, the effective V_{DRV} becomes approximately half of V_{DD}, like the V_{DRV} shown in Fig. 1. The driver stages are connected as a cascade structure; the dc current is

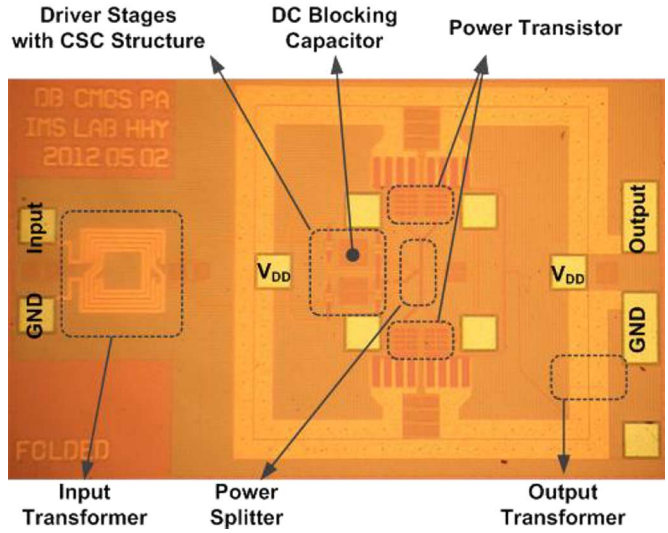


Fig. 4. Photograph of the implemented PA.

shared between the two driver stages. By using the CSC structure in the driver stages, we can eliminate the loss that arises from the regulator required to make V_{DRV} be half of V_{DD}. If the current consumption in the driver stage of the conventional amplifier shown in Fig. 1 is $I_{DRV1} + I_{DRV2} = I_{DRV}$, the proposed driver stages consume almost half of I_{DRV} because I_{DRV1} is reused in the second driver stage.

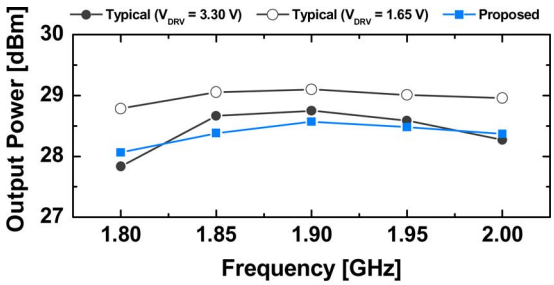
B. Design of the Power Amplifier

We designed a switching mode RF CMOS PA to verify the feasibility of the CSC structure. All of the first driver, second driver, and power stages are designed using a differential structure. The first and second driver stages are designed using class-D topology with feedback resistors. A dc blocking capacitor is used between the first and second driver stages to eliminate undesired effects that arise from the different voltage levels between the first stage output and the second stage input. On the other hand, the first driver stage is stacked on top of the second driver stage in order to allow the removal of the dc blocking capacitor between the second driver and the power stages. If the second driver stage is stacked on top of the first driver stage, a dc blocking capacitor between the output of the second driver stage and the input of the power stage becomes essential.

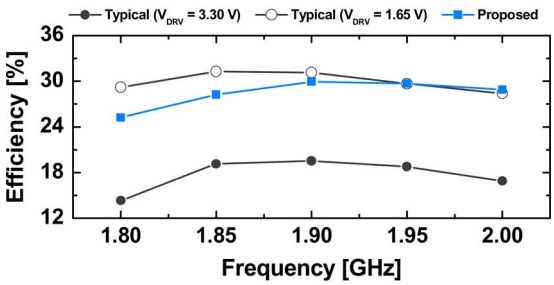
A distributed active transformer is used as the output matching network of the power stage in order to complete the fabrication of an efficient class-E PA [1]. The class-E matching network is completed using the MIM capacitors and the inductance of the output transformer. The power stage is designed using a cascode structure in order to solve the breakdown problems. A simplified schematic of the PA using the proposed CSC structure is shown in Fig. 3.

IV. Measurement Results

Fig. 4 provides a photograph of the designed PA with operating frequency of 1.9 GHz. 0.13 μm RFCMOS technology is used, in which six metal layers are provided. The top metal layer is implemented using copper with a 3 μm thickness. The V_{DD} and gate bias of the common-gate transistor of the power stage



(a)



(b)

Fig. 5. Measured frequency responses: (a) output power and (b) overall power added efficiency.

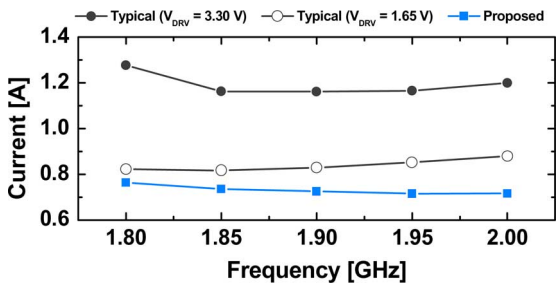


Fig. 6. Measured currents vs. operating frequency.

TABLE I
COMPARISONS OF CMOS POWER AMPLIFIERS

Ref.	Freq. [GHz]	P_{OUT} [dBm]	PAE [%]	Process [nm]	Size [mm^2]
[2]	2.4	31	33	180	2
[7]	2.5	30.8	30.6	180	2.0 × 1.2
[8]	2.4	21	33	180	0.9 × 0.6
[9]	1.8	33	31	180	1.8×1.65
This work (Proposed)	1.9	28.6	30	130	1.7×1.0

are 3.3 V and 2.8 V, respectively. As can be seen in Fig. 3, in order to obtain a fair comparison between the performances of the proposed and typical structures, all of the design parameters of the PA are identical to those in the earlier work [5]. Additionally, the proposed amplifier is fabricated using the same technology as that used in the earlier work. A difference between this and earlier works is that in this work a dc blocking capacitor is added between the first and the second driver stages.

Fig. 5 shows the measured frequency responses. The input power is fixed at 13 dBm. To obtain fairly compared results, we also show the results of a typical PA with $V_{DRV} = 1.65$ V and $V_{DRV} = 3.3$ V. As can be seen in Fig. 5(a), the maximum output powers of the typical and the proposed PAs are nearly the same. However, the efficiencies are different, as shown in Fig. 5(b). In these measured results, the loss induced by the regulator for a typical amplifier with 1.65 V of V_{DRV} is not included. The efficiency of the proposed amplifier is approximately the same as that of a typical amplifier with a V_{DRV} of 1.65 V and is higher than that of a typical amplifier with a V_{DRV} of 3.3 V. However, if the loss induced by the regulator, which is essentially required for a typical amplifier with a V_{DRV} of 1.65 V, is included in the calculation of the efficiency, the efficiency of the typical amplifier will be degraded further. Fig. 6 shows the measured currents of the typical and the proposed amplifiers. As can be seen in Fig. 6, among the measured amplifiers, the proposed amplifier consumed the lowest amount of current. Table I shows the comparisons of CMOS PAs [7]–[9].

V. CONCLUSION

In this work, we propose a current shared cascade (CSC) structure for the driver stages of an RF CMOS PA. Using the CSC structure, we obtain supply voltages for the driver stages that are effectively half of V_{DD} of the power stage; this is in spite of the absence of an additional regulator to generate half of V_{DD}. Undesired power consumption in the additional regulator is therefore removed. Additionally, a PA using the CSC structure is designed. From the measured results obtained, the feasibility of the proposed CSC structure is successfully proved.

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