A 0.18-μm CMOS Dual-Band Frequency Synthesizer With Spur Reduction Calibration

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***Abstract*—This letter presents a 0.18 μm CMOS dual-band frequency synthesizer with charge-pump current mismatch calibration to reduce reference spurs. To enhance calibration accuracy the high-resolution phase detector (HRPD) is incorporated in this work. The measured output spur level is less than −63 dBc after the calibration circuits are activated and the reference spur reduction is more than 5.6 dB throughout the whole frequency range. The frequency synthesizer draws 16 mA from a 1.8 V power supply, and the covered frequency bands are 5.18–5.32 GHz and 5.74–5.82 GHz.**

***Index Terms*—Charge-pump (CP) current calibration, frequency synthesizer, phase-locked loop (PLL), spur suppression.**

I. Introduction

CHARGE PUMPs (CPs) are extensively used in the phase-locked loops (PLLs) to convert the phase/frequency difference between the output and reference signals into a proportional voltage for the voltage-controlled oscillators (VCOs). The mismatch between the pump and dump currents of a conventional CP in a PLL will lead to poor reference spurs and static phase error [1]. The charge-pump current mismatch results from device mismatch and channel-length modulation of the transistors and the issue gets worse for the advanced CMOS technology.

One of the bottlenecks for mismatch calibration of charge-pump current is the minimum detectable phase error of a phase detector (PD). The detectable phase error for a typical 0.18-μm CMOS bang-bang phase detector (BBPD) is around 45 ps and it calls for the need of a technique to improve the minimum detectable phase error for enhancing the accuracy of mismatch calibration. The high-resolution phase detector (HRPD) is developed to enlarge the phase error before the BBPD. The current mismatch calibration results in the reference spur reduction of the CMOS frequency synthesizer up to 6.7 dB.

II. Circuit Description

Fig. 1 shows the proposed synthesizer. It is composed of a conventional integer-N PLL with a 5-bit digital-controlled CP, an automatic frequency control (AFC) block, and additional CP current mismatch calibration circuits. The additional calibration circuits include a lock detector (LD), a HRPD, and a 5-bit successive approximation register-controlled (SAR) controller.

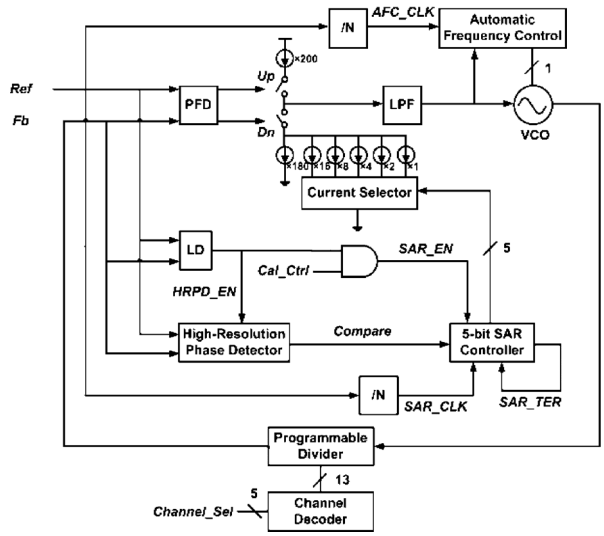

Fig. 1. Proposed frequency synthesizer.

A. CP Current Mismatch Calibration

The flowchart for CP current mismatch calibration is shown in Fig. 2. Initially, the HRPD and all control bits of the SAR controller are reset when the PLL is out of lock. The pump current and dump current of the CP are 200 μA and 180 μA, respectively. When the synthesizer is locked, LD will trigger the calibration process. Since the CP current mismatch will result in a static phase error between the *Ref* and *Fb* signals, shown in Fig. 1, the BBPD in the HRPD is used to detect the error. The output of the BBPD is sent to the SAR controller to determine the five control bits of the CP, which enable the dump current to match the pump current. The minimum detectable phase error for a typical 0.18 μm CMOS BBPD is difficult to achieve less than 45 ps, so the HRPD is developed to enhance the calibration accuracy.

B. High-Resolution Phase Detector

The high-resolution phase detector consists of a duty cycle equalizer, a high-gain time difference amplifier (TDA), and a BBPD as shown in Fig. 3. The amplification factor of a TDA will be degraded if the duty cycles of its two input signals are different. A duty cycle equalizer preceding the TDA is added to solve this problem. The TDA used in this work includes a charge-transferring differential pair [2] and two comparators. Through cross-coupling of the two differential transistor pairs, the transfer characteristic of the transistor pair with the slower input signal is interfered and slowed by the other one. Therefore,

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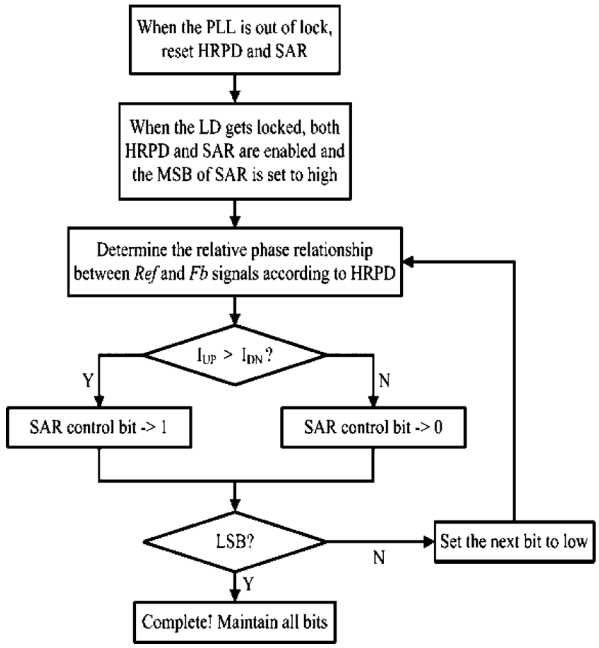


Fig. 2. Flowchart for CP current mismatch calibration.

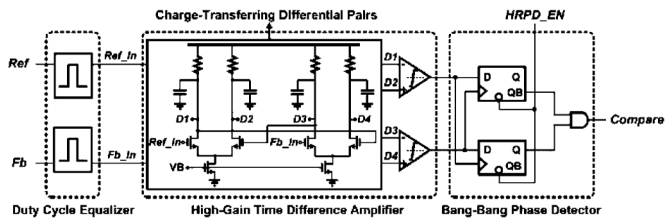


Fig. 3. High-resolution phase detector (HRPD).

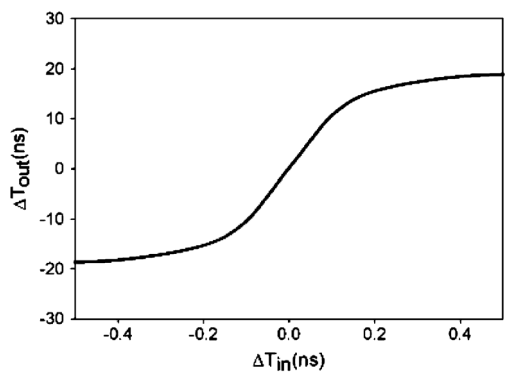


Fig. 4. Simulated transfer characteristics of the high-gain TDA. ΔT_{in} and ΔT_{out} are the input and output timing differences of the TDA, respectively.

the timing difference between the two input signals is extended. Fig. 4 shows the simulated transfer characteristics of the TDA. When the input timing difference is within 200 ps, the timing amplification factor is more than 75. Thanks to the TDA, the minimum detectable phase error of the HRPD can be reduced to 0.6 ps.

C. 5-Bit SAR Controller

The SAR controller in [3], which performs a binary-search algorithm, is revised as shown in Fig. 5. In the beginning, the LD sends SAR_EN signal to clear all the cells in the SAR controller. When the first clock arrives, the most significant bit (MSB), bit 4, is set to *high*. The MSB is maintained *high* or

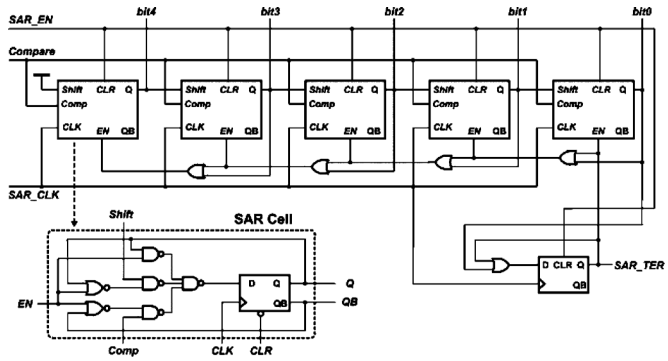


Fig. 5. 5-bit SAR controller.

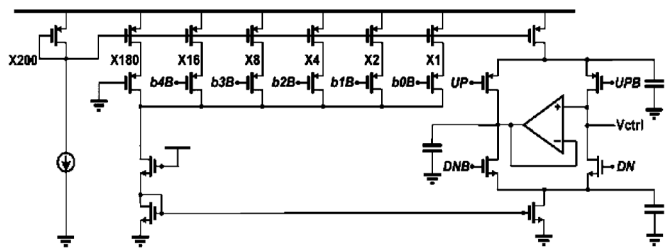


Fig. 6. 5-bit digital-controlled CP.

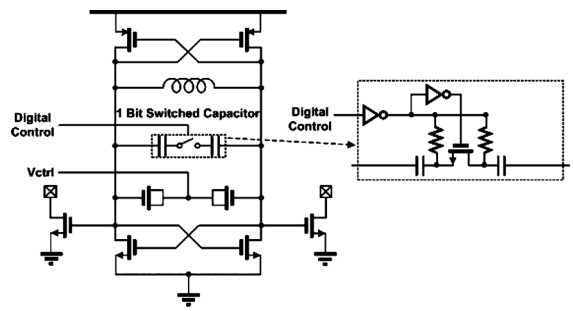


Fig. 7. Dual-band VCO.

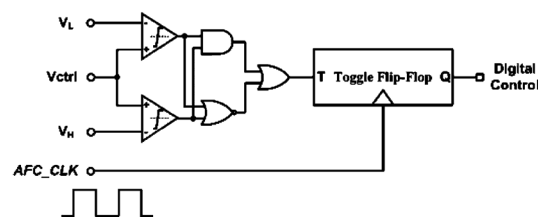


Fig. 8. Automatic frequency control circuit.

changed to *low* depending on the comparison result, *Compare*, from the HRPD at the next clock. If *Compare* is *high*, the MSB is maintained *high*. On the other hand, the MSB is changed to *low* if *Compare* is *low*. The process will repeat until the least significant bit (LSB), bit 0, is determined. Then the SAR controller generates the signal, SAR_TER, to indicate that the calibration is completed.

D. 5-Bit Digital-Controlled CP

Fig. 6 shows the 5-bit digital-controlled CP. The pump current has a nominal value of 200 μA, and the dump current is digitally controlled and it can cover from 180 to 211 μA. The minimum current step is chosen as 1 μA to achieve the worst case current mismatch of 0.5% in the CP. The control bits of the CP are changed only during the calibration process and they are fixed after the calibration is completed. The synthesizer may

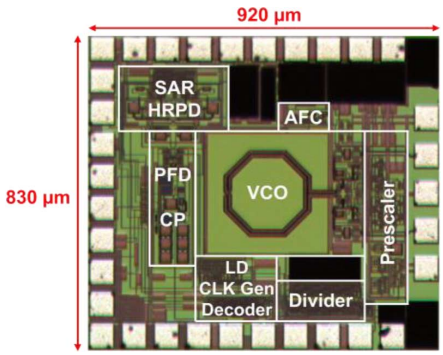
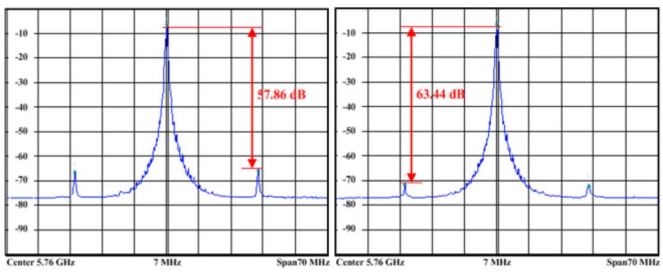


Fig. 9. Die photograph.



(a) (b)

Fig. 10. Measured frequency synthesizer spectrum: (a) without calibration and (b) with calibration.

TABLE I
CMOS FREQUENCY SYNTHESIZERS FOR 5 GHZ U-NII BAND

Ref.	[6]	[7]	[8]	This work
CMOS Process	0.25 μm	0.24 μm	0.18 μm	0.18 μm
Freq. (GHz)	4.12 - 4.72	4.84 - 4.99	4.8	5.18 - 5.32 5.74 - 5.82
f_{Ref} (MHz)	4	11	1	20
BW (kHz)	90	280	N/A	280
Phase Noise (dBc/Hz)	N/A	-101 @ 1MHz	-104 @ 1MHz	-102 @ 1MHz
Spur (dBc)	- 45	- 45	- 55	< - 63
AFC	None	None	None	Yes
Supply (V)	2.5	1.5 / 2	1.8	1.8
Power (mW)	117.5	25	18	28.8
FOM (dB)	72.0	73.1	N/A	85.9

$$\text{FOM(dB)} = 20\log\left[\frac{\text{Bandwidth (kHz)}}{f_{\text{Ref}}\text{(MHz)}}\right] - \text{Spur (dBc)}$$

need to initiate locking process if its characteristic is varied due to the change of temperature or supply voltage. The calibration will be automatically invoked when the synthesizer is locked again.

E. VCO, Divider, and AFC

Fig. 7 shows the schematic diagram of the dual-band VCO, which utilizes 1-bit control to switch the capacitors. The VCO frequency covers the low (5.15–5.25 GHz), middle (5.25–5.35 GHz), and upper (5.725–5.825 GHz) U-NII bands. The CMOS cross-coupled transistor pair is used to provide larger negative transconductance than the PMOS or NMOS cross-coupled pair [4]. The programmable divider consists of a high-speed divide-by-16/17 dual modulus prescaler followed by a pulse-swallow divider. A true single-phase-clocked (TSPC) divider cell [5] is used in the prescaler. According to the input $Channel\_Sel$ code, the division ratio of the divider chain can be reconfigured. With a reference clock, f_{Ref} of 20 MHz, this integer-N frequency synthesizer generates the output frequency from 5.18 to 5.32 GHz and from 5.74 to 5.82 GHz with a step of 20 MHz. The AFC circuit is shown in Fig. 8. When the control voltage of the VCO is higher than 1.4 V, it means that the oscillation frequency is lower than the desired frequency and it will trigger a band switching to the high operation band. On the contrary, when the control voltage is lower than 0.4 V, it will trigger a band switching to the low operation band.

III. MEASUREMENT RESULT

This chip was fabricated in TSMC 0.18 μm CMOS 1P6M technology. A die photograph is shown in Fig. 9. The overall chip size is 0.92 mm $\times$ 0.83 mm. The measured frequency ranges of the VCO are from 4.99 to 5.50 GHz for low band and from 5.45 to 6.09 GHz for high band. The synthesized frequencies for low band and high band are from 5.18 to 5.32 GHz and from 5.74 to 5.82 GHz, respectively. Fig. 10 shows the measured output spectrum of the synthesizer with and without current mismatch calibration. The reference spur is -63.4 dBc when the calibration is enabled and the improvement resulting from the calibration is 5.58 dB. The measured phase noise of the synthesizer is -102.1 dBc/Hz at 1 MHz offset. Table I summarizes the performance of the CMOS frequency synthesizers [6]–[8] for the 5 GHz U-NII band. This work features dual-band operation with low spur level and achieve an excellent figure of merit (FOM).

IV. CONCLUSION

A CMOS frequency synthesizer covering the U-NII bands of 5.18–5.32 GHz and 5.74–5.82 GHz is presented. The high-resolution phase detector is proposed to enhance the calibration accuracy of charge-pump current mismatch. The measured reference spur of the synthesizer is improved by 5.6 dB with the calibration and is lower than -63 dBc.

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