Least-Squares Equalizer Demonstrations Using a Full-Digital Bandwidth Sub-Nyquist-Sampled Wideband Beamformer on an RFSoC

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The radio frequency system-on-a-chip (RFSoC) has recently become a viable candidate for completely replacing traditional analog and digital front ends, facilitating the development of wideband phased-array systems where the modern-day RFSoC takes the comprehensive, dominate role in the architecture of the array. Wideband phased-array systems require high-fidelity compensation techniques capable of correcting imbalanced and dispersive channel effects for effective beamforming. This article provides solutions to these challenges by designing a wideband equalizer for a sub-Nyquist-sampled 1.6-GHz *S*-band phased-array system implemented on a Xilinx 8-channel RFSoC, whose analog-to-digital converters (ADC) operate at 4 gigasamples per second. In brief, an RFSoC is a unique, state-of-the-art, highly integrated device that incorporates a field programmable gate array, high-speed ADCs and digital-to-analog converters with a system-on-a-chip architecture on a single monolithic device. By definition, true time delay beamsteering can be implemented digitally via a combination of integer-sample delays and fractional-sample delay finite impulse response filters. By modifying the filter structure of the fractional-sample delay filter bank to support complex coefficients, channel equalization is integrated with fractional-sample delay filters to mitigate undesired channel effects. For the first time, to the best of our knowledge, this article has developed an equalizer design methodology for an uncalibrated 8-element RFSoC-based sub-Nyquist-sampled wideband beamformer. Lab measurements confirm efficacy.

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I. INTRODUCTION

Only recently have radio frequency system-on-a-chip (RFSoCs) been viable candidates for completely replacing traditional analog and digital front ends [1]–[6]. As such, this article describes a completely new approach for wideband phased-array systems where the modern-day RFSoC takes the comprehensive, dominate role in the architecture of the array. However, because accurate array performance relies on matched channel behavior [7], substantial interchannel magnitude and phase errors present in most practical phased-array systems often preclude uncalibrated operation. Frequency-varying amplitude and dispersive phase behavior [8], which varies between channels, inhibits the coherent summation of element signals degrading performance characteristics such as main beam and null steering accuracy and null depths. This is of particular concern in adaptive beamforming applications, which seek to place deep, spatially accurate nulls based on current element signal samples [9].

Given that many narrowband systems implement channel compensation via attenuators and phase shifters [10], simple adjustments to channel control signals are commonly sufficient to mitigate interchannel imbalances for such applications. This assumes that channel variations are sufficiently steady over the narrow instantaneous bandwidth to be corrected by a constant shift in attenuator and phase commands, effectively a single-tap complex-coefficient finite impulse response (FIR) filter. As instantaneous bandwidth is often configurable within a larger system bandwidth, a series of frequency-dependent compensation values may be required, commonly stored in a lookup table (LUT). A system bandwidth may be partitioned into several frequency bins such that compensation values can be represented by zeroth- or first-order approximations, reducing calibration table memory requirements. In contrast, wideband applications require higher fidelity compensation over the band of interest. As channel responses for most practical systems have appreciable frequency dependence, zeroth- or first-order approximations fail to accurately represent channel characteristics. FIR filters have been shown to effectively compensate over a prescribed bandwidth and can be implemented at the element level in fully digital architectures [11].

To provide some background, Johnson *et al.* [12] demonstrated an equalization approach for both deterministic and adaptive applications. They provided adaptive nulling demonstrations with instantaneous bandwidths of 1 MHz, a considerable achievement given the technology available at the publication of this seminal work. The deterministic approach is leveraged in [9] to determine the impact of equalization on adaptive digital beamforming for

a 4-element array. Channel data consist of a 124 MHz chirp represented at a sample rate of 125 MHz. Our past work [13] used measured channel data in the frequency domain to synthesize channel equalizers for a bandwidth of about 500 MHz sampled at 1.5 GHz. In [14], wideband calibration is implemented using the time reversal technique and demonstrated [8] using a 16-element array with 500 MHz of instantaneous bandwidth sampled at 1.333 GHz. Antenna patterns at various discrete frequencies are provided at multiple steering angles. In this article, we expand on these techniques by leveraging the equalizer group delay to construct a fractional-sample delay filter bank at a substantially wider bandwidth on a fully digital system.

There are several papers that describe the implementation of digital equalization on a field programmable gate array (FPGA) for radar applications, and several prominent ones are [15]–[20]. Recently, with the expanded memory capabilities of modern FPGAs, element-level true time delay (TTD) wideband beamforming is evolving from its infancy. There are several papers that implement TTD on an FPGA, which include [21]–[23]. The most famous is the paper by Cheung *et al.* [21] that was published in 2013. Currently, no published research exists that combines both equalization and TTD—except a paper written by Yao *et al.* [24] in 2015 and a paper written by our teammates described by Thompson *et al.* [25] in 2016. Both were in a simulated environment, i.e., vis-à-vis MATLAB. Moreover, the paper by Yao *et al.* was for a narrowband system, where TTD was not actually necessary.

In 2017, Xilinx announced the RFSoC product line, which incorporates a high-performance FPGA together with several gigasample per second (GSPS) data converters and a system-on-a-chip (SoC) architecture into the same integrated circuit package. As pointed out by Franco *et al.* [26], a classic approach for communicating with external converters exploits the JESD204 interface [27], [28]. By integrating the converters inside the SoC, it is possible to avoid this interface, improving power consumption and reducing the component footprint. For instance, Vivekanandan, *et al.* [29] reported a footprint reduction of 50% and power reduction of 75% while Fagan, *et al.* [30] showed a 6× power improvement when adopting the RFSoC over traditional FPGA and analog-to-digital converter (ADC) typologies. The improvement in power consumption and footprint from combining the data converters with an FPGA and SoC enables higher operating frequencies for phased-array systems due to a smaller achievable lattice, previously precluded by the prohibitively high thermal and component densities of the distributed architecture.

In brief, these compact devices were geared toward the next-generation telecommunication industry, such as 5G and 6G, yet they provide an ideal technology platform for the future of phased-array radar for three reasons: 1) sample synchronization across multiple channels is readily possible, 2) low power consumption, and 3) compact form factor. The latter is especially evident, as traditional analog up/down conversion circuits are not needed for radar systems in the *S*-band owing to the multigigasample RF data converters, which enable direct sampling of incident waveforms. Other researchers have been exploring RFSoC technology for next-generation radar applications, and recent breakthroughs include bistatic radar [31], phased-array cost reduction [30], data reduction for digital apertures [5], near-field calibration [2], real-time signal generation [32], or fully digital radar system development [6].

For the first time, to the best of our knowledge, this article has developed an equalizer design methodology for an uncalibrated 8-element RFSoC-based sub-Nyquist-sampled wideband beamformer. This allows the digital domain to be substantially closer to the phased-array aperture. In this article, ADC channels operate at 4 GSPS on 1.6 GHz of bandwidth captured using a wideband Vivaldi array. The aperture is centered at 3 GHz and supports better than 2 GHz of bandwidth. The instantaneous bandwidth of 1.6 GHz represents the full digital bandwidth due to the 80% Nyquist bandwidth of the decimation and interpolation filters in the RFSoC digital downconverter and digital upconverter. The beamformer output is provided through a digital-to-analog converter (DAC) for chamber measurement. At the center of the testbed is the Pentek Quartz Model 5950, a 3U OpenVPX carrier card that integrates a Xilinx Zynq UltraScale+ RFSoC, providing MMCX RF interfaces to the eight ADCs and eight DACs. Pentek factory software and firmware provide the necessary functionality for waveform generation and RF data capture and a solid base on which to design and implement the digital equalizer and beamformer.

The rest of this article is organized as follows. The relevant background, including channel characterization, equalizer synthesis techniques, equalizer performance assessments, and fractional-sample delay filter bank implementation, is presented in Section II. An overview of the wideband equalizer and beamformer testbed is provided in Section III, discussing equalizer design decisions and implementation of a wideband configurable complex-coefficient FIR filter bank. Section IV provides simulation results and far-field anechoic chamber measurements for various steering directions and system configurations. Finally, Section V concludes this article. An Appendix is also included at the end of the article, which provides channel characterization data and equalizer results.

II. PROBLEM FORMULATION AND DESIGN APPROACH

This section discusses the theory behind the equalizer synthesis techniques explored herein and the design approach for the wideband beamformer demonstrated in Section IV. Wideband equalization and beamforming are implemented via configurable complex-coefficient FIR filters synthesized using measured channel characterization data, assuming a linear system response. Extensive work in nonlinear equalization [33], [34] and digital predistortion [35], [36] explores techniques for addressing nonlinear system responses. Implementing wideband beamsteering

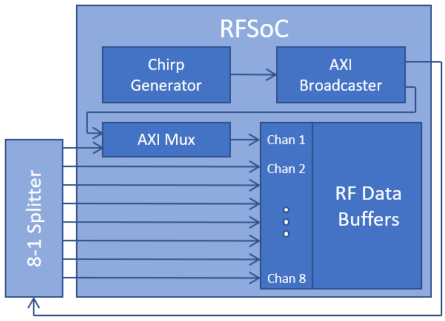

Fig. 1. RFSoC channel characterization block diagram. External loopback provides the reference waveform to all eight channels simultaneously, internal loopback allows for capture of the reference waveform.

in the digital domain simplifies the calibration landscape significantly as the dispersive effects of the unnecessary analog components (amplifiers, up/downconverters, phase shifters/time delay units (TDUs)) are no longer present. However, obtaining timing closure with the limited FPGA resources while achieving real-time throughput of the full digital bandwidth is not without its challenges.

Section II-A discusses the capture of channel characterization data. Filter synthesis techniques are presented in Section II-B, which include FIR filter synthesis from an arbitrary frequency response and fractional-sample delay filter bank synthesis to support TTD beamsteering [37]. Section II-C discusses equalizer performance metrics used to quantify equalizer performance sensitivity to group delay and filter length.

A. Characterization Data Capture

High accuracy in channel characterization is paramount for effective equalizer implementation. Characterization can be accomplished either in the frequency domain [14] or the time domain [9], [13]. The channel response to a series of continuous wave tones uniformly distributed across the system bandwidth provides a frequency domain estimate of the channel characteristics. Alternatively, if time domain channel data can be captured directly, the response to a reference waveform can serve to characterize channel behavior. This requires the selection and generation of a reference waveform with which to excite the channel under test. Although several waveforms have been utilized for channel characterization, which may be dependent on the specific system application, the intent is that all frequencies within the band of interest are uniformly excited [9]. Pentek factory firmware support for waveform capture and generation was integral to channel characterization efforts. Fig. 1 shows a block diagram describing the relevant firmware components for channel characterization. We modified factory firmware with the addition of the two AXI4-Stream components shown in Fig. 1, which enable internal digital loopback of the reference waveform. The channel 1 DAC serves as the external reference source, looped back through an 8-to-1 splitter to the eight ADCs. RF data were captured concurrently for all channels, recording several chirp pulses for characterization. A linear frequency modulated chirp waveform spanning 90% of the Nyquist zone served as the reference waveform in this application. We configured the chirp generator within the Pentek RFSoC firmware to output a 1.8-GHz chirp at 4 GSPS centered in the second Nyquist zone. This provided adequate spectral coverage of the 1.6-GHz bandwidth received from the 3 GHz centered array during system operation.

In the following sections, measured characterization data are represented as M-length column vectors containing the time domain samples. The reference waveform internal loopback is represented by the column vector $\mathbf{y} = [y_0, y_1, \ldots, y_{\mathrm{M}-1}]^{\mathrm{T}}$. The channel response data are stored in a series of column vectors $\mathbf{x}_{\mathrm{c}} = [x_0, x_1, \ldots, x_{\mathrm{M}-1}]^{\mathrm{T}}$ where subscript c denotes the channel number. A Hann window is applied to the initial and final 2.5% of each data vector.

B. Channel Equalizer Filter Synthesis

This section outlines two methods for synthesizing filter coefficients for a channel equalizer using measured reference waveform and channel characterization data. Frequency domain synthesis is discussed in Section II-B1 and time domain synthesis is discussed in Section II-B2. Both techniques utilize a least-squares approach to minimize the mean squared error between the equalizer output and the reference waveform. Section II-B3 discusses the importance of appropriately delaying the reference waveform prior to filter synthesis. By accounting for the group delay associated with the equalizer filter, the reference waveform can be time-aligned with the equalizer output, drastically improving performance. Section II-C discusses a few metrics for quantifying equalizer performance.

1) *Frequency Domain Synthesis:* This approach seeks to synthesize a channel equalizer filter using a given frequency response [13]. A filter whose frequency response most closely approximates the desired response $\mathbf{H}_{\mathrm{des}}$ is determined using filter synthesis of an arbitrary frequency response [38]. This desired response is that which compensates the frequency response of a given channel to match that of the reference waveform, as given by $\mathbf{H}_{\mathrm{des}} = \frac{\mathbf{H}_{\mathrm{y}}}{\mathbf{H}_{\mathrm{x}}}$ where the variables $\mathbf{H}_{\mathrm{y}}$ and $\mathbf{H}_{\mathrm{x}}$ are the frequency responses for the reference waveform and given channel, respectively.

As part of equalizer design for the RFSoC, we revisit seminal design techniques for digital filters and explain our design choices. Filter synthesis of the arbitrary frequency response $\mathbf{H}_{\mathrm{des}}$ is achievable using the inverse discrete Fourier transform, which is defined as

$$h_n \triangleq \frac{1}{N}\sum_{k=0}^{N-1} H_k e^{i\frac{2\pi}{N}kn},\ n \in [0, N-1]. \tag{1}$$

This can be rewritten in matrix form, as given by $\mathbf{h} = \mathbf{C}^{-1}\mathbf{H}$, where $\mathbf{H}$ is an N-length column vector of frequency domain H_k values, $\mathbf{h}$ is an N-length column vector of time domain h_n values, and $\mathbf{C}$ is an $N \times N$ Fourier transform kernel matrix whose elements are given by $e^{-i\frac{2\pi}{N}kn}$. The indices k and n index the rows and columns of $\mathbf{C}$, respectively.

This approach is inefficient as the resulting filter length is equivalent to the number of specified frequency points. Hence, either the frequency response will have poor resolution or the FIR filter will be prohibitively long. One can approximate the desired frequency response by reducing the filter length to L yielding the overdetermined system given by

$$\mathbf{H} \approx \mathbf{C}_{\mathrm{o}}\mathbf{h}_{\mathrm{o}} \tag{2}$$

where $\mathbf{h}_{\mathrm{o}}$ is an L-length column vector of time domain h_n values and $\mathbf{C}_{\mathrm{o}}$ is an $N \times L$ kernel matrix consisting of the first L columns of $\mathbf{C}$

Equation (2) can be approximately solved using the method of ordinary least squares, which has a closed-form solution given by

$$\mathbf{h}_{\mathrm{o}} = \left(\mathbf{C}_{\mathrm{o}}^{H}\mathbf{C}_{\mathrm{o}}\right)^{-1}\mathbf{C}_{\mathrm{o}}^{H}\mathbf{H}. \tag{3}$$

The notation $\{\cdot\}^H$ indicates the Hermitian, or conjugate, transpose and the term $(\mathbf{C}_{\mathrm{o}}^{H}\mathbf{C}_{\mathrm{o}})^{-1}\mathbf{C}_{\mathrm{o}}^{H}$ is known as the Moore–Penrose pseudoinverse [39] of the matrix $\mathbf{C}_{\mathrm{o}}$. One can apply an N-length frequency-dependent weighting function in the form of a diagonal matrix $\mathbf{W}$ to prioritize particular subbands within the spectrum, as given by

$$\mathbf{h}_{\mathrm{o}} = \left(\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{C}_{\mathrm{o}}\right)^{-1}\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{H}. \tag{4}$$

Substituting the desired frequency response $\mathbf{H}_{\mathrm{des}}$ for the arbitrary response $\mathbf{H}$ yields the filter coefficients $\mathbf{h}_{\mathrm{eq}} = \mathbf{h}_{\mathrm{o}}$. Thus, frequency domain equalizer synthesis is given by

$$\mathbf{h}_{\mathrm{eq}} = \left(\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{C}_{\mathrm{o}}\right)^{-1}\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{H}_{\mathrm{des}}. \tag{5}$$

2) *Time Domain Synthesis:* Equalizer filter coefficients can also be synthesized directly using time domain samples. Here, we delve further into a procedure outlined in [12], applying key features of it to our RFSoC-based wideband beamformer. In brief, this procedure utilizes the least-squares approach to identify a weight vector, which closely converts time domain samples of the channel characterization data to those of the reference waveform, as given by

$$\mathbf{y}_{\mathrm{des}} \approx \mathbf{X}\mathbf{w}_{\mathrm{eq}}. \tag{6}$$

The column vector $\mathbf{y}_{\mathrm{des}}$ is of length $N = (M + L - 1)$ where M is the number of time domain samples in the reference waveform/channel characterization data and L is the equalizer filter length. It contains time domain samples of the reference waveform $\mathbf{y}$ zero-padded by $L - 1$ such that

$$\mathbf{y}_{\mathrm{des}} = \left[y_0, y_1, \ldots, y_{M-1}, 0, \ldots, 0\right]^{\mathrm{T}}. \tag{7}$$

The column vector $\mathbf{w}_{\mathrm{eq}}$ is of length L and contains the equalizer filter coefficients $\mathbf{h}_{\mathrm{eq}}$ in reverse order such that $w_l = h_{(L-1)-l}$ where $l = 0, 1, \ldots, L-1$.

Equation (6) implements a convolution between the channel characterization data $\mathbf{x} = [x_0, x_1, \ldots, x_{\mathrm{M}-1}]^{\mathrm{T}}$ and the unknown weight vector $\mathbf{w}_{\mathrm{eq}} = \left[h_{L-1}, h_{L-2}, \ldots, h_0\right]^{\mathrm{T}}$. Thus, the matrix $\mathbf{X}$ is of size $N \times L$ and contains time domain samples of the characterization data for the given channel such that each row consists of L sequential samples. To implement the full convolution, $\mathbf{x}_{\mathrm{ch}}$ is zero-padded with $L - 1$ zeros at the beginning and end of the array, as given by

$$\mathbf{X} = \begin{bmatrix} 0 & 0 & \cdots & 0 & x_0 \\ 0 & 0 & \cdots & x_0 & x_1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & x_{L-4} & x_{L-3} \\ 0 & x_0 & \cdots & x_{L-3} & x_{L-2} \\ x_0 & x_1 & \cdots & x_{L-2} & x_{L-1} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ x_{M-L} & x_{M-L+1} & \cdots & x_{M-2} & x_{M-1} \\ x_{M-L+1} & x_{M-L+2} & \cdots & x_{M-1} & 0 \\ x_{M-L+2} & x_{M-L+3} & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ x_{M-2} & x_{M-1} & \cdots & 0 & 0 \\ x_{M-1} & 0 & \cdots & 0 & 0 \end{bmatrix}. \tag{8}$$

As (6) is of the same form as (2), the solution to the ordinary least-squares method, given in (3), is used to determine $\mathbf{w}_{\mathrm{eq}}$, namely

$$\mathbf{w}_{\mathrm{eq}} = \left(\mathbf{X}^{H}\mathbf{X}\right)^{-1}\mathbf{X}^{H}\mathbf{y}_{\mathrm{des}}. \tag{9}$$

3) *Prescribed Group Delay:* Time alignment between the reference waveform and equalizer output, briefly discussed in [12], is of particular importance in equalizer design, as ignoring the filter's group delay degrades performance considerably. Applying the appropriate delay to the reference waveform ensures that filter synthesis seeks a filter with a practical group delay. We refer to this reference waveform delay as the equalizer's *prescribed group delay* Δm_{g}, specified in samples and not necessarily an integer. Performance metrics discussed in Section II-C are used to examine the dependence of equalizer performance on prescribed group delay, providing an opportunity for optimization.

To explore the prescribed group delay, we define a new variable $\mathbf{H}_{\mathrm{des,d}} = \frac{\mathbf{H}_{\mathrm{y,d}}}{\mathbf{H}_{\mathrm{x}}}$ where $\mathbf{H}_{\mathrm{y,d}}$ is the frequency domain response of the reference waveform delayed by Δm_{g} samples. Substituting this desired response into (5) yields the corresponding equalizer $\mathbf{h}_{\mathrm{eq,d}}$. Similarly, a delayed time domain reference waveform vector $\mathbf{y}_{\mathrm{des,d}}$ is substituted into (9) to determine the corresponding weight vector $\mathbf{w}_{\mathrm{eq,d}}$.

The governing equations for frequency and time domain equalizer synthesis, given in (5) and (9), can be expanded for simultaneous processing of several delays. We define a prescribed group delay range of $\Delta m_{\mathrm{g}} \in [0, L]$ samples specified with some fractional-sample step size $\delta_{m_{\mathrm{g}}}$ such that there are $D = \frac{L}{\delta_{m_{\mathrm{g}}}} + 1$ steps. The reference waveform vectors associated with each delay are concatenated to form a reference waveform matrix, as given by

$$\mathbf{H}_{\mathrm{des},\Delta} \triangleq \left[\mathbf{H}_{\mathrm{des},0}\ \mathbf{H}_{\mathrm{des},1}\ \cdots\ \mathbf{H}_{\mathrm{des,D}}\right] \tag{10}$$

for frequency domain synthesis and

$$\mathbf{Y}_{\mathrm{des},\Delta} \triangleq \left[\mathbf{y}_{\mathrm{des},0}\ \mathbf{y}_{\mathrm{des},1}\ \cdots\ \mathbf{y}_{\mathrm{des,D}}\right] \tag{11}$$

for time domain synthesis. Substituting (10) and (11) into (5) and (9), respectively, yields

$$\mathbf{h}_{\mathrm{eq},\Delta} = \left(\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{C}_{\mathrm{o}}\right)^{-1}\mathbf{C}_{\mathrm{o}}^{H}\mathbf{W}\mathbf{H}_{\mathrm{des},\Delta} \tag{12}$$

and

$$\mathbf{W}_{\mathrm{eq},\Delta} = \left(\mathbf{X}^{H}\mathbf{X}\right)^{-1}\mathbf{X}^{H}\mathbf{Y}_{\mathrm{des},\Delta}. \tag{13}$$

The columns of $\mathbf{h}_{\mathrm{eq},\Delta}$ and $\mathbf{W}_{\mathrm{eq},\Delta}$ contain the sets of filter coefficients corresponding to each prescribed group delay. Recall that columns of $\mathbf{W}_{\mathrm{eq},\Delta}$ contain the equalizer coefficients in reverse order.

As described in [40], wideband beamforming is achieved through the use of TTD beamsteering, which can be digitally implemented through a combination of integer-sample delays and fractional-sample delays [13]. Thus, we desire a channel-specific fractional-sample delay filter bank that compensates the particular channel frequency response. By adjusting the prescribed group delay, the fractional-sample delay can be synthesized directly into the equalizer. To synthesize the calibrated fractional-sample delay filter bank, we select a block of prescribed group delays spanning an integer sample at the appropriate fractional-sample resolution.

C. Equalizer Performance

A numerical metric for equalizer performance provides an efficient method for selecting from various equalizer options, whether they be from different synthesis techniques or different prescribed group delays. This section discusses two methods for quantifying equalizer performance, the channel pair cancellation ratio (CPCR) [41] and the residual tracking error [12].

1) *Channel Pair Cancellation Ratio:* The CPCR is defined as the ratio of equalizer output power to residual power, as given by

$$\mathrm{CPCR} \triangleq \frac{P_{\mathbf{x}_{\mathrm{out}}}}{P_{\mathbf{x}_{\mathrm{res}}}}. \tag{14}$$

The output signal vector $\mathbf{x}_{\mathrm{out}}$ is the result of filtering the channel characterization data with the synthesized equalizer. The residual signal vector $\mathbf{x}_{\mathrm{res}}$ is defined as the difference between the desired signal vector and output signal vector. Low residual power indicates better agreement between the output signal vector and the reference signal vector resulting in a higher CPCR.

2) *Residual Tracking Error:* Alternatively, the residual tracking error can be used as an indicator of equalizer performance. We redefine the overdetermined systems given in (2) and (6) in terms of residual error matrices $\mathbf{E}$ and update them to incorporate the reference waveform matrices given in (10) and (11) such that

$$\mathbf{E}_{\mathrm{freq}} = \mathbf{W}^{1/2}\mathbf{H}_{\mathrm{des},\Delta} - \mathbf{W}^{1/2}\mathbf{C}_{\mathrm{o}}\mathbf{h}_{\mathrm{eq},\Delta} \tag{15}$$

and

$$\mathbf{E}_{\mathrm{time}} = \mathbf{Y}_{\mathrm{des},\Delta} - \mathbf{X}\mathbf{W}_{\mathrm{eq},\Delta}. \tag{16}$$

Equation (15) assumes that the diagonal weighting matrix $\mathbf{W}$ is incorporated into (2), as given by $\mathbf{W}^{1/2}\mathbf{H} \approx \mathbf{W}^{1/2}\mathbf{C}_{\mathrm{o}}\mathbf{h}_{\mathrm{o}}$. If the equalizer coefficients have already been determined, the residual tracking error for the dth delay is given by the squared magnitude of the diagonal elements of the given error matrix, namely $|E_{dd}|^2$.

Alternatively, QR decomposition, which can be used to efficiently compute the least-squares solution in real-time embedded systems, provides the residual tracking errors prior to computing equalizer coefficients [42]. Define, for a given system of equations $\mathbf{E} = \mathbf{Y} - \mathbf{X}\mathbf{W}$, the extended matrix $\mathbf{Z} = [\,\mathbf{X}\;\mathbf{Y}\,] = \mathbf{Q}\mathbf{R}$. QR decomposition decomposes $\mathbf{Z}$ into a unitary matrix $\mathbf{Q}$ and an upper triangle matrix $\mathbf{R}$ such that

$$\mathbf{Z}^{H}\mathbf{Z} = \begin{bmatrix} \mathbf{X}^{H}\mathbf{X} & \mathbf{X}^{H}\mathbf{Y} \\ \mathbf{Y}^{H}\mathbf{X} & \mathbf{Y}^{H}\mathbf{Y} \end{bmatrix} = \mathbf{R}^{H}\mathbf{R}. \tag{17}$$

Several methods exist for computing the QR decomposition, such as the Householder transformations [43], the Gram–Schmidt process [44], or Givens rotations [45], which are useful for implementing QR decomposition in an embedded system. The matrix $\mathbf{R}$ can be partitioned as described by

$$\mathbf{R} = \begin{bmatrix} \mathbf{U} & \mathbf{V} \\ \mathbf{0} & \mathbf{T} \end{bmatrix}. \tag{18}$$

Given that $\mathbf{R}$ is an upper triangle matrix, the matrices $\mathbf{U}$ and $\mathbf{T}$ are also both upper triangle. Thus, computing the matrix inverse $\mathbf{U}^{-1}$, necessary to determine the least-squares solution given by $\mathbf{W} = \mathbf{U}^{-1}\mathbf{V}$, is of considerably lower complexity. We seek the equalizer associated with smallest residual tracking error, which can be determined prior to solving for the equalizer coefficients using the matrix $\mathbf{T}$. The residual tracking error is given for the dth delay by

$$|E_{dd}|^2 = \sum_{c=1}^{d} |T_{cd}|^2. \tag{19}$$

III. RESEARCH TESTBED

Fig. 2 shows a block diagram of our wideband beamformer. Mixed-signal processing is accomplished on Pentek hardware that houses a Xilinx RFSoC and interfaces with a wideband Vivaldi antenna array. Received signals are sampled in the second Nyquist zone by ADCs at 4 GSPS and digitally downconverted to complex baseband where they are decimated by a factor of 2, processed, and combined. The combined signal is interpolated by a factor of 2, digitally upconverted, and sourced by the DAC at 4 GSPS to be measured in the anechoic chamber. As is common for smaller arrays, we terminated the two edge elements with matched loads to mitigate edge effects. As such, the center six aperture elements interface to the RFSoC ADCs. Fig. 3 shows our testbed mounted in the University of Oklahoma's far-field anechoic chamber.

A. Channel Characterization

As mentioned in Section II-A, the first step in equalizer design is channel characterization. Measured characterization data for channels 1–6, shown in Fig. 4, consist of $M = 2000$ complex-valued time domain samples captured

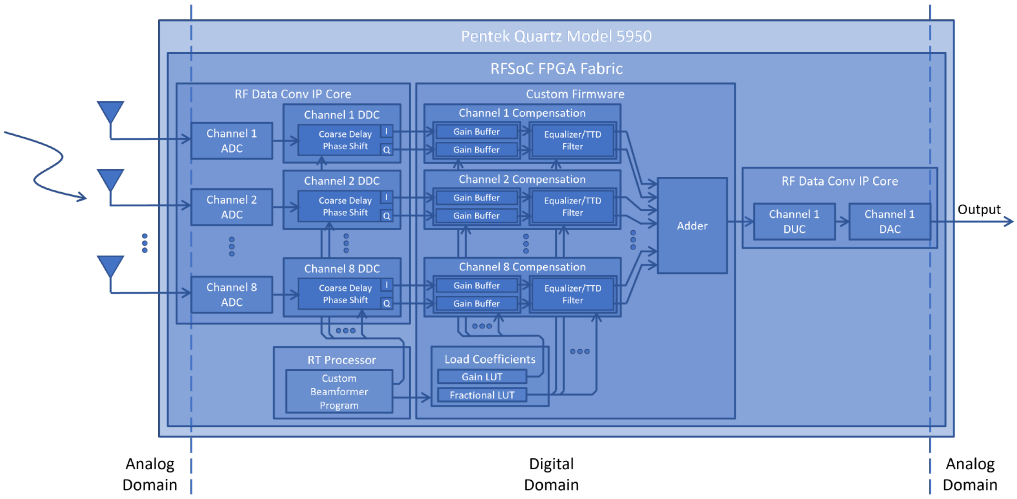

Fig. 2. Wideband beamformer functional diagram.

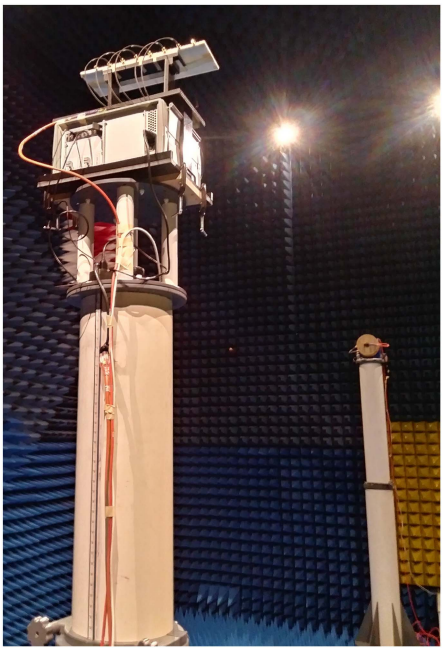

Fig. 3. Research testbed mounted in our far-field anechoic chamber.

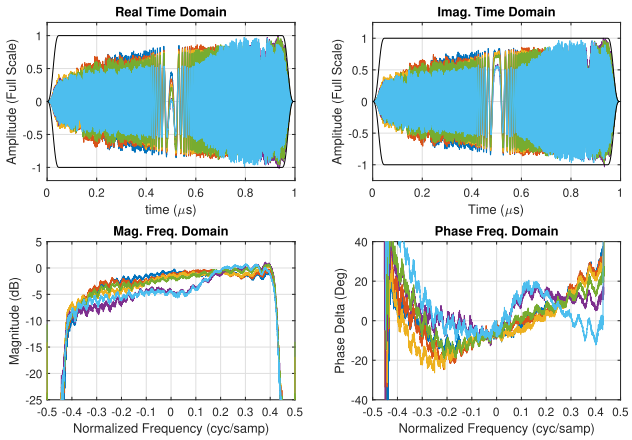

Fig. 4. Channel 1–6 characterization data. Top left: real time domain. Top right: imaginary time domain. Bottom left: frequency domain magnitude. Bottom right: frequency domain phase.

at 2 GSPS. The top row shows real and imaginary time domain data on the left and right, respectively. The black traces show the Hann window function, applied to the first and last 2.5% of the time domain data prior to processing.

Frequency domain data are shown in the bottom row, with magnitude and phase on the left and right, respectively. This was generated with an $N = 4096$-point fast Fourier transform of the time domain data. To emphasize the dispersive channel effects, phase data are presented as relative to the reference waveform. Specifically, traces show the difference between the unwrapped phase of the channel response and that of the reference waveform. Phase offsets are adjusted such that traces cross 0° at $f = 0 \frac{\text{cyc}}{\text{samp}}$. Given that the reference waveform spans 90% of the Nyquist zone, phase behavior outside the reference bandwidth of $-0.45 \leq f \leq 0.45$ is inconsequential given its low signal energy.

The appreciable frequency dependence in both magnitude and phase of each channel is readily apparent. Notably, dispersive effects can be seen in the phase plots necessitating higher fidelity compensation as compared to narrowband adjustments. Also apparent is a frequency-dependent ripple of about 1–2 dB and 10° due to mismatched interfaces of the commercial-off-the-shelf (COTS) hardware. As will be shown, equalizer fidelity is insufficient to correct for this ripple behavior, at least not as constrained by the RFSoC resources.

B. Channel Equalization

Channel characterization data shown in Fig. 4 were processed using both frequency and time domain filter synthesis techniques discussed in Section II. RFSoC FPGA resources used in this demonstration enabled timing closure

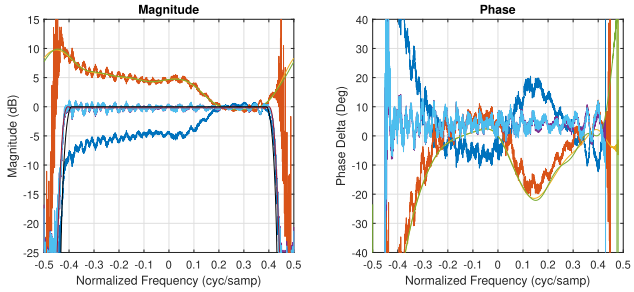

Fig. 5. Channel 6 equalizer magnitude (left) and unwrapped phase delta (right). Dark blue—channel characterization data. Red-orange: desired filter response. Yellow: filter response via frequency domain synthesis. Green: filter response via time domain synthesis. Purple: filter output via frequency domain synthesis. Cyan: filter output via time domain synthesis. Black: window function for frequency domain synthesis.

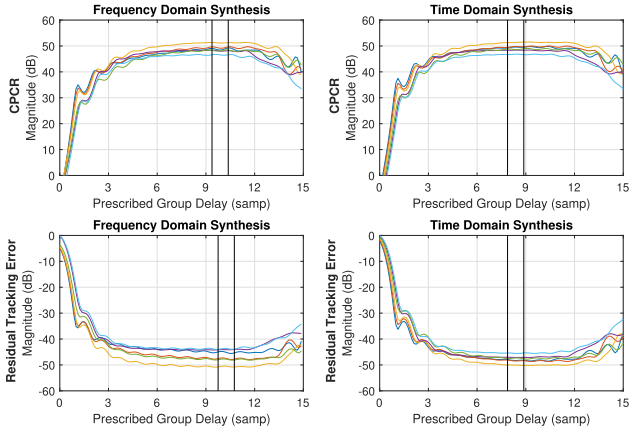

Fig. 6. Channel 1–6 equalizer performance. Top row—CPCR. Bottom row—residual tracking error. Left column—frequency domain synthesis. Right column—time domain synthesis.

for a full digital bandwidth, 15-tap complex-coefficient filter bank with $\frac{1}{8}$-sample step size. Resource utilization is discussed further in Section III-C. Equalizer frequency response data for channel 6 are provided in Fig. 5. In this figure, magnitude data are shown on the left and relative unwrapped phase data are provided on the right. Dark blue traces correspond to the channel 6 characterization data (cyan traces in Fig. 4), corresponding to $\mathbf{H}_{\mathrm{x}}$ in Section II-B1 and $\mathbf{X}$ in Section II-B2. The red-orange traces show the desired equalizer frequency response $\mathbf{H}_{\mathrm{des}}$. The yellow and green traces show the equalizer frequency responses provided through frequency and time domain synthesis, respectively. Note the strong agreement between the two synthesis techniques, as well as with the desired frequency response $\mathbf{H}_{\mathrm{des}}$.

The purple and cyan traces show the result of filtering channel characterization data using each equalizer. A flat magnitude and phase response shows good agreement between the equalizer outputs and the reference waveform, although the frequency ripple present within the channel characterization data is also present at the equalizer outputs. Equalizer frequency response data are provided in Appendix A.

1) *Equalizer Latency Optimization:* As mentioned in Section II-C, equalizer effectiveness is a function of its latency, which can be adjusted by delaying the reference waveform prior to filter synthesis. Fig. 6 shows the CPCRs and residual tracking errors as a function of prescribed group delay Δm_{g}. We synthesized equalizers using (12) and (13) for a series of prescribed group delays ranging from 0 samples to the instantiated filter length $L = 15$ samples at a step size of $\frac{1}{8}$-sample. Frequency domain synthesis results are given in the left column while time domain synthesis results are given in the right column. The optimum delay is near $\Delta m_{\mathrm{g}} \approx 9$ samples, but varies from channel to channel and between each synthesis technique. As previously mentioned, a delay of 0 samples results in particularly poor performance.

When incorporating the $\frac{1}{8}$-sample fractional-sample delay filter bank, we sought the optimum block of eight sets of coefficients, providing the necessary fractional-sample delay range. It is important to note that although individual channels may show better performance at different delays, matched channel delay is necessary for beamsteering operations. Hence, the optimum delay block was selected based on cumulative channel data rather than individual performance. As all six channels were fairly well-behaved, we selected the block with the highest total CPCR, or the lowest residual tracking error.

Namely, we averaged CPCR for each channel over each potential block of eight delays and selected the block for which the cumulative mean CPCR, summed over all channels, was greatest. This was also carried out for the residual tracking error, seeking the minimum cumulative mean. The prescribed group delay of the resulting delay blocks, denoted by the vertical bands in Fig. 6, differ depending on synthesis technique. As the performance metrics are generally flat near the optimum delay, subtle differences between the two synthesis techniques such as the frequency-weighting function $\mathbf{W}$ in (12) can cause differences in the resulting filter bank group delay. Also of note is the slight variation between frequency domain synthesis CPCR and residual tracking error, also due to the frequency-weighting function $\mathbf{W}$ incorporated in (15) but not accounted for in the CPCR. For implementation, filter banks were selected using the residual tracking error criteria.

The channel 3 filter bank frequency response for both synthesis techniques is shown in Fig. 7, along with the equalizer output for each delay. The level traces correspond to the filter output, indicating effective equalization. The nonlevel traces correspond to the filter frequency response—each delay step is given by a different color. The time domain synthesis filter bank is given by solid traces while the frequency domain synthesis filter bank is given by dashed traces. Phase data show the increased group delay for each delay step while magnitude data show little variation within the band of interest. This is expected, as the magnitude response should remain consistent between delay steps while the phase slope of the filter response should increase by the corresponding delay. Agreement

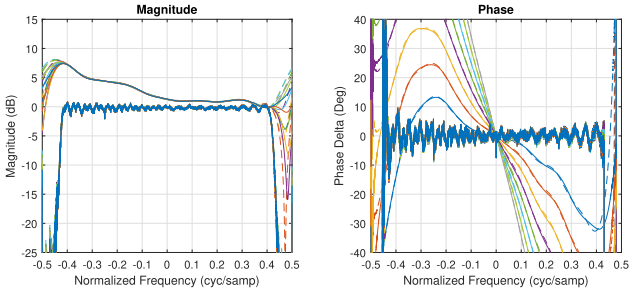

Fig. 7. Channel 3 equalized fractional-sample delay filter banks for frequency domain synthesis and time domain synthesis at $\frac{1}{8}$-sample steps. Solid traces—time domain synthesis. Dashed traces—frequency domain synthesis. Colors correspond to a given delay step.

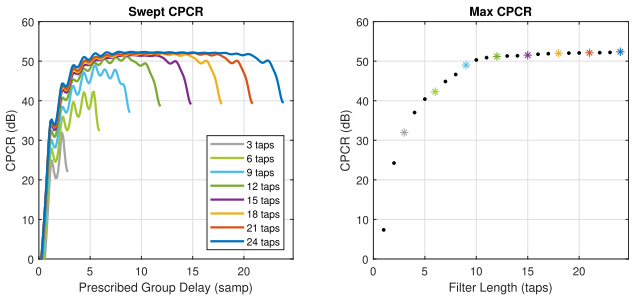

Fig. 8. Channel 3 CPCR for various filter lengths. Left—CPCR versus prescribed group delay. Right—optimum CPCR versus filter length.

between the two synthesis techniques can be seen most easily by correspondence between pairs of phase data for each delay step. Additionally, there is very strong agreement between equalized output data for each filter bank as all eight outputs of each synthesis technique virtually eclipse each other.

2) *Equalizer Filter Length:* Equalizer performance is also dependent on filter length, which is often constrained by system resources. The CPCR for channel 3 is shown in Fig. 8 for various filter lengths. The left plot shows CPCR versus prescribed group delay Δm_{g}, similar to the top row of Fig. 6. Each color corresponds to a select filter length with $\Delta m_{\mathrm{g}} \in [0, L]$, where L is the given filter length. The right plot shows the maximum CPCR for each filter length, with lengths shown in the left plot denoted with an asterisk of the corresponding color. Although dependent on the given channel characteristics, we see a point of diminishing returns around a filter length of 10–15 taps. Here, the CPCR response flattens out, plateauing near 52 dB. It is expected that a more dispersive channel would require a longer filter to reach this point of diminishing returns.

For this specific characterization data, simulations show an improvement in CPCR of about 5 and 8 dB around 30 and 45 taps, respectively. At these lengths, filter fidelity becomes capable of compensating higher order components of the mismatch ripple in the channel characterization data. This is not explored further for two reasons. First, the required filter lengths are impractical under our resource constraints. Second, the ripple in the channel characterization data is due to mismatches between the RFSoC DAC

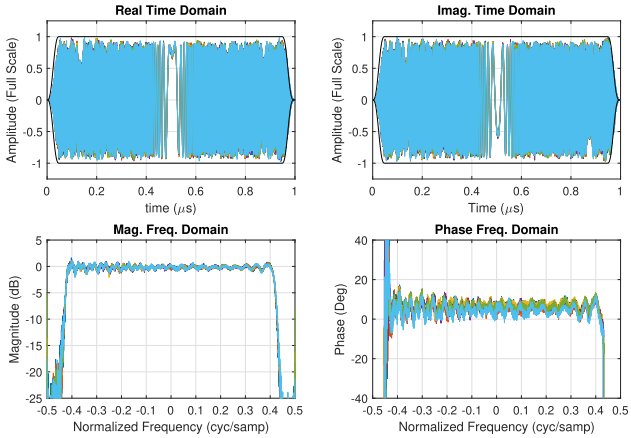

Fig. 9. Channel 1–6 equalizer response via frequency domain synthesis. Top left: real time domain. Top right: imaginary time domain. Bottom left: frequency domain magnitude. Bottom right: frequency domain phase.

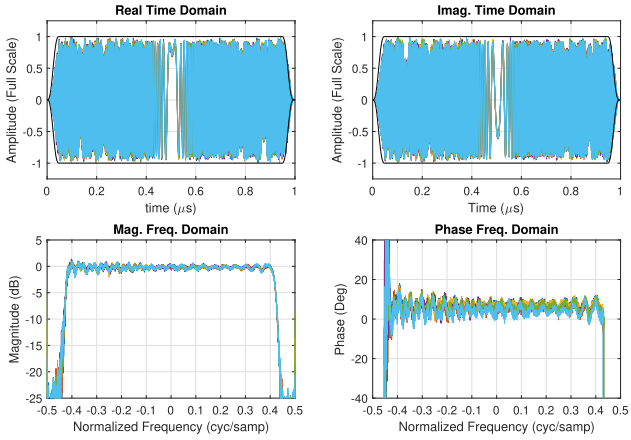

Fig. 10. Channel 1–6 equalizer response via time domain synthesis. Top left: real time domain. Top right: imaginary time domain. Bottom left: frequency domain magnitude. Bottom right: frequency domain phase.

and ADCs under the characterization configuration outlined in Fig. 1. For chamber measurements, the ADCs interface with the aperture elements, resulting in different mismatch characteristics.

3) *Time/Frequency Domain Synthesis Comparison:* Both frequency domain synthesis and time domain synthesis yield strong results. Equalizer output results using frequency domain synthesis are shown in Fig. 9 and output results using time domain synthesis are shown in Fig. 10. Both figures show effective equalization of the channel characterization data given in Fig. 4. Although there is little discernable difference between the plots of Figs. 9 and 10, the difference in CPCR between frequency domain synthesis and time domain synthesis is given in Fig. 11. Negative traces indicate superior performance of time domain synthesis to frequency domain synthesis, which is seen for any delay greater than one sample. It should be noted that this difference is quite small and almost vanishes near the optimum prescribed group delay of $m_{\mathrm{g}} \approx 9$ samples. Given that the difference between the two synthesis techniques

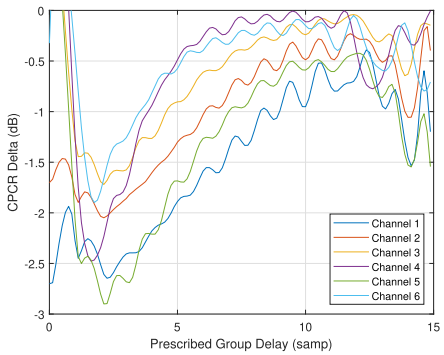

Fig. 11. CPCR delta between frequency domain and time domain synthesis.

decreases with increasing delay Δm_g, instances for which filter length is more limited may see a slight benefit from utilizing time domain synthesis over frequency domain synthesis.

C. Complex Coefficient Filter Implementation

In an uncalibrated complex baseband beamformer, individual channel compensation relies on a pair of real-valued fractional-sample delay filter instantiations. Each filter operates independently on the I or Q complex baseband signal samples such that

$$\mathbf{x}_{\text{out,r}} = \mathbf{h}_{\text{ttd}} * \mathbf{x}_{\text{ch,r}} \tag{20}$$

and

$$\mathbf{x}_{\text{out,i}} = \mathbf{h}_{\text{ttd}} * \mathbf{x}_{\text{ch,i}} \tag{21}$$

where $\mathbf{x}_{\text{ch,r}}$ and $\mathbf{x}_{\text{ch,i}}$ represent the I and Q data streams, respectively. Given that a channel equalizer operating on a complex baseband waveform generally does not have conjugate symmetry, a complex-coefficient filter is required.

By leveraging Karatsuba multiplication [46], a complex coefficient filter can be implemented using three real-valued convolutions, at the cost of some pre- and postarithmetic, as described by

$$\mathbf{x}_1 = \mathbf{h}_{\text{r}} * \mathbf{x}_{\text{ch,r}} \tag{22}$$

$$\mathbf{x}_2 = \mathbf{h}_{\text{i}} * \mathbf{x}_{\text{ch,i}} \tag{23}$$

and

$$\mathbf{x}_3 = (\mathbf{h}_{\text{r}} + \mathbf{h}_{\text{i}}) * (\mathbf{x}_{\text{ch,r}} + \mathbf{x}_{\text{ch,i}}). \tag{24}$$

The real and imaginary output components are given by

$$\mathbf{x}_{\text{out,r}} = \mathbf{x}_1 - \mathbf{x}_2 \tag{25}$$

and

$$\mathbf{x}_{\text{out,i}} = \mathbf{x}_3 - \mathbf{x}_1 - \mathbf{x}_2. \tag{26}$$

One must ensure sufficient bit allocation to account for the bit growth associated with the summations in (24)–(26). Additionally, it is important to note that by computing the real and imaginary outputs after the accumulate step in the convolutions given in (22)–(24), FIR convolution resources can be instantiated independent from the each other, simplifying FPGA routing.

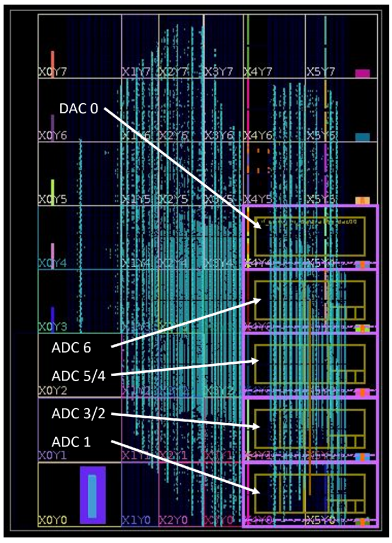

Fig. 12. Wideband beamformer design layout for the RFSoC.

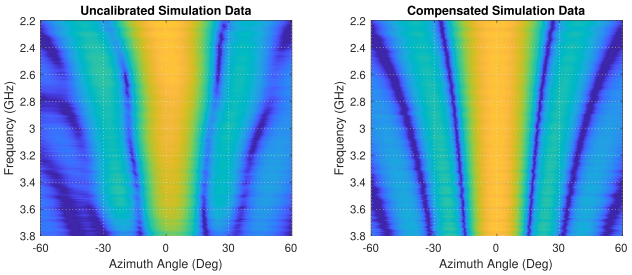

Fig. 13. Equalizer boresight simulation results. Left—uncalibrated data. Right—compensated data.

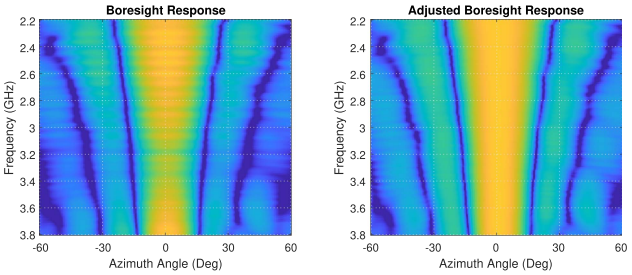

Fig. 14. Vivaldi aperture boresight pattern. Left—raw data. Right—postprocessed data.

Each channel compensation filter utilizes three instantiations of an interleaved filter design, corresponding to (22)–(24). The full digital bandwidth, interleaved implementation requires eight separate filter instantiations to process complex-valued samples at 2 GSPS at a clock rate of 500 MHz. Thus, the RFSoC digital signal processor (DSP) slice requirements for the implementation of a 15-tap complex coefficient FIR beamformer consists of three multipliers per tap, eight filter instantiations per channel, and six channels totaling 2160 multipliers. The FPGA floorplan is provided in Fig. 12, showing the layout of the routed FPGA design. Table I provides resource utilization. Of note

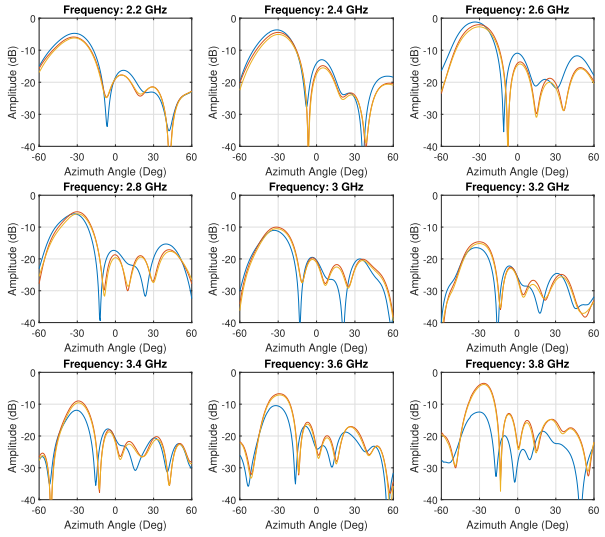

Fig. 15. Frequency cuts for $\theta_{st} = -30^\circ$. Blue—uncalibrated. Red-orange: frequency domain synthesis equalization. Yellow—-time domain synthesis equalization.

TABLE I
FPGA Resource Utilization for the Wideband Beamformer With Equalizer

Resource	Utilization	Available	%
LUT	78237	425280	18.4
LUTRAM	3199	213600	1.5
FF	124249	850560	14.6
BRAM	62	1080	5.7
DSP	2256	4272	52.8
IO	35	347	10.1
BUFG	7	696	1.0
MMCM	1	8	12.5

is the DSP slice usage rate of 52.8%. A gain/attenuator block in each channel utilizes 16 multipliers, in order to simultaneously process eight complex-valued samples. This results in a total of 2256 DSP slices for the wideband beamformer.

IV. RESULTS

This section discusses simulated and measured data demonstrating equalizer performance. Chamber measurements demonstrate broadband performance at various steering angles for uncalibrated and calibrated configurations.

A. Simulation Results

To generate an estimate of the uncalibrated antenna response, we provided measured channel characterization data to our bit-accurate wideband antenna model. The boresight response is given in the left plot of Fig. 13, which shows reasonable agreement with the measured uncalibrated boresight pattern shown in the left plot of Fig. 16. The calibrated simulation antenna pattern was generated by passing channel characterization data through the synthesized channel equalizer filter bank. The result, via time domain synthesis, is provided in the right plot of Fig. 13 and shows effective equalization. The effects of the characterization data frequency ripple can be seen throughout the bandwidth near the pattern nulls.

B. Chamber Measurements

This section presents chamber measurement results for the equalized wideband digital beamformer, shown in our far-field anechoic chamber in Fig. 3. Azimuth patterns consist of $\pm 60^\circ$ sweeps at 0.5° increments. At each angular step, we captured a frequency sweep from 2.2 to 3.8 GHz at 10 MHz steps. Patterns were captured for three system configurations: 1) uncalibrated wideband beamforming, 2) equalized wideband beamforming via frequency domain synthesis, and 3) equalized wideband beamforming via time domain synthesis. For each configuration, the beamformer was commanded to steer to $\theta_{st} = 0^\circ$, -15°, -30°, and -45°. 2-D wideband patterns are provided for all steering angles along with frequency cuts for $\theta_{st} = -30^\circ$.

1) *Amplitude Postprocessing:* The raw boresight pattern for the 6-element Vivaldi array is shown in the left plot of Fig. 14. This pattern was captured with the aperture elements connected to a broadband power splitter. The main beam amplitude varies over frequency due to the chamber probe and Vivaldi aperture effects, which were not captured during channel characterization. To compensate the measured patterns, we extracted the frequency response from the main beam of the raw boresight pattern and applied its inverse as a correction factor across each azimuth angle. The result is shown in the right plot of Fig. 14, in which the main beam shows constant intensity. Subsequent plots incorporate this correction factor.

2) *Compensated Results:* Frequency cuts steered to $\theta_{st} = -30^\circ$ for the uncalibrated response, equalized response via frequency domain synthesis, and equalized response via time domain synthesis are shown in Fig. 15. The blue traces show the uncalibrated response and the red-orange and yellow traces show the equalized response for frequency and time domain synthesis, respectively. Frequency cuts span the 1.6-GHz bandwidth at 200-MHz steps. Of note is the steering error in the uncalibrated response, which is consistently off by about 3° up until the higher end of the band, when all configurations shift to the right. Except for the 2.4-GHz cut, sidelobe behavior is consistently superior in the calibrated patterns as compared to the uncalibrated response, indicating a general improvement in channel coherency. There is an appreciable drop in gain toward the center of the band, despite the amplitude correction just discussed. We hypothesize that this is due to mismatch between the aperture elements and RFSoC ADCs, effects that are not accounted for in our current configuration or amplitude postprocessing. Additionally, matching differences between the characterization configuration shown in Fig. 1 and operating configuration may exacerbate these effects.

Two-dimensional wideband patterns showing the antenna response as a function of both azimuth angle and frequency steered to $\theta_{st} = 0^\circ$, -15°, -30°, and -45° are shown in Figs. 16–19. As mentioned regarding the frequency cuts,

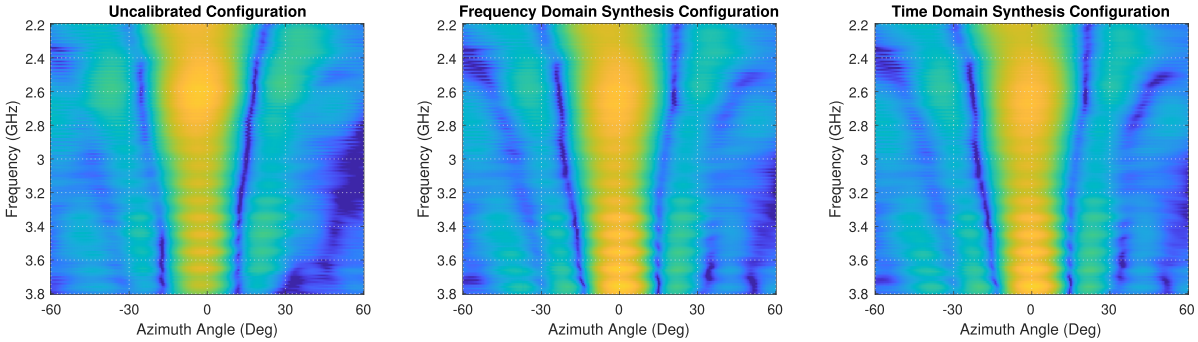

Fig. 16. Antenna patterns for $\theta_{st} = 0^{\circ}$. Left—uncalibrated. Center—frequency domain synthesized equalizer. Right—time domain synthesized equalizer.

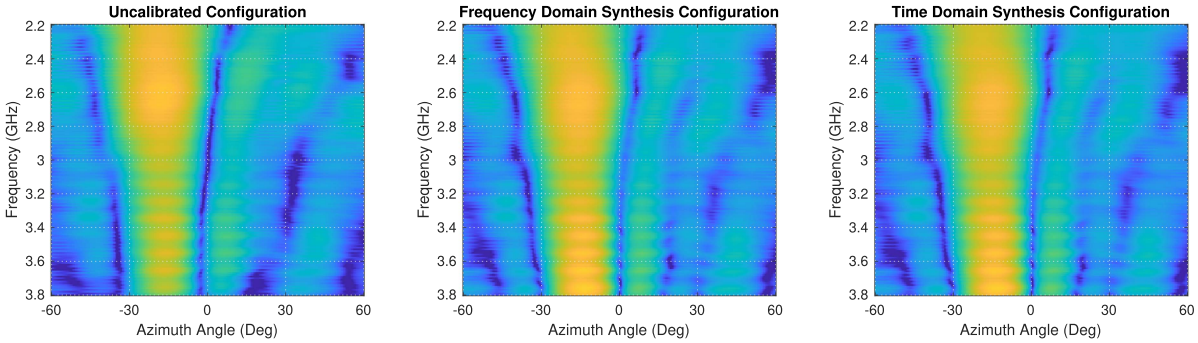

Fig. 17. Antenna patterns for $\theta_{st} = -15^{\circ}$. Left—uncalibrated. Center—frequency domain synthesized equalizer. Right—time domain synthesized equalizer.

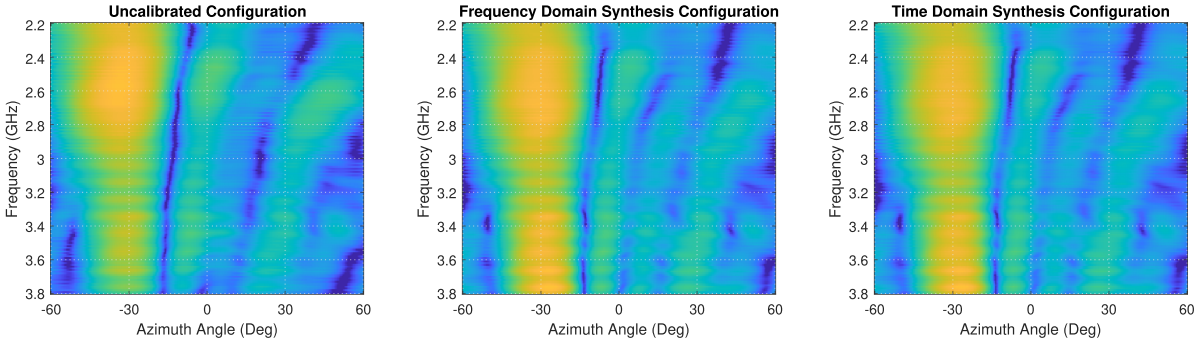

Fig. 18. Antenna patterns for $\theta_{st} = -30^{\circ}$. Left—uncalibrated. Center—frequency domain synthesized equalizer. Right—time domain synthesized equalizer.

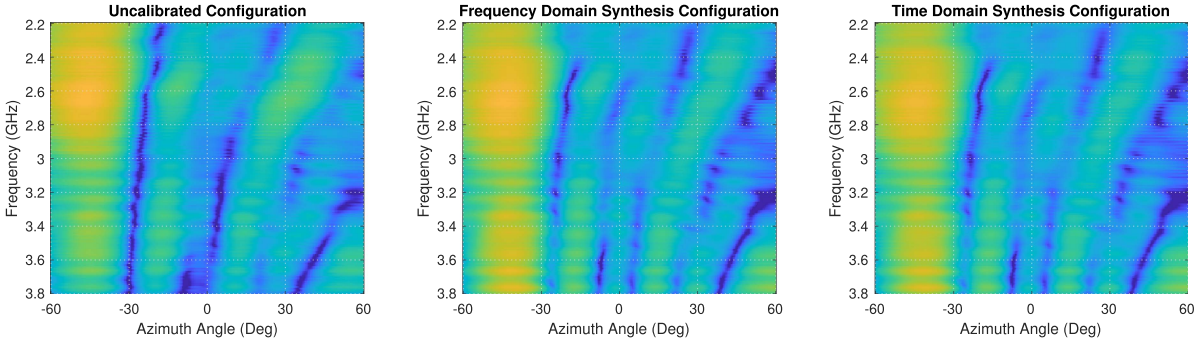

Fig. 19. Antenna patterns for $\theta_{st} = -45^{\circ}$. Left—-uncalibrated. Center—frequency domain synthesized equalizer. Right—time domain synthesized equalizer.

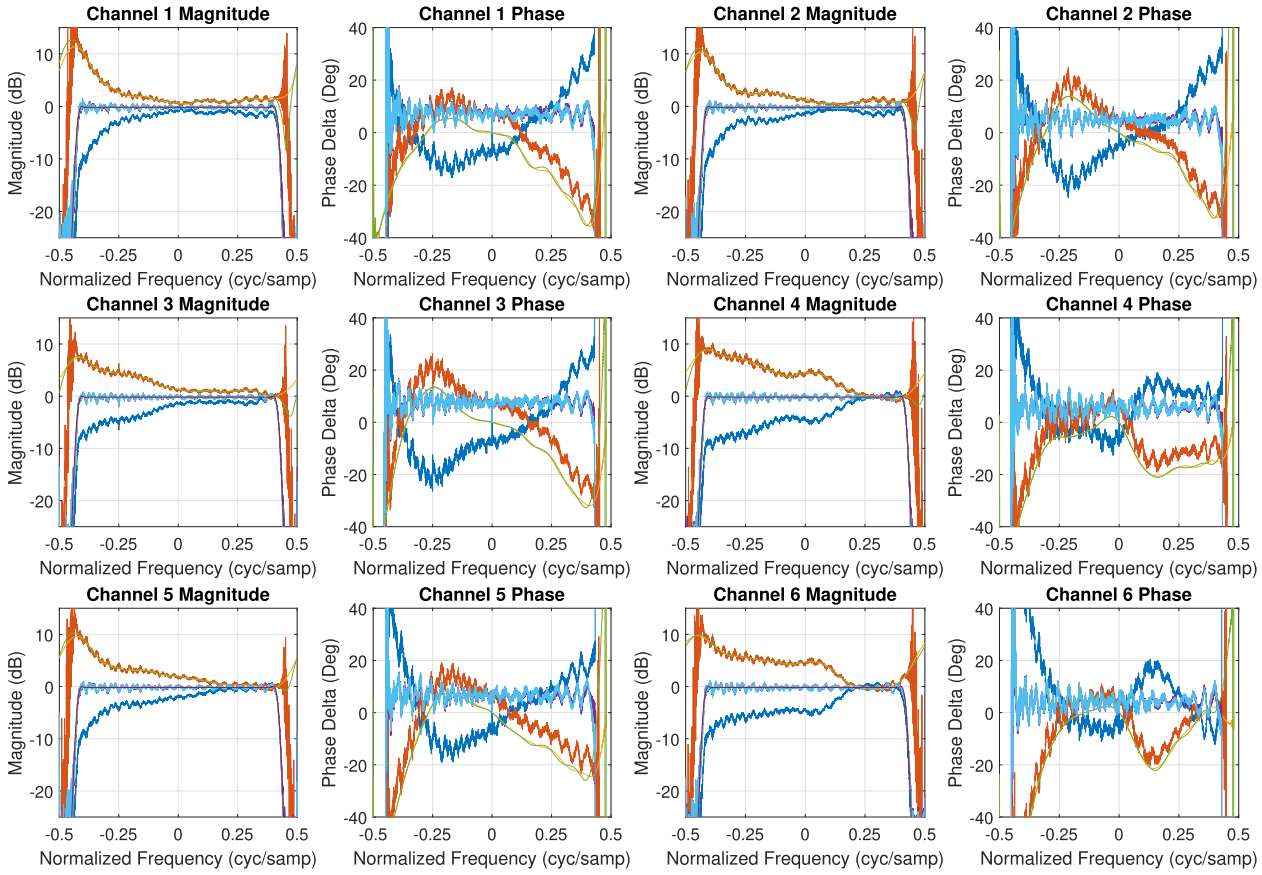

Fig. 20 Equalizer magnitude and unwrapped phase delta for channels 1–6. Dark blue—channel characterization data. Red-orange—desired filter response. Yellow—filter response via frequency domain synthesis. Green—filter response via time domain synthesis. Purple—filter output via frequency domain synthesis. Cyan—filter output via time domain synthesis. Black—window function for frequency domain synthesis.

steering accuracy shows noticeable improvements in the equalized responses as compared to the uncalibrated response. Additionally, sidelobes appear merged together in the uncalibrated responses over steering angles. Although sidelobe nulls are not deep in the equalized responses, they do sure noticeable improvements. Lastly, main beam strength is more consistent throughout the system bandwidth, particularly at the higher end of the calibrated patterns.

3) *Future Efforts:* Notable factors that contribute to suboptimal behavior include the following. First, mismatch between the antenna elements and ADCs results in ripple across the system bandwidth, which is not captured in the channel characterization data and cannot be compensated at the practical equalizer lengths of this RFSoC. If this mismatch is significant enough to impact the lower order phase response, which is compensated by the equalizer, there will disagreement between the channel equalizer and the realized channel response. Second, system characterization disregarded the effects of mutual coupling, which is particularly influential in the Vivaldi aperture due to its reliance on mutual coupling to meet performance metrics. Longbrake *et al.* [8] explored this further by fitting their measurements to an array model in which they includes coupling terms between adjacent elements. By solving for coupling terms using their measured data, they successfully modeled a reasonable approximation of their measurements. Sidelobe behavior and null depth in their measurements show similarities to those captured herein.

V. CONCLUSION

We have confirmed our hypothesis that an RFSoC could be used as the replacement for the typical radar front end in wideband beamforming modes. In brief, compact RFSoC devices are geared toward the next-generation telecommunication industry, such as 5G and 6G, yet they provide an ideal technology platform for the future of phased-array radar for three reasons: 1) sample synchronization across multiple channels is readily possible, 2) low power consumption, and 3) compact form factor. For the first time, the authors have developed an equalizer design methodology for an uncalibrated 8-element RFSoC-based wideband beamformer with accompanying wideband antenna. This technology allows the digital domain to be substantially closer to the phased-array aperture, while eliminating most of the analog radar front end. Bandpass sampling enables digital representation of bandpass signals sampled below the Nyquist rate. Sampled signals alias from higher Nyquist zones to within the digital spectrum without requiring

frequency conversion. This drastically simplifies the analog circuitry as traditional up/down conversion circuits are not needed. Our laboratory results were able to confirm eight ADC channels operating each at an astonishing 4 GSPS on 1.6 GHz of bandwidth using a wideband Vivaldi array centered at 3 GHz. These are impressive results that will help shape the momentum of the next generation of phased-array radars.

APPENDIX
EQUALIZATION DATA

This appendix provides characterization data for channels 1–6 and equalizer synthesis results for both synthesis techniques. Individual channel data for frequency domain and time domain synthesis are provided in Fig. A1. In each plot, the dark blue trace shows measured characterization data for the given channel. The red-orange trace shows the desired filter response. The yellow and green traces show the synthesized filter responses while the purple and cyan traces shows the equalizer output data. The black traces in the magnitude plots show the window function implemented in the diagonal matrix **W** for frequency domain synthesis.

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The views, opinions expressed, and/or findings contained in this report are those of the authors(s), do not necessarily represent the opinions of the U.S. Government.

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