An Affordable IMA Bridge for Refreshing Deployed Avionics Systems

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Outline

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- Emerging "IMA Like" Derived Needs for Deployed Systems
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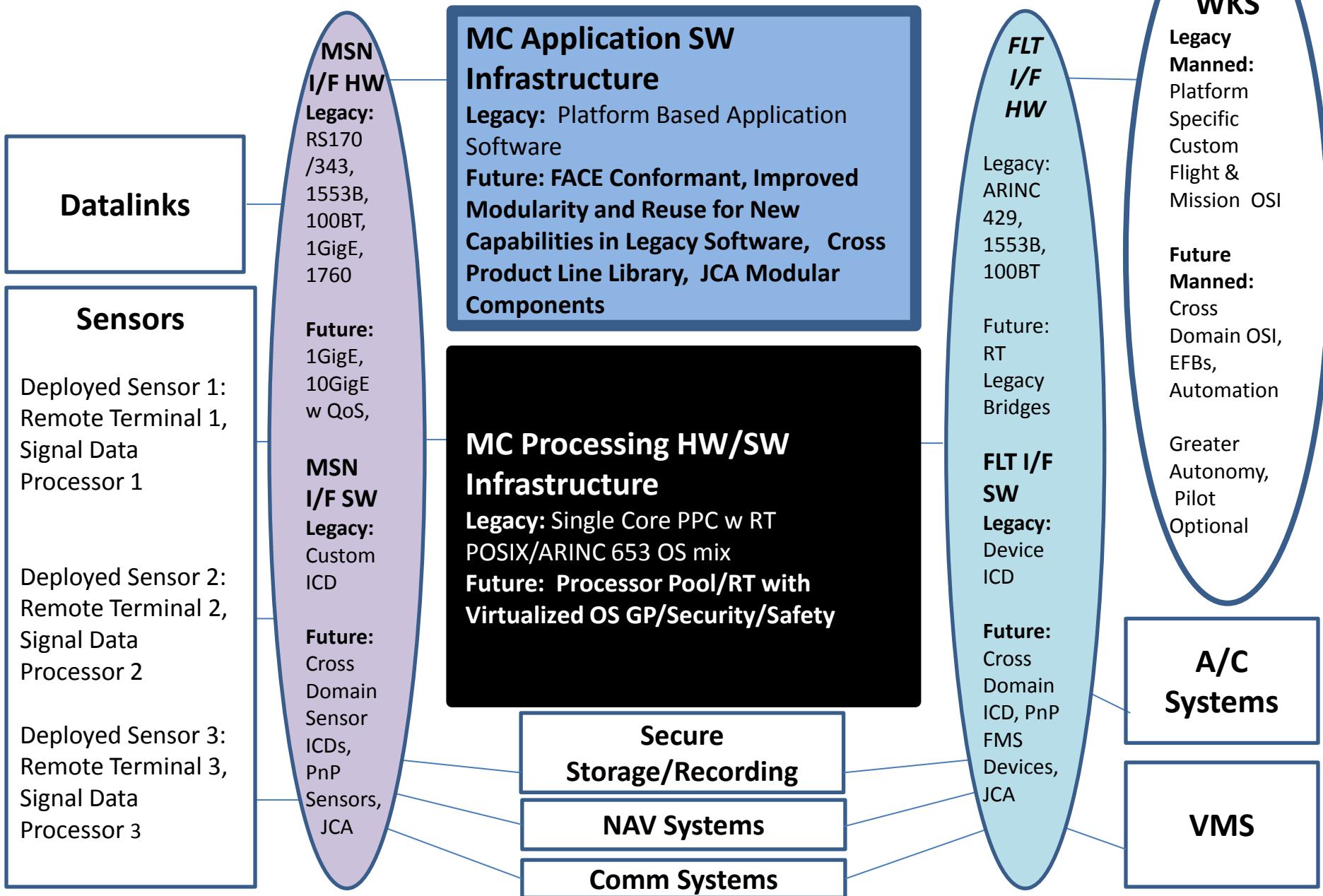
Deployed System Challenges

- Deployed avionics systems must add new capabilities at affordable cost without disruption of the installed base and while accommodating legacy architecture constraints

- Today's deployed avionics solutions have with computer resources by estimating the future processing, I/O and software infrastructure requirements for these new capabilities and providing installed growth

- Due to spiral funding, these systems were developed and extended incrementally and have 3-4 generations of processing and software infrastructure components on onboard

- In addition, interface definition and standards of hardware and software components have typically been driven by the mixture of existing and new development items and the open architecture standards of the time

Ideal IMA Architecture Context

- Ideal IMA architecture is based on a high-integrity, partitioned environment that hosts multiple avionics functions of different criticalities on a shared computing platform
  - Common processing subsystems: Allow multiple applications to share and reuse the same computing resources (Common processor card)
    - Benefit: Results in a reduced number of subsystems that need to be deployed and more efficient use of system resources, leaving space for future expansion
  - Common software environment: isolates the application not only from the underlying bus architecture but also from the underlying hardware architecture (Common Time and Space Partitioned Operating System, Middleware and Network with QoS)
    - Benefit: Enhances portability of applications between different platforms and also enables the introduction of new hardware to replace obsolete architectures
  - Common software services (Common system management and control)
    - Benefit: Reduces development time while affording the developer a method of redeploying existing applications without extensive modification
- Many deployed systems have partial IMA solutions based on funding cycles
  - Bridging IMA into deployed systems is a combination of Tech Refresh in HW and SW coupling with new capability insertion => Need an IMA Figure of Merit

Example Deployed System Legacy and Future IMA Drivers

Datalinks

Sensors

Deployed Sensor 1: Remote Terminal 1, Signal Data Processor 1

Deployed Sensor 2: Remote Terminal 2, Signal Data Processor 2

Deployed Sensor 3: Remote Terminal 3, Signal Data Processor 3

MSN I/F HW

Legacy: RS170/343, 1553B, 100BT, 1GigE, 1760

Future: 1GigE, 10GigE w QoS,

MSN I/F SW

Legacy: Custom ICD

Future: Cross Domain Sensor ICDs, PnP Sensors, JCA

MC Application SW Infrastructure

Legacy: Platform Based Application Software

Future: FACE Conformant, Improved Modularity and Reuse for New Capabilities in Legacy Software, Cross Product Line Library, JCA Modular Components

MC Processing HW/SW Infrastructure

Legacy: Single Core PPC w RT POSIX/ARINC 653 OS mix

Future: Processor Pool/RT with Virtualized OS GP/Security/Safety

Secure Storage/Recording

NAV Systems

Comm Systems

FLT I/F HW

Legacy: ARINC 429, 1553B, 100BT

Future: RT Legacy Bridges

FLT I/F SW

Legacy: Device ICD

Future: Cross Domain ICD, PnP FMS Devices, JCA

0-N WKS

Legacy Manned: Platform Specific Custom Flight & Mission OSI

Future Manned: Cross Domain OSI, EFBs, Automation

Greater Autonomy, Pilot Optional

A/C Systems

VMS

Establishing an IMA Figure of Merit

IMA Component Attribute	Relevant Processing Subsystems	Common Component Criteria	IMA Ideal Value	Deployed Actual	IMA Factor
Processing LRUs/SRAs	4: Sensor 1 SDP, Sensor 2 SDP, Sensor 3 SDP, MC	Number of Unique Processor Board Types	3: SP (1), DP (1) GP (1)	12: Sensor 1 (4), Sensor 2 (2.5), Sensor 3 (2), MC (3.5)	0.25
Middleware	"	Number of Unique Middleware	1 Unified	4: Sensor 1 (2), Sensor 2 (0.5), Sensor 3 (1), MC (0.5)	0.25
Operating Systems	"	Number of Unique Operating Systems	1 Unified	5: Sensor 1 (2), Sensor 2 (0.5), Sensor 3 (1), MC (1.5)	0.2
System Management and Control	"	Unique Components for System Management	1 Unified	4: Sensor 1 (2), Sensor 2 (1), Sensor 3 (1), MC (1)	0.25
Interconnection Types	"	Number of Primary Networks	2: 1 BP, 1 Net	4: GigE, VME, 1553, Fabric	0.5
Custom SLOC	"	% SLOC by Subsystem	Pooled Processing Cluster	Sensor1 (20%), Sensor 2 (5%), Sensor 3 (5%), MC (70%)	0.7

Proposed Bridge Need for "IMA Like" Extensions

- A new set of affordability challenges are driving toward "IMA like" solutions with regard to:

    1.) Inserting IMA common multicore pooled processing for SWAP and cost reduction by leveraging Moore's Law

    2.) Extending hardware agnostic software environments across subsystems to support reduced life cycle support

    3.) Accommodating mixed legacy, FACE conformant, SOA, and cross platform domain software for improved reuse and interoperability

    4.) Addressing I/O migration issues in video, networking, and security

- The embedded world technologies of Pooled Server Processing, Virtualization, a Publish/Subscribe Infrastructure, and I/O Migration can serve as an IMA Bridge for refreshing deployed military avionics systems
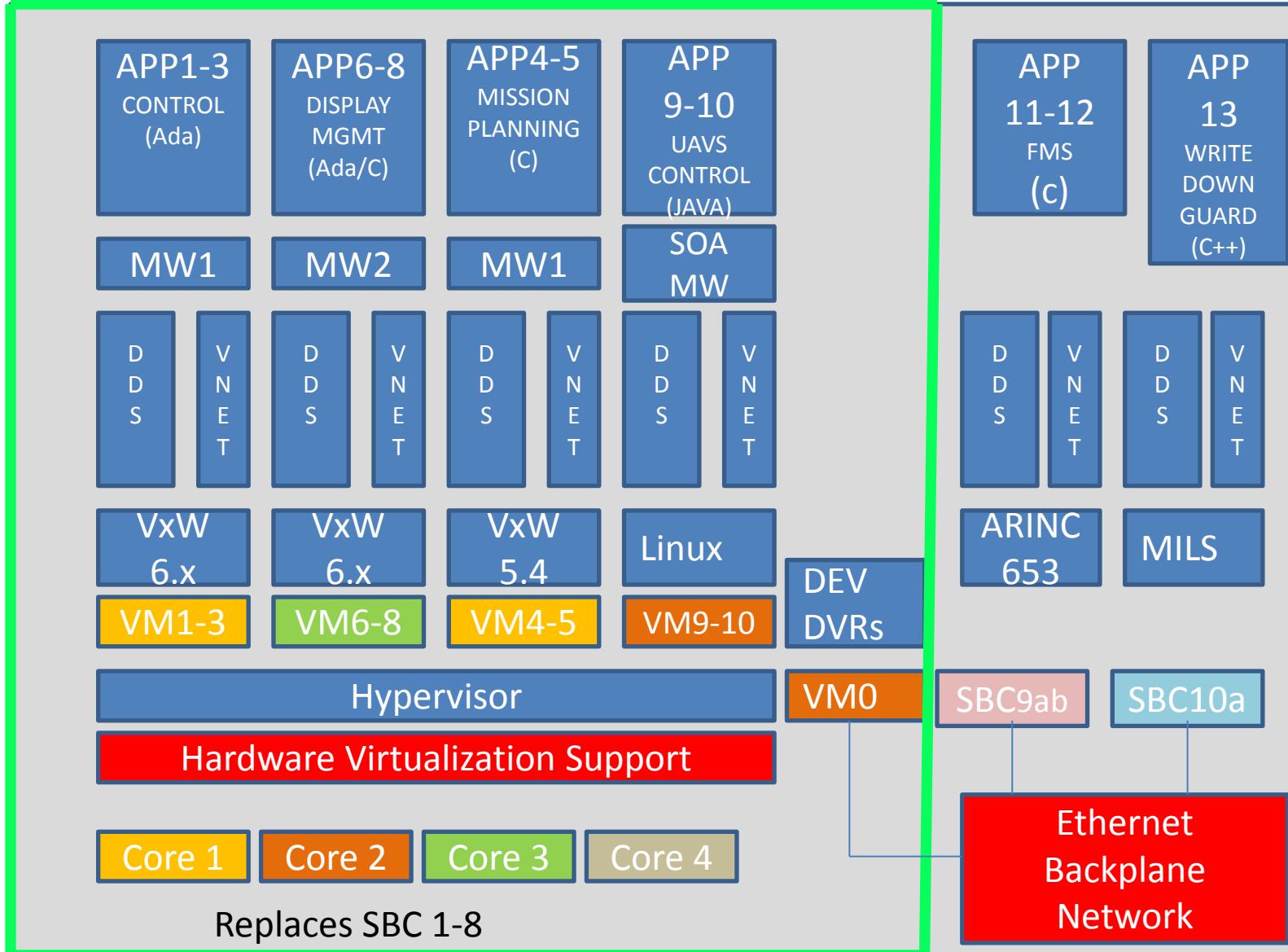
Emerging "IMA Like" Derived Needs for Legacy Systems

– Multicore Pooled Processing

  • Approach: Initially Adjunct insertion for maximum benefit

– Bridge across General Purpose Profile, Safety Critical, and Security HW Agnostic Software Environments Across Subsystems

  • Approach: Mixed Hypervisor environments

– Accommodate Mixed legacy, FACE Conformant, SOA, and Cross Platform Domain SW

  • Approach: Incrementally unify mixed infrastructure environment with Hypervisor and Publish/Subscribe

– I/O Transformation and Unification From: Legacy I/O and Analog Video To: Emerging I/O and Digital Video

  • Approach: Leverage I/O Adapter Gateways

Embedded Multicore Processing

- Enabler: Facilitate leveraging Moore's Law across mixed PowerPC heterogeneous systems and transition to Intel
- Impact: 25-100x RAW speedup per processor chip to legacy for general purpose computing
  - 400K Coremarks for 16 core Cannonlake (2017+)
  - 100K Coremarks for Quad core i7 Haswell (2014)
  - 4K CoreMarks Single core PowerPC 7448 (2005)
- Insertion Analysis: Need to migrate to split Power PC and Intel mixed environments
  - Small form factor computing enables incremental performance extensions via adjunct processing elements
- Benefit Target: Non safety critical avionics subsystems suitable for pooled processing
  - Benefit: IMA processing infrastructure SWAP reduction

Multicore Bridge to IMA Virtualization

| APP1-3 CONTROL (Ada) | APP6-8 DISPLAY MGMT (Ada/C) | APP4-5 MISSION PLANNING (C) | APP 9-10 UAVS CONTROL (JAVA) | | APP 11-12 FMS (c) | APP 13 WRITE DOWN GUARD (C++) |

| MW1 | MW2 | MW1 | SOA MW | | |

| D D S | V N E T | D D S | V N E T | D D S | V N E T | D D S | V N E T | | D D S | V N E T | D D S | V N E T |

| VxW 6.x | VxW 6.x | VxW 5.4 | Linux | DEV DVRs | ARINC 653 | MILS |

| VM1-3 | VM6-8 | VM4-5 | VM9-10 | | | |

| Hypervisor | VM0 | SBC9ab | SBC10a |

| Hardware Virtualization Support |

| Core 1 | Core 2 | Core 3 | Core 4 | | Ethernet Backplane Network |

Replaces SBC 1-8

Virtualization

- Enabler: Facilitate consolidation of software applications running on top of a mixed CPUs and operating systems, with little or no disruption to the existing software
- Impact: Enables SWAP consolidation and virtual board isolation with mixed guest OS environments on multicore
- Insertion Analysis:
  - Processing requirements legacy and emerging for General Purpose Profile, Safety Critical, and Security
  - Networking interconnection considerations legacy and emerging
- Benefit Target:
  - Enables processor pooling to start incrementally by leveraging adjunct processing then transition to block upgrade in future

Hypervisor Solutions for Safety, Security, General Purpose

| Characteristic	ARINC-653 Virtualization	MILS Virtualization	Embedded Hypervisor Virtualization
APIs	APEX		
Multicore Support	Multicore PPC	N	Multicore Intel
Support for Guest OSs	RTOS	Linux, High Assurance APIs	RTOS, Linux
Scheduling	APEX Scheduler	MILS Scheduler	Virtual Board Level
Local Communication Model	ARINC Sampling and Queuing Ports	Shared Memory and Queues Enforcing NEAT	Shared Memory, Queues, Virtual Networking
Distributed Communication Model	DO-178B TCP/IP, AFDX, TTE	PCS	TCP/IP, Virtual Networking
Middleware	DDS on Guest OS	DDS on Guest OS	DDS on Guest OS
Partitions	Time and Space	NEAT	Virtual Boards
Emerging Processing Density	Dependent on multi-core security improvements	Dependent on multi-core security improvements	More cores

Publish/Subscribe Infrastructure

- Enabler: Facilitate integration of software applications running on top of a multitude of CPUs and operating systems, with little or no disruption to the existing software using a publish-subscribe communication model
- Impact:
  - Allows distributed processes to share data without concern for the actual physical location, programming language, or architecture of their peers.
  - A fundamental benefit of DDS is simplifying otherwise complex distributed programming.
    - The publish-subscribe model is used for sending and receiving data, events and commands among network nodes
    - The job of DDS is to handle data transfer chores: message addressing, data marshaling and demarshalling (also called serialization and deserialization), delivery, flow control, retries, etc
    - Any application can be a publisher, subscriber, or both simultaneously. DDS provides many Quality of Service (QoS) policies specifically geared for real-time (deterministic) distributed systems
- Insertion Analysis: Partition architecture to leverage both standard DDS and Certifiable DDS
- Benefit Target:
  - Incremental extension of a unified data distribution environment that supports on board and offboard system-of-systems

Unified Publish/Subscribe General Purpose and Safety Critical

GENERAL PURPOSE STANDARDS BASED DDS + EMERGING
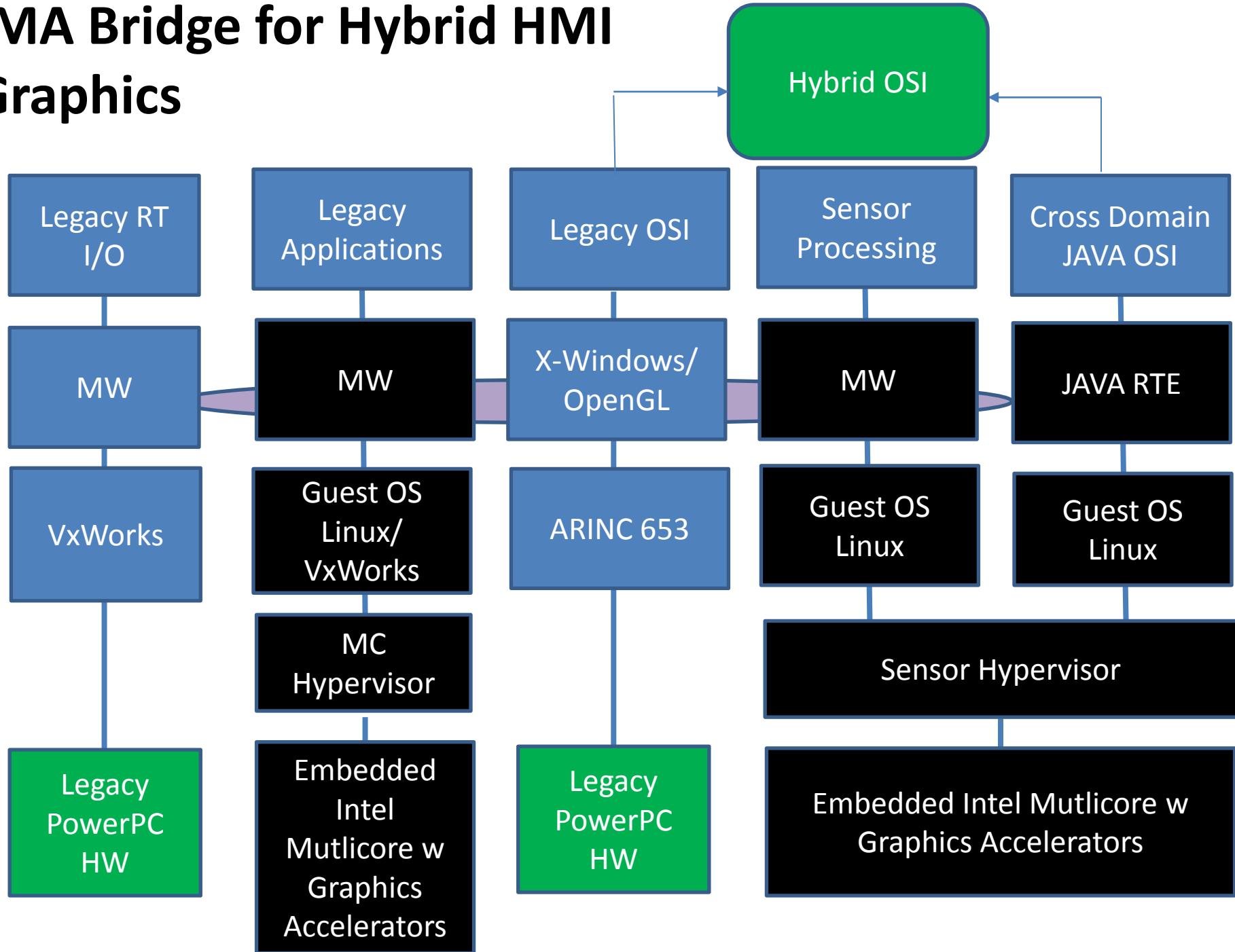
Certifiable DDS – Core Capabilities

- Support for multiple domains
- Domain Participant Factory
  - Create/delete Domain Participants
- Domain Participant
  - Create topics (keyed and keyless)
  - Create publications
  - Create subscriptions
  - Delete contained entities

- Subscription
  - Polling
  - Notification
  - Read/take
- Publication
  - Write with or without timestamp
  - Dispose
  - Liveliness
- Thread-safe

I/O Migration

- Enabler: Facilitate I/O migration with little or no disruption to the existing software
- Impact: Must not impact A/C wiring significantly and must be in place to support COTS mainstream networking
- Insertion Analysis:
  - Design to support both Legacy MC as remote terminal and refresh to new small form factor remote terminals
    - Incrementally migrate from legacy aircraft data interfaces, legacy analog video interfaces and legacy custom interfaces
  - Establish improved PnP interfaces with domain specific data representations
- Benefit Target:
  - Need to transition I/O to mainstream "everything is digital and networked IoT vision"
  - Embedded marketplace is now driven by mainstream COTS interfaces with considerations for information security and tamper resistance

IMA Bridge for Hybrid HMI Graphics
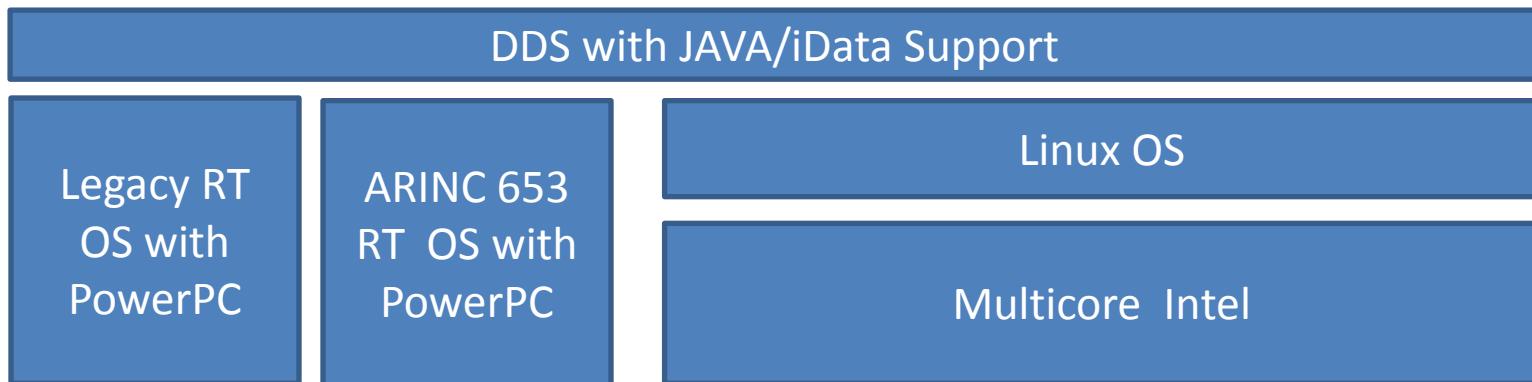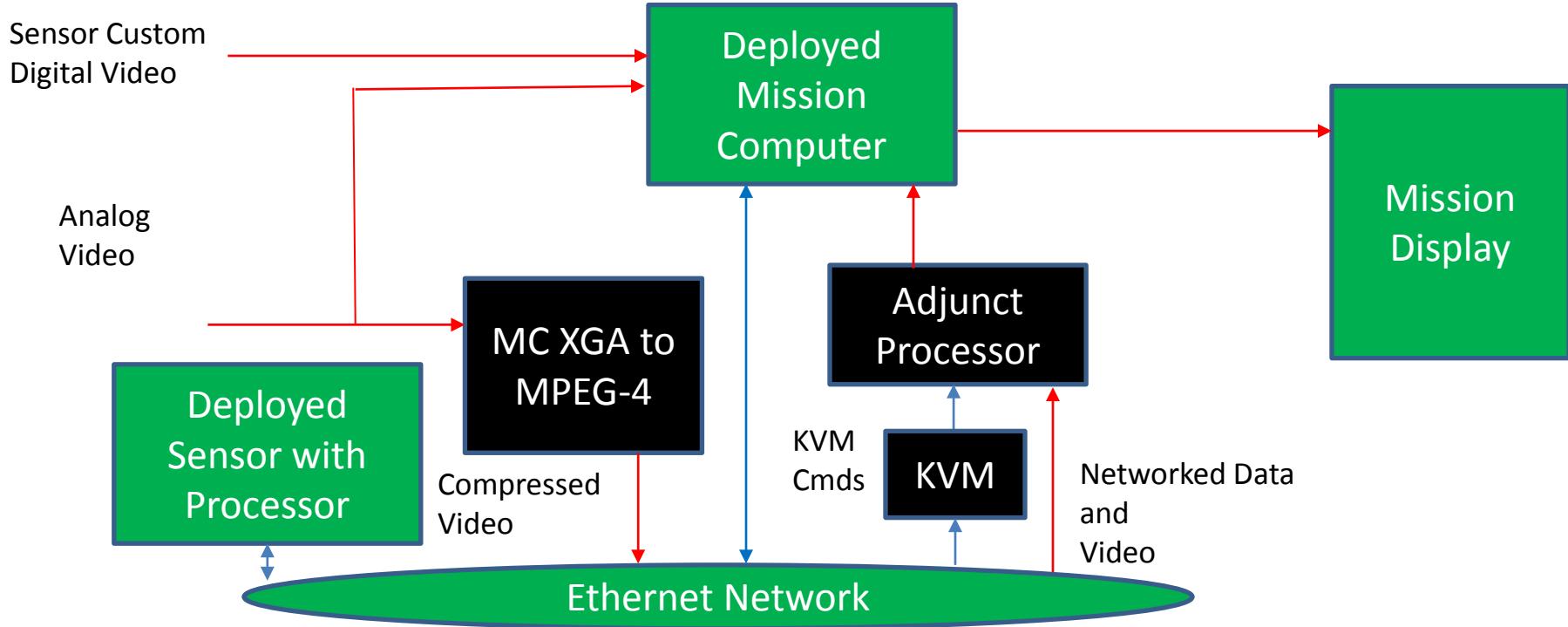
IMA Bridge Insertion Approach

1. **Select Processor Types and Throughput**
   - PowerPC Multicore, Intel Multicore
   - 3U VME/OpenVPX, 6U VME/OpenVPX, Small Form Factor
2. **Identify Operating System Guest OS Requirements based on Application Software "IMA Like" Considerations**
   - General-Purpose Guest OS, Security Guest OS, Safety Guest OS
3. **Identify Transport Services and any Bridges based on "IMA Like" Considerations**
   - Sockets, CORBA, DDS, World Wide Web Consortium (W3C)
4. **Identify I/O Services and I/O Migration Bridges**
   - Based on Data Flow Analysis and Wiring Impacts
5. **Architect System Management and HMI/Autonomy Bridges**
   - Based on Software Domain Specific Reuse considerations
   - JAVA HMI, Legacy X-Windows Based HMI , Model Based HMI
6. **Prototype Selected New Capability Candidates using an Adjunct Processor/Infrastructure Insertion Approach**
7. **Refine Payoff and Open Architecture of Clean Slate IMA Refresh Versus Adjunct Approach**
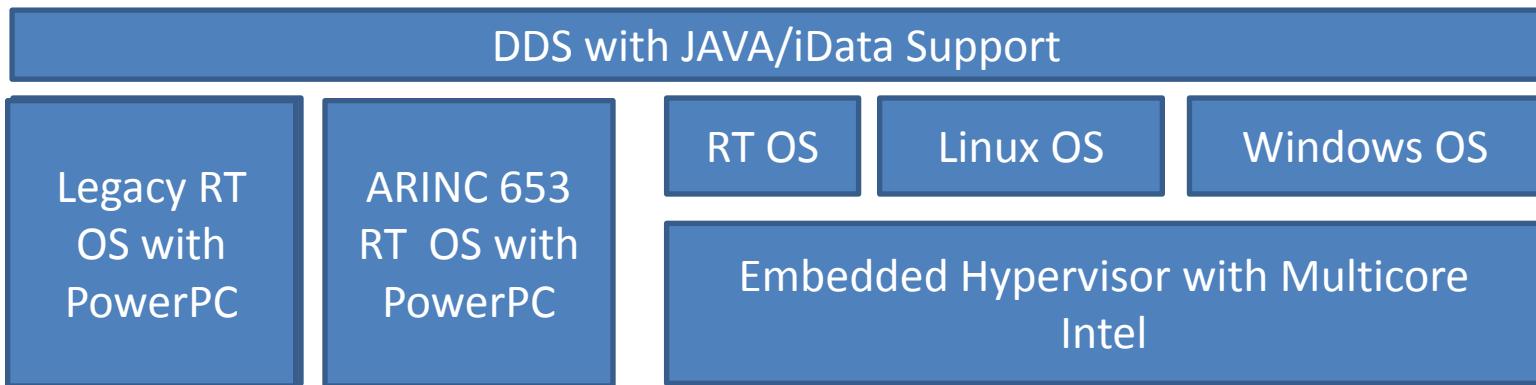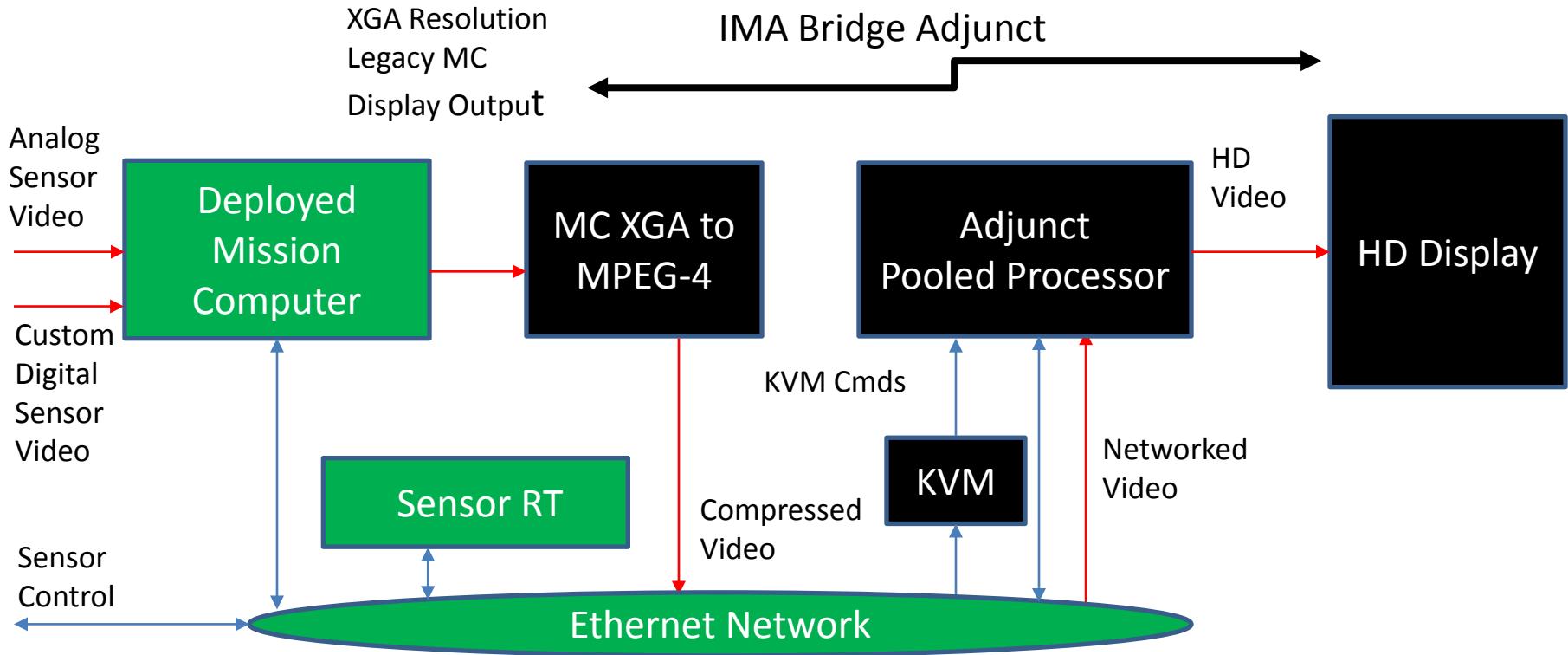
IMA Bridge Architecture Tradeoffs

Element	Legacy Constraints	Tech Refresh Driver Considerations
Multicore Processing	Single Core – Primary PowerPC with single chip/dual chip/quad chips on VME	Emergence of Intel Multicore over PowerPC in Embedded
Hypervisor	None or single core PowerPC with ARINC 653 time and space partitioning	Emergence of multiple hypervisor realizations
Publish/Subscribe	Custom middleware with point to point client/server services	Need to interface multiple middleware environments with multiple HMI environments
I/O Migration	MIL-STD-1553B, ARINC 429, Discrete I/O, 100BT/1000BT Ethernet, Analog Video, Custom Digital Video	Multiple QoS strategies for Ethernet unification based on general purpose, safety, and security
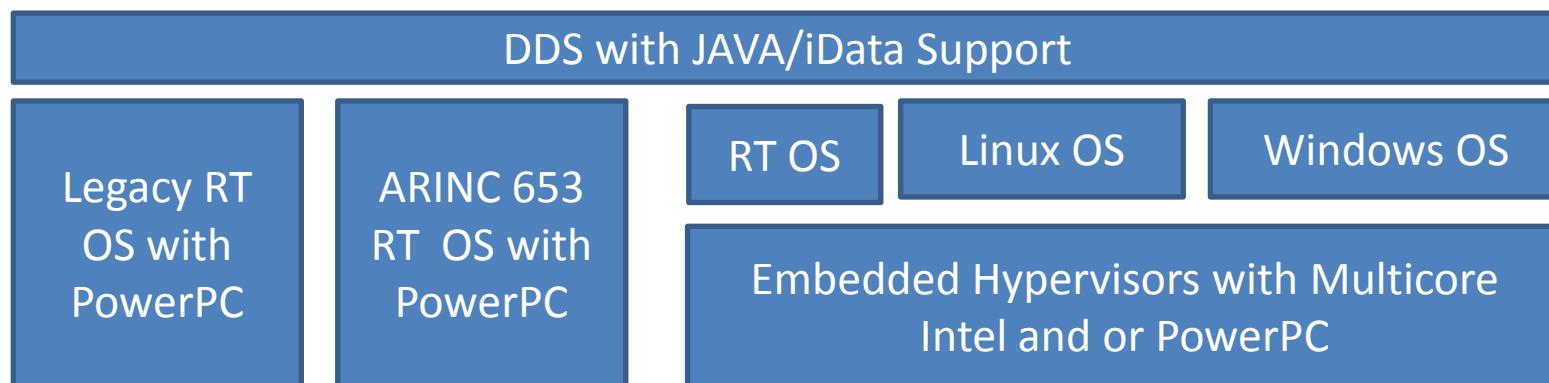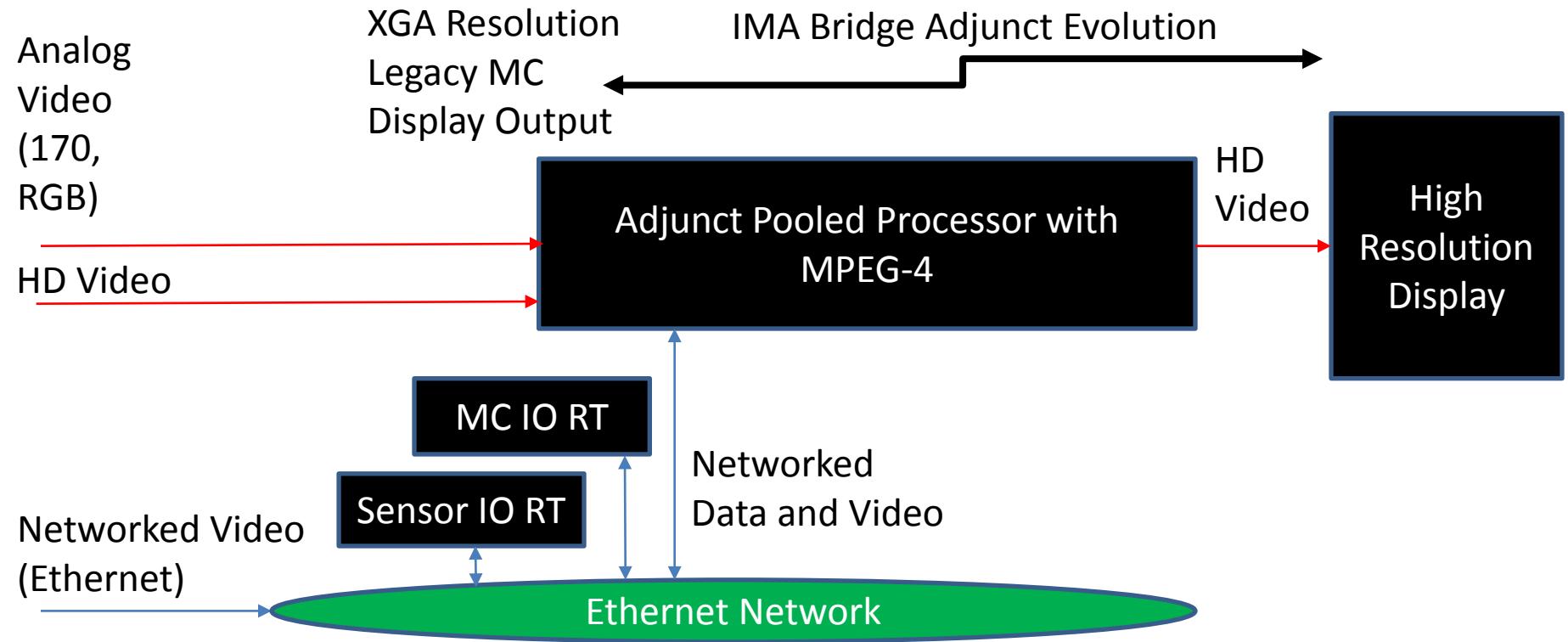
Adjunct Processor Smart Sensor Bridge

Sensor Custom
Digital Video

Analog
Video

Deployed
Mission
Computer

Mission
Display

Deployed
Sensor with
Processor

MC XGA to
MPEG-4

Adjunct
Processor

KVM
Cmds

KVM

Compressed
Video

Networked Data
and
Video

Ethernet Network

DDS with JAVA/iData Support

Legacy RT
OS with
PowerPC

ARINC 653
RT OS with
PowerPC

Linux OS

Multicore Intel

Adjunct Pooled Processor

XGA Resolution
Legacy MC
Display Output

IMA Bridge Adjunct

Analog Sensor Video

Deployed Mission Computer

MC XGA to MPEG-4

Adjunct Pooled Processor

HD Video

HD Display

Custom Digital Sensor Video

Sensor RT

KVM Cmds

KVM

Networked Video

Compressed Video

Sensor Control

Ethernet Network

DDS with JAVA/iData Support

Legacy RT OS with PowerPC

ARINC 653 RT OS with PowerPC

RT OS

Linux OS

Windows OS

Embedded Hypervisor with Multicore Intel

IMA Bridge Evolution

XGA Resolution Legacy MC Display Output

IMA Bridge Adjunct Evolution →

Analog Video (170, RGB)

HD Video

Adjunct Pooled Processor with MPEG-4

HD Video

High Resolution Display

MC IO RT

Sensor IO RT

Networked Data and Video

Networked Video (Ethernet)

Ethernet Network

DDS with JAVA/iData Support

Legacy RT OS with PowerPC

ARINC 653 RT OS with PowerPC

RT OS

Linux OS

Windows OS

Embedded Hypervisors with Multicore Intel and or PowerPC

Transformational Bridge IMA Enablers

Synergistic to FACE Safe & Secure Multicore => Incremental Intel Path with Mature Intel Hypervisor	**Bridges FACE Enterprise Profile and Next Gen TSS => Linux and DDS**	**Enables Desktop/ Tactical Training => Support for Mixed OS & GUIs**	**Extends Legacy Processing to Processor Pooling => Adjunct 16 Core Intel Processors by 2016**	**Enables Rapid SW Insertion of Desktop to Tactical => SDK API Framework**	**Supports Evolution Path to Digital Video => MPEG-4 and HD**	**Enables NDI Path to Protecting Advanced IP => Enables COTS Security**

Supports Hybrid Software Modularity - Opens new Legacy to Next Generation partitioning

Transformational Intel Based Technology:
Multicore Intel + Hypervisor for Multiple OS Environments +
Publish/Subscribe Application Interface + Hybrid GUI with High
Resolution Networked Video

Conclusions

- Legacy systems have the challenge of being developed with 3-4 generations of HW and SW technology without a clean slate opportunity
- Transition to IMA capabilities can happen incrementally using an adjunct approach to establish a system gateway
- Legacy systems should have a forward plan/staged proof of concept focus for transformational adjunct processing that enables software transformation while also supporting currently deployed systems
- Emergence of embedded processing and IoT will accelerate capabilities of adjunct processing capabilities
- Architecture analysis and prototyping is critical to finding the most affordable and supportable insertion of IMA like capability in deployed systems

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