Ultradense Silicon Photonic Interface for Optical Interconnection

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***Abstract*— A scalable ultradense silicon photonic interface with 61 compact vertical grating couplers on a pitch of 42.3 μm is designed and fabricated to match a pitch reducing optical fiber array (PROFA) hexagonal channel pattern. Experimental results show that the designed grating couplers with a minimum insertion loss of 4.5 dB and a 3-dB bandwidth of 50 nm are obtained. The crosstalk between different channels is less than −50 dB and the maximum loss difference across the PROFA interface is ∼0.7 dB. High-speed data transmission indicates that a bandwidth density as large as 27 Tb/s/mm^2 could be achieved within a footprint of 0.096 mm^2, demonstrating the potential of silicon photonics for broadband optical interconnection.**

***Index Terms*— Multicore fiber array, bandwidth density, vertical grating couplers, silicon photonics, photonic integrated circuits (PICs), optical interconnection.**

I. INTRODUCTION

SILICON photonics has become one of the leading technologies in photonic integration leveraging cost-efficient complementary metal-oxide-semiconductor (CMOS) fabrication [1]. A wide variety of electro-optical and optical devices including modulators, photodetectors, switches, and filters have been implemented using a silicon-on-insulator (SOI) platform targeting applications requiring high-bandwidth optical transceivers such as high-performance computing (HPC), optical telecommunications and data communications, and potentially on-chip optical interconnections [2], [3]. A large number of optical inputs/outputs (I/Os) is required to connect diverse components through the optical interface. Efforts have been made to increase the channel count at the optical interface through both in-plane edge coupling and vertical out-of-plane surface coupling between optical fibers and on-chip photonic waveguides [4]–[7]. For example, three-dimensional (3-D) adiabatically taper structures are used to transform the mode size of sub-micron nanophotonic waveguides to that of a 10-μm standard single-mode fiber (SMF) [8]. A multichannel tapered coupler enabling the efficient coupling between an array of SMFs to an array of Si waveguides with spot-size converters on a 20-μm pitch has been reported in [5]. Despite good coupling efficiency and wide bandwidth, the scalability of the channel count is limited by the one-dimensional chip edge. The two-dimensional channel arrangement is utilized in out-of-plane surface coupling, where vertical grating couplers (VGCs) are incorporated to Si waveguides to match the optical mode of standard SMF [9], [10]. Furthermore, high channel density plays a significant role in saving chip real estate and reducing the propagation loss of routing waveguides. Currently, typical channel spacing of VGCs is 125 μm for standard fiber arrays, limiting further channel density increase at the interface of silicon photonic integrated circuits (PICs). A pitch reducing optical fiber array (PROFA) has been developed by Chiral Photonics with a reduced pitch ranging from 35 μm–50 μm, while maintaining the original mode field diameter (MFD) and numerical aperture (NA) of standard SMF [11]. A 37-channel two-dimensional optical interface using high-efficient grating couplers was demonstrated with a 40-μm pitch PROFA [7], [12].

In this letter, we demonstrate an optical I/O bandwidth density of 27 Tb/s/mm^2 using a dense silicon photonic interface with a hexagonal array of 61 VGCs on a 42.3 μm pitch matching a two-dimensional PROFA. The interface was fabricated through IMEC's standard multi-project wafer fabrication run. The structure, design and fabrication of the PROFA interface are discussed based on the simulation results and application rules. The performance of the VGCs along with interconnected devices is assessed experimentally with the 61-channel PROFA. High-speed data transmission is performed to investigate the bandwidth density (Tb/s/mm^2). The PROFA-VGC array interface is scalable towards higher channel count for increased density and I/O throughput.

II. DESIGN AND FABRICATION

The silicon photonic interface is designed to match the given PROFA, maintaining the same MFD and NA of standard SMF with a pitch of 42.3 μm. The pitch is selected so that every three grating couplers can also be tested with a standard fiber array. As shown in Fig. 1(a), compact focusing VGCs reported in [13] are used as the basic building block element of the optical I/Os. The structure parameters of VGCs, including

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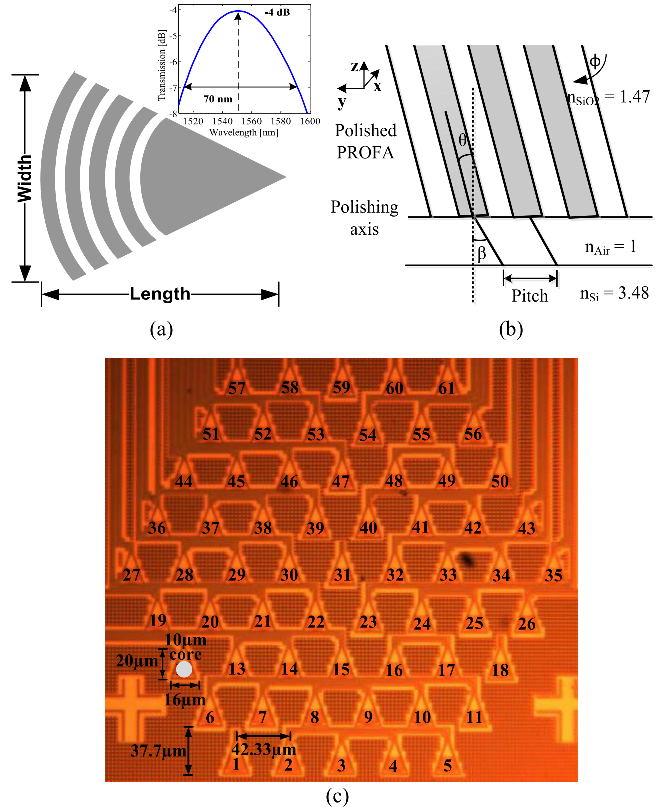
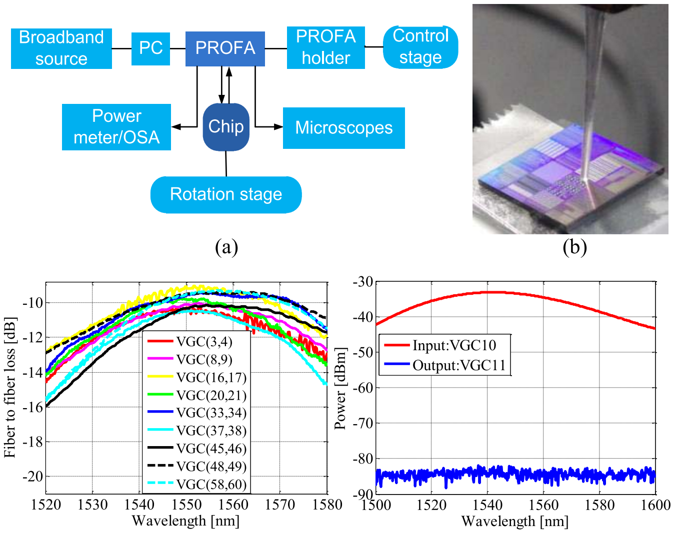


(a) (b)

(c)

Fig. 1. (a) Vertical grating coupler (VGC) layout. (inset: the simulated transmission of grating coupler). (b) Side view of PROFA interface to the VGCs with relevant angles and effective indices. (c) Image of the two-dimensional PROFA interface with 61 numbered VGCs with indicated horizontal and vertical pitch of 42.33 μm and 37.7 μm, respectively.

the incident angle, the pitch and duty cycle, are determined with the aid of finite-difference time-domain (FDTD) simulation (by Lumerical Solutions, Inc.) to satisfy the requirement for compact grating size, which tends to have larger insertion loss. Further, too small a pitch between VGCs makes them sensitive to crosstalk between neighboring channels. The inset of Fig. 1(a) is the simulation results of the transmission spectrum for the designed grating coupler clad by air for fabrication through IMEC passive silicon photonic IC technology (SOI with 220 nm Si). With an incident angle (β) of 20° to the normal for the PROFA, the simulated transmission spectrum shows a peak centered at 1550 nm with an insertion loss of 4.0 dB, and a 3-dB bandwidth of 70 nm. According to the simulation results for optimized VGCs with properly designed dimensions, 61 such VGCs are arranged to match the 61-channel PROFA in a hexagonal array. The side view of the interface between the PROFA and VGC array is shown in Fig. 1(b). The PROFA was polished at 13° (θ) based on Snell's law. Considering the stretching effect of two-dimensional channel pattern along the polishing axis θ, and the potential rotation with respect to the polishing axis, Φ, the spacing between VGCs along the two axes (x,y) should be designed to match the exact two-dimensional channel pattern of the PROFA [14]. In our design, (θ, Φ) equal to (13°, 0°) and the horizontal and vertical channel pitches are 42.3 μm and 37.7 μm, respectively.



(a) (b)

(c) (d)

Fig. 2. (a) Schematic of experimental setup, (b) graph of PROFA tip aligned to PIC, (c) the transmission of designed grating coupler, (d) the crosstalk between two unconnected adjacent channels.

The PROFA interface of 61 VGCs and routing waveguides are fabricated within a 0.2 mm^2 (500 μm × 400 μm) die. The image of the fabricated PROFA interface is presented in Fig. 1(c) with labeled channels. In the design, some of the VGCs are directly connected with each other. Not shown in the figure are other VGCs interconnected through routing devices such as delay lines (*e.g.*, VGC(27,30)), ring resonators and multi-channel ring resonator based Multiplexer/Demultiplexer (Mux/Demux) (*e.g.*, VGC(46,47) and VGC(45,46,47)). There are also 10 variations in the dimensions of the VGCs with width ranging from 15 to 20 μm, and length from 20 to 35 μm to investigate the effect of the grating size reduction on the insertion loss, bandwidth and peak wavelengths.

III. DEVICE PERFORMANCE AND DISCUSSION

A. Performance of the Ultra-Dense Si Photonic Interface

The performance of the VGC-based PROFA interface is characterized with a PROFA polished at 13°. This PROFA has 1.2 μm average channel positioning error over all 61 channels relative to an ideal hexagonal grid. The experimental setup is illustrated in Fig. 2(a). The broadband source is a wideband erbium doped fiber amplifier (EDFA). A polarization controller (PC) is used at the input of the VGCs, which support the transverse electric (TE) mode. A rotation stage is necessary to align the chip in the polishing axis of the PROFA, in the (x,y) plane. All 61 PROFA channels are simultaneously and actively aligned to the corresponding VGCs on the chip, as shown in Fig. 2(b). The input light is coupled to the chip through the VGC and the output is extracted from the connected VGC. The fiber-to-fiber transmission results of seven different interconnected VGC pairs across the entire PROFA interface is shown in Fig 2(c) with a wavelength peak centered around 1550 nm as designed. Note that the PROFA can be attached to the silicon photonic interface with an index-matching adhesive. The polished angle or grating structure parameters should be adjusted to maintain the peak wavelength due to the refractive index change of the cladding.

TABLE I

LOSS MEASUREMENTS OF 10 VARIATIONS IN VGC DIMENSIONS

Width [μm]	15	16	16	16	18	18	18	20	20	20
Length[μm]	20	20	25	30	20	25	30	25	30	35
Loss [dB]	5.0	**4.5**	**4.5**	4.6	4.7	4.6	**4.5**	4.6	**4.5**	**4.5**

TABLE II

OPTIMUM PERFORMANCE PARAMETERS OF 16 μm × 20 μm VGC

Insertion loss [dB]	**3-dB bandwidth [nm]**	**Loss difference [dB]**	**Crosstalk [dB]**
4.5	50	0.7	-50

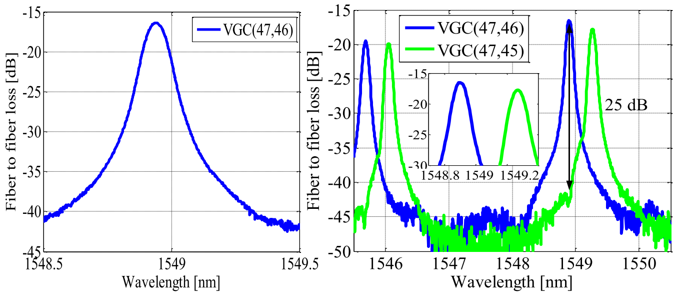
The best insertion loss of the fabricated VGCs from fiber to fiber is approximately 9.0 dB corresponding to 4.5 dB per grating coupler. The 0.5 dB loss difference from theory is mainly due to imperfect alignment of the PROFA and chip. Better insertion loss can be obtained via VGC optimization [7], [12]. The maximum loss difference between different VGCs is 0.7 dB with an average loss of 4.8 dB and a standard deviation of 0.4 dB over 18 VGCs. The variation depends on the alignment as well as the positioning error of the PROFA channels from its fabrication. The measured 3-dB bandwidth is about 50 nm, narrower by 20 nm from simulation, potentially due to the gap or tilt between the PROFA and chip [15]. Crosstalk of less than −50 dB can be seen in Fig. 2(d) at 1550 nm. The output spectrum of channel VGC11 is measured, while the broadband optical source is connected to the adjacent channel VGC10.

The measured loss of 10 VGCs with different widths and lengths are presented in Table I. One VGC variation with dimensions of 15 μm × 20 μm shows an insertion loss of 5.0 dB. While the characterizations of the other nine variations in the dimensions exhibit almost no performance penalty as long as the grating size is greater than the core size of the 10-μm SMF (represented by the white reference dot on Fig. 1(c)). Hence, the potential grating length and width are required to be larger than 20 μm and 16 μm, respectively. The alignment requirement between the PROFA and chip becomes stricter, and the tolerance of positioning error of PROFA channels and VGCs is reduced with smaller dimensions [16].

Table II presents key performance parameters for optimum dimensions of 16 μm × 20 μm.

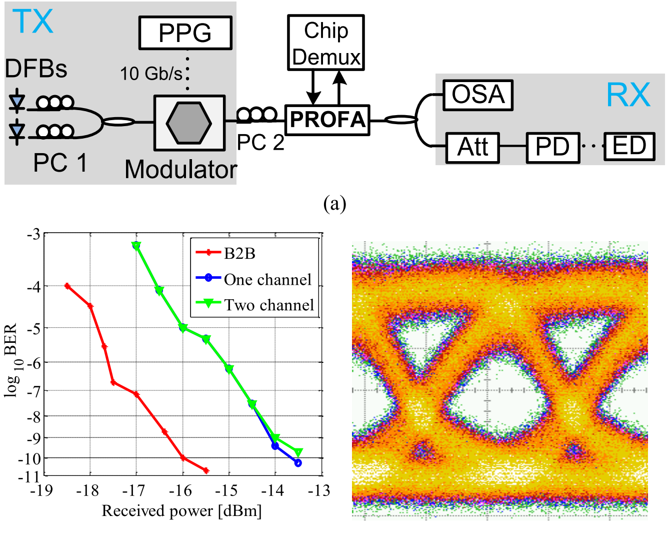
B. Towards Ultra-Dense Photonic Interconnection

The performance of the devices interconnected through the designed VGCs of the silicon photonics PROFA interface is measured with the setup illustrated in Fig. 2(a). A ring resonator (RR) and a channel multiplexer based on the IMEC process development kit (PDK) were designed with their respective transmission spectrum shown in Fig. 3. In Fig. 3(a), the coupling efficiency of the ring resonator from the drop port is approximately −6 dB taking into account a 10 dB loss from the optical I/Os. The channel isolation is 25 dB. The 3-dB bandwidth is 0.1 nm limiting the data rate to 10 Gb/s. The high insertion loss and narrow bandwidth are likely caused by fabrication variation on the gap (0.22 μm) between the waveguide and ring. Through a more optimized design, insertion loss has been shown to be as low as 1 dB [17].



(a) (b)

Fig. 3. Spectrum of (a) ring resonator and (b) RR-based (de)multiplexer.

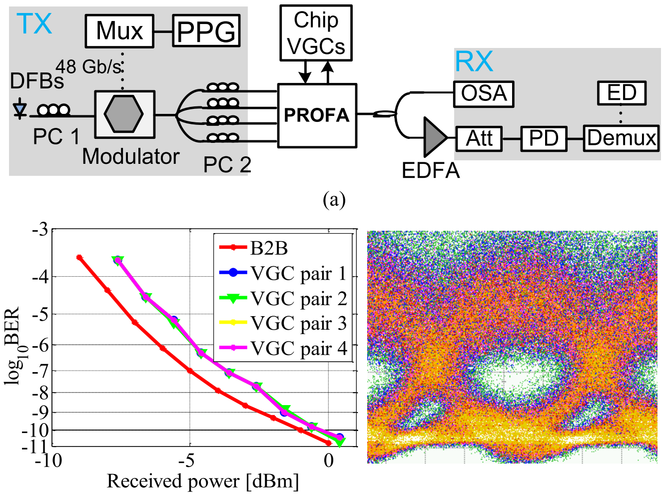


(a)

(b) (c)

Fig. 4. (a) Experimental setup for data transmission through the (de)multiplexer (Att: attenuator), (b) BER measurement as a function of received power for back-to-back, one-channel and two-channel data transmission and (c) 10 Gb/s optical eye diagram at BER of 10^{-9}.

A 3-channel ring-based (de)multiplexer is designed based on the above ring resonator with 0.32-nm channel spacing (Fig. 3(b)). Only two channels are shown as the third channel has a large insertion loss also potentially due to fabrication variation that may have affected the critical parameters such as waveguide width. The center wavelengths of the two working channels are 1548.90 nm and 1549.22 nm, respectively. Fig. 4(a) illustrates the experimental setup with two distributed-feedback (DFB) lasers in the transmitter (TX). The DFBs are externally modulated at 10 Gb/s (non-return-to-zero, NRZ) with a pseudo-random bit sequence (PRBS, $2^{31} - 1$ bits) generated by a pulse pattern generator (PPG). In the receiver (RX), the optical spectrum is measured by an optical spectrum analyzer (OSA) with resolution of 0.1 nm and sensitivity of −85 dBm. The bit error rate (BER) performance is measured by the error detector (ED). The measured BER as a function of the received optical power at the photodetector (PD) is shown in Fig. 4(b) for back-to-back, one-channel and two-channel data transmission. Compared to back-to-back measurements, there is about 2 dB power penalty for the (de)multiplexer mainly caused by the narrow bandwidth of the ring resonator (0.1 nm) filtering part of spectral content of the modulated signal. The signal distortion can be noted



(a)

(b) (c)

Fig. 5. (a) Experimental setup of high-speed data transmission, (b) the BER as a function of received power for back-to-back, VGC pairs data transmission and (c) the corresponding eye diagram at BER of 10^{-9} .

in the eye diagram shown in Fig. 4(c). Ring-based structures will certainly limit the achievable bandwidth density and broadband structures should be considered to fully exploit the dense interface.

A higher-speed data transmission at 48 Gb/s was performed on four adjacent connected VGC pairs within an area of 7200 μm^2. As the experimental setup shows in Fig. 5(a), the modulator is driven by a 4:1 MUX clocked by a signal generator at 48 Gb/s. The modulated signal is optically broadcast to four optical signals and propagated through four different PROFA channels. A low-noise-figure EDFA is used to amplify the signals before the PD. Fig. 5(b) shows the BER as a function of the received power for back-to-back and four VGC pair data transmission. Nearly the same BER performance can be seen for the four VGC pairs. The eye diagram with the BER below 10^{-9} is depicted in Fig. 5(c) with noise originating from the EDFA boosting the signal to the photodetector with the sensitivity of -7 dBm at 40 Gb/s. The power penalty is 0.5 dB at a BER of 10^{-9} and increases to 1.5 dB at a BER of 10^{-4}.

The channel aggregate bandwidth is 192 Gb/s within a surface chip area of 7200 μm^2, which corresponds to an on-chip bandwidth density of approximately 27 Tb/s/mm^2 for the designed PROFA interface. We can scale those results to a total capacity for the ultra-dense interface of 1.44 Tb/s using all 61 channels within a footprint of 0.096 mm^2. Larger capacity can simply be achieved through expanding the number of wavelength-division multiplexed (WDM) channels per I/O.

IV. CONCLUSIONS

In this letter, an ultra-dense silicon photonic interface with 61 vertical grating couplers (VGCs) has been designed and fabricated at IMEC-ePIXfab to interface with a pitch reducing optical fiber array (PROFA). The performance of the VGC and interconnected devices are characterized experimentally. A minimum insertion loss of 4.5 dB and a 3-dB bandwidth of 50 nm for the VGCs are achieved without additional etching and processing steps in the fabrication. The crosstalk between channels is also as low as -50 dB with a maximum loss variation across the PROFA interface of approximately 0.7 dB. Four channels modulated at 48 Gb/s were successfully propagated through four connected VGC pairs occupying 7200 μm^2 of surface chip area, demonstrating an extremely high bandwidth density of 27 Tb/s/mm^2. The dense PROFA interface enables scalability with higher channel count for increased throughput.

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REFERENCES

[1] R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.

[2] B. Jalali and S. Fathpour, "Silicon photonics," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4600–4615, Dec. 2006.

[3] A. E.-J. Lim *et al.*, "Review of silicon photonics foundry efforts," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 4, Jul./Aug. 2014, Art. ID 8300112.

[4] B. G. Lee *et al.*, "20-μm-pitch eight-channel monolithic fiber array coupling 160 Gb/s/channel to silicon nanophotonic chip," in *Proc. Opt. Fiber Commun. (OFC) Conf.*, Mar. 2010, pp. 1–3, paper PDPA4.

[5] F. E. Doany *et al.*, "Multichannel high-bandwidth coupling of ultradense silicon photonic waveguide array to standard-pitch fiber array," *J. Lightw. Technol.*, vol. 29, no. 4, pp. 475–482, Feb. 15, 2011.

[6] V. I. Kopp *et al.*, "Two-dimensional, 37-channel, high-bandwidth ultra-dense silicon photonics optical interface," in *Proc. Opt. Fiber Commun. (OFC) Conf.*, Mar. 2014, pp. 1–3, paper Th5C.4.

[7] V. Kopp *et al.*, "Two-dimensional, 37-channel, high-bandwidth, ultra-dense silicon photonics optical interface," *J. Lightw. Technol.*, to be published.

[8] D. Vermeulen *et al.*, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform," *Opt. Exp.*, vol. 18, no. 17, pp. 18278–18283, 2010.

[9] A. Sure, T. Dillon, J. Murakowski, C. Lin, D. Pustai, and D. W. Prather, "Fabrication and characterization of three-dimensional silicon tapers," *Opt. Exp.*, vol. 11, no. 26, pp. 3555–3561, 2003.

[10] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–68, Mar./Apr. 2006.

[11] V. I. Kopp, J. Park, M. Wlodawski, J. Singer, D. Neugroschl, and A. Z. Genack, "Pitch reducing optical fiber array for dense optical interconnect," in *Proc. IEEE Avionics, Fiber-Opt. Photon. Technol. Conf. (AVFOP)*, Sep. 2012, pp. 48–49.

[12] D. Taillaert *et al.*, "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers," *IEEE J. Quantum Electron.*, vol. 38, no. 7, pp. 949–955, Jul. 2002.

[13] F. Van Laere *et al.*, "Compact focusing grating couplers for silicon-on-insulator integrated circuits," *IEEE Photon. Technol. Lett.*, vol. 19, no. 23, pp. 1919–1921, Dec. 1, 2007.

[14] *Optical Coupling & Design Guide*, Chiral Photonics, Inc., Pine Brook, NJ, USA, Apr. 2014, pp. 10–11.

[15] Z. Xiao, T.-Y. Liow, J. Zhang, P. Shum, and F. Luan, "Bandwidth analysis of waveguide grating coupler," *Opt. Exp.*, vol. 21, no. 5, pp. 5688–5700, 2013.

[16] D. Taillaert *et al.*, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," *Jpn. J. Appl. Phys.*, vol. 45, no. 8A, pp. 6071–6077, 2006.

[17] X. Zheng *et al.*, "A tunable 1 × 4 silicon CMOS photonic wavelength multiplexer/demultiplexer for dense optical interconnects," *Opt. Exp.*, vol. 18, no. 5, pp. 5151–5160, 2010.