High-Efficiency Low-Crosstalk 1310-nm Polarization Splitter and Rotator

Hang Guan, Ari Novack, Matthew Streshinsky, Ruizhi Shi, Yang Liu, Qing Fang, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg

***Abstract*— We demonstrate the first example of a polarization splitter and rotator (PSR) at 1310 nm built on a silicon-on-insulator platform using 248-nm deep-ultraviolet lithography. The PSR is constructed with a directional coupler, a bilevel taper-based TM0-to-TE1 mode converter, and an asymmetric Mach–Zehnder-based TE1-to-TE0 mode converter. A worst-case TM0-to-TE0 mode-conversion loss of 2 dB, with polarization crosstalk lower than −20 dB over a wide bandwidth of 40 nm is experimentally demonstrated. The worst-case polarization-dependent loss is 0.76 dB.**

***Index Terms*— Integrated optics, polarization splitter and rotator, silicon-on-insulator (SoI).**

I. Introduction

SILICON-ON-INSULATOR (SOI) photonic integrated platform is very promising due to its compatibility with current complementary metal-oxide-semiconductor (CMOS) fabrication techniques [1]. However, it also suffers from large polarization dependence, which is a major challenge for its practical use [2]. During the past few years, there has been growing attention paid to polarization diversity circuits, which could be used to achieve polarization independence [3], [4]. There are mainly two methods at the chip interface that can be adopted to solve this problem. One way is to use a polarization splitter grating coupler (PSGC) [5], [6]. Another way is to use a polarization insensitive edge coupler combined with a polarization splitter and rotator (PSR). On-chip PSRs demonstrated or proposed in the last few years fall into three general categories [7]. The first method is to use waveguides with asymmetric cross-sections, which can cause scattering at the abrupt interface to achieve mode conversion [8], [9]. Mode evolution is another method that has been adopted, in which a higher-order mode is used as a transition between the fundamental transverse electric (TE0) mode and the fundamental transverse magnetic (TM0) mode [10], [12]. The third rotation method is to use non-silicon-based materials [13]–[15].

In terms of realized devices that do not require an additional material such as nitride, one of the lowest loss demonstrations has been that of Y. Ding *et al*. [2], which achieved low insertion loss (<2.5 dB) and a low polarization crosstalk (<12 dB) in the wavelength region 1480–1580 nm. However, this device is fabricated using electron-beam lithography with air as cladding. The lack of a top-cladding layer makes these devices incompatible with most metal back-end-of-line (BEOL) processes. Another interesting result is that of Aamer et al [9], in which losses better than 2.5 dB are shown from 1545–1575 nm using 193-nm optical lithography. In this case, a top cladding layer was utilized. To our knowledge, however, there has yet to be any demonstration of polarization rotation in the important 1310-nm regime.

In this letter we present a PSR built on a 220-nm SOI platform using 248-nm deep-ultraviolet (DUV) lithography. The PSR is designed for 1310-nm data communication with silica as cladding. Despite the coarser photolithographic process used as compared to [9], losses of 2 dB or better are shown across a 40-nm bandwidth near 1310 nm. With a low polarization crosstalk of 20 dB and small device footprint of $8 \times 56\ \mu\text{m}^2$ we expect that our design will be a practical component in silicon photonic circuits near 1310 nm.

II. Principle and Simulation

The PSR is constructed with a directional coupler, a TM0-to-the-first-order-TE-mode (TM0-to-TE1) converter, and a Mach-Zehnder-based TE1-to-TE0 mode converter. The use of a symmetric directional coupler as a polarization beam splitter (PBS) has been described in [4], [16]. The bi-level taper as a TM0-to-TE1 mode converter is detailed in [17]. The use of an asymmetric Mach-Zehnder as a TE1-to-TE0 mode converter has been described in [18]. Although above building blocks have already been demonstrated individually, their combination is novel. The key idea comes from the fact that the TE1 mode comprises two TE0-mode-like portions with π phase difference. By introducing an asymmetric Mach-Zehnder, we can then phase-align and combine the two TE0-mode-like portions into one TE0 output.

Manuscript received December 1, 2013; revised February 24, 2014; accepted March 4, 2014. Date of publication March 11, 2014; date of current version April 10, 2014. This work was supported in part by Gernot Pomrenke, in part by the Air Force Office of Scientific Research through OPSIS under Grant FA9550-10-l-0439, and in part by PECASE under Grant FA9550-13-1-0027.

H. Guan, A. Novack, M. Streshinsky, and R. Shi are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119077 (e-mail: hang.guan@nus.edu.sg; arinovack@nus.edu.sg; mstreshinsky@nus.edu.sg; ruizhi.shi@nus.edu.sg).

Y. Liu and T. Baehr-Jones are with the Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716 USA (e-mail: phyliuyang@gmail.com; baehrjt@udel.edu).

Q. Fang, A. E.-J. Lim, and G.-Q. Lo are with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685 (e-mail: fangq@ime.a-star.edu.sg; limej@ime.a-star.edu.sg; logq@ime.a-star.edu.sg).

M. Hochberg is with the Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716 USA, and also with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119077 (e-mail: michael.hochberg@gmail.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LPT.2014.2310635

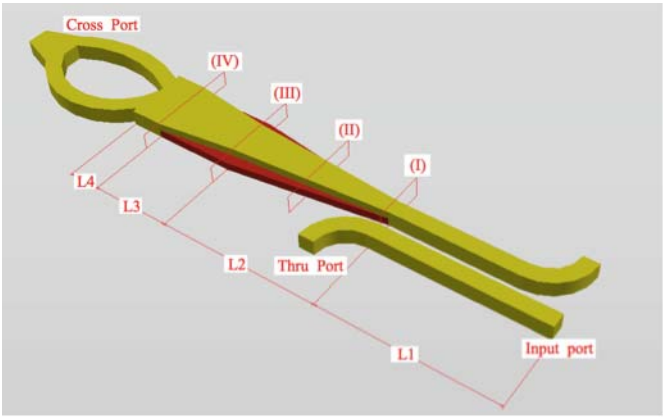


Fig. 1. Schematic structure of the proposed PSR.

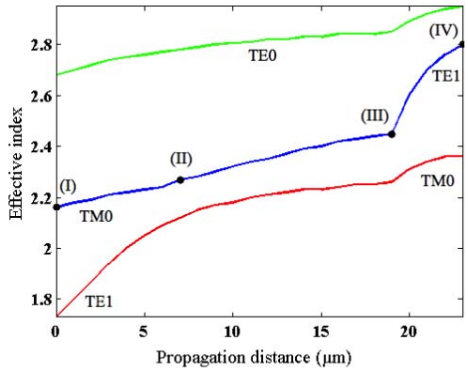


Fig. 2. Mode index evolution along the PR structure.

The proposed PSR is schematically depicted in Fig. 1. Both the TE0 and TM0 modes are sent into the input of the left waveguide on the bottom right corner of the figure. In the case of TE0 input, the light will go through the left-side waveguide to the thru-port directly. In case of TM0 input, the light will be coupled to the right side and gradually converted to the TE1 mode when traveling through the adiabatic bi-level taper. The TE1 mode will then be split into two TE0 mode beams. An extra phase difference of π is introduced between the two beams by the asymmetric Mach-Zehnder. In the end, the two beams will be phase-aligned and can be converted into the TE0 mode with minimal interference loss.

In this letter, we use a SOI wafer with a silicon thickness of H1 = 220 nm (colored in yellow in Fig. 1) and partially etched waveguide thickness H2 = 90 nm (colored in red in Fig. 1). The directional coupler uses two identical silicon nanowires, whose width is chosen as W1 = 400 nm and L1 = 15 μm. The gap spacing between the two nanowires is set to be W2 = 220 nm. Since there is a bend at the beginning of the right-side waveguide, the actual coupling length is L_C = 10 μm. After the directional coupler, a bi-level taper is used to convert the TM0 mode into the TE1 mode. Since a SOI double-rib waveguide is not symmetrical in the vertical direction, mode hybridization may occur. The bi-level taper consists of two sections. The length of the first section is L2 = 19 μm. In this section, the ridge waveguide width converts from W1 = 400 nm to W2 = 620 nm, while the double-etched waveguide width converts from W1 = 400 nm

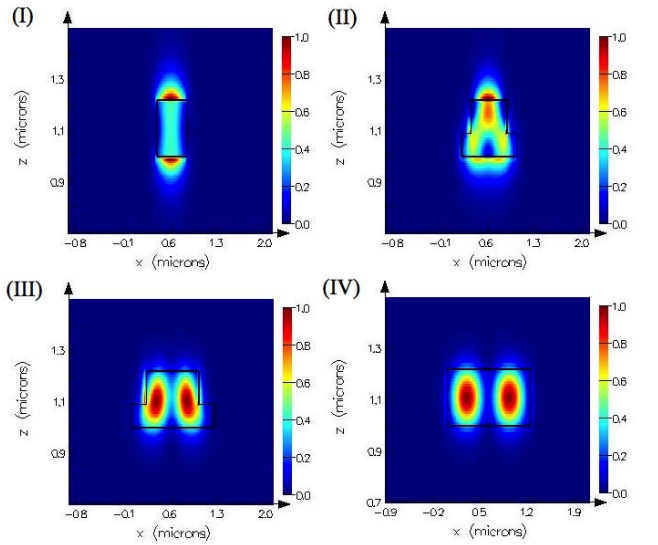


Fig. 3. Total electric-field amplitude (|E|) changes as the input TM0 field travels through the bi-level taper. The above four subplots show the mode profiles at corresponding sections in Fig. 1.

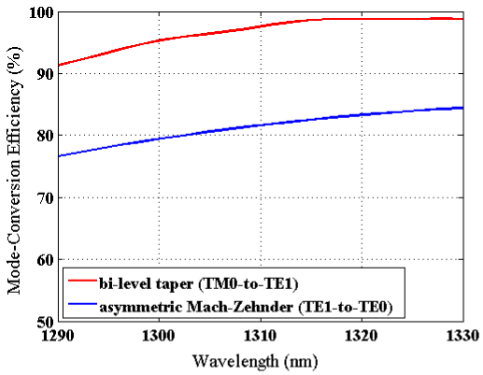
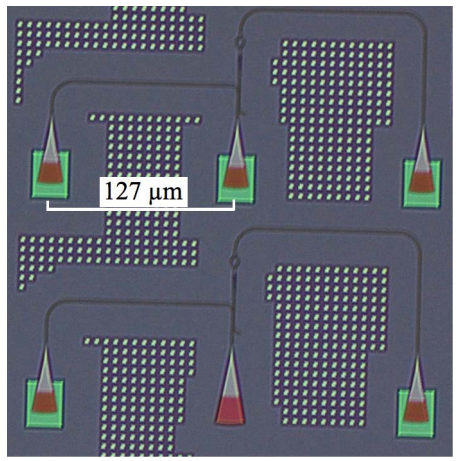


Fig. 4. Simulated mode-conversion efficiencies of the bi-level taper and asymmetric Mach-Zehnder.

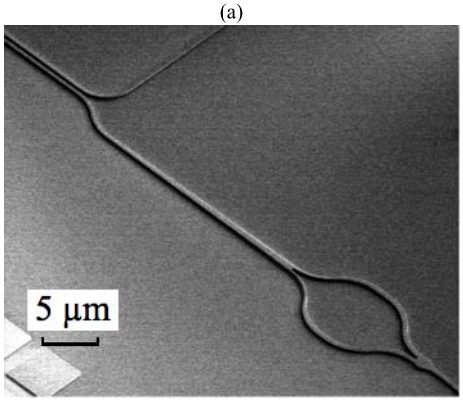
to W3 = 1.22 μm. The length of the second section is L3 = 4 μm. In this section, the ridge waveguide width converts to W3 = 1.22 μm.

Fig. 2 illustrates an example of the mode evolution along the bi-level taper. As shown in Fig. 2, the effective indices of the TM0 mode and the TE1 mode are very close to each other between point (II) and point (III), which causes strong mode hybridization and conversion. Thus, the original TM0 mode (I) entering into the taper will become the final TE1 mode (IV), which is illustrated by the change of electric-field distribution shown in Fig. 3.

In order to understand the loss contributions of each part of the overall PSR system, three-dimensional finite-difference time-domain simulations were performed in the wavelength region 1290–1330 nm on each constituent component. Based on the simulation, the PBS has an insertion loss of 0.44 dB at 1310 nm when launching the TE0 mode. In case of the TM0 mode as input, the PBS has an insertion loss of 0.08 dB. As shown in Fig. 4, the bi-level taper has a TM0-to-TE1 mode-conversion loss of 0.13 dB at 1310 nm, and the worst-case mode-conversion efficiency is better than 0.36 dB.



(a)



(b)

Fig. 5. (a) Optical micrograph of two fabricated calibration structures, with PSRs designed to be identical. (b) Scanning electron microscope picture of fabricated PSR.

The Mach-Zehnder has a TE1-to-TE0 mode-conversion efficiency of 0.86 dB at 1310 nm, and the mode-conversion efficiency is larger than 1.13 dB in the aforementioned wavelength region. Overall, then, the TE0 input is predicted to experience a 0.44 dB loss, while the TM0 input experiences a worst-case loss of 1.57 dB. As indicated later in Fig. 7(a), this is in close agreement with our experiment results.

III. Fabrication and Experiment Results

A. Device Fabrication

The device was fabricated on an 8-inch SOI wafer, with 220-nm top silicon film and a 2-μm buried oxide (BOX) layer. Three masks were used to pattern the wafer using 248-nm DUV lithography. The first mask defined the 220 nm silicon height used for waveguides. The second mask was used to define a 160 nm silicon layer that was used to build the grating couplers. The final mask defined the 90 nm layer used in the rib of the PSR. Unpatterned areas were fully etched to the BOX and an oxide layer was deposited.

B. Device Characterization

Devices were measured on a wafer-scale optical test setup. Light from a tunable laser was coupled into the device under test by aligning a fiber-array containing a pair of polarization-maintaining fiber to a set of input- and output-grating couplers.

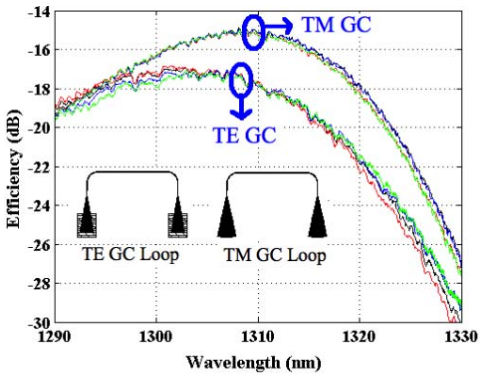


Fig. 6. Spectral responses of the TE and TM SPGC loops. The spectra of four loops of each coupler type was averaged and used to extract the PSR loss.

The TE grating coupler and TM grating coupler that were used in the testing were periodic single-polarization grating couplers (SPGCs). Periodicities of the TE and TM SPGCs are 0.5 μm and 0.68 μm respectively. The phase-matching condition for both the grating couplers could be achieved using 17° fiber angle [19].

To calibrate the loss and crosstalk of the PSR for the TM-input and the TE-input, two calibration structures are needed. Both structures have three ports and use the center port as the input as seen in Fig. 5(a). The top structure measures the response of the PSR to the TE-input, while the bottom structure measures the response of the PSR to the TM-input. It should be noted that while the grating couplers changed between the two structures, the PSRs embedded in the two structures were designed to be identical. While the two PSRs have some differences due to process variations, statistical data show that this variation is acceptable.

C. Device Performance

Fig. 6 shows the spectral response of four TE grating coupler loops and four TM grating coupler loops. The spectral response of four grating couplers was averaged and then used to separate the grating coupler loss from the PSR loss. As shown in Fig. 6, the TM grating coupler has an average coupling loss of 7.6±0.05 dB at 1310 nm, while the TE grating coupler has an average coupling loss of 8.9 ± 0.05 dB at 1310 nm. The small variation in grating coupler loss shows that they can be accurately separated to find the PSR loss.

As shown in Fig. 7, the PSR shows a 2 dB worst-case TM0-to-TE0 polarization-conversion loss. Meanwhile, when launching the TE0 mode, the insertion loss is around 0.5 dB. Another key metric is the degree of crosstalk, that is, the amount of TE0 input light coupled into the TE0 mode at the TM output-port (a mode/port location which should be solely due to the TM0 input). In this and the corresponding TM0-input cases, we measure these values to be better than 20 dB as shown in Fig. 7(b). We note that our measurement approach effectively filters out any power that could be in the TM0 modes of the output waveguide. Whatever unmeasured power might be scattered into these waveguides should not be a concern, since there are many ways of discarding the TM0 mode, like cascading a directional coupler behind [15], [20].

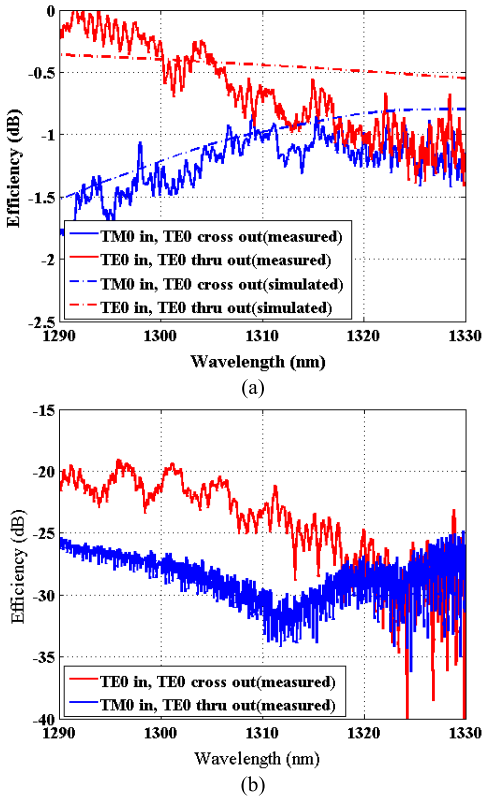


Fig. 7. Measured and simulated spectra of the PSR with input and output grating loss normalized showing (a) conversion loss and (b) crosstalk.

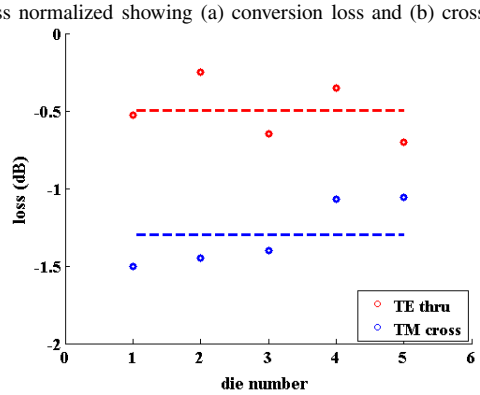


Fig. 8. Measured TE thru output losses and TM cross output losses in five dies.

The PSR performance across five dies is shown in Fig. 8, with the TE mode input having a loss of 0.5 ± 0.2 dB and the TM mode input having a loss of 1.26 ± 0.2 dB at 1310 nm.

IV. Conclusion

We have presented a PSR built on the SOI platform at 1310 nm. A low TM-to-TE conversion loss of better than 2 dB with a minimum insertion loss of 1 dB is demonstrated. Polarization crosstalk was measured to be lower than 20 dB over a wide bandwidth of 40 nm.

References

[1] T. Baehr-Jones, T. Pinguet, P. G.-Q. Lo, S. Danziger, D. Prather, and M. Hochberg, "Myths and rumours of silicon photonics," *Nature Photon.*, vol. 6, pp. 206–208, Mar. 2012.

[2] Y. Ding, H. Ou, and C. Peucheret, "Wideband polarization splitter and rotator with large fabrication tolerance and simple fabrication process," *Opt. Lett.*, vol. 38, no. 8, pp. 1227–1229, 2013.

[3] T. Barwicz *et al.*, "Polarization transparent microphotonic devices in the strong confinement limit," *Nature Photon.*, vol. 1, pp. 57–60, Dec. 2007.

[4] H. Fukuda, K. Yamada, T. Tsuchizawa, T. Watanabe, H. Shinojima, and S. I. Itabashi, "Silicon photonic circuit with polarization diversity," *Opt. Express*, vol. 16, no. 7, pp. 4872–4880, Mar. 2008.

[5] D. Taillaert, H. Chong, P. Borel, L. Frandsen, R. De La Rue, and R. Baets, "A compact two-dimensional grating coupler used as a polarization splitter," *IEEE Photon. Technol. Lett.*, vol. 15, no. 9, pp. 1249–1251, Sep. 2003.

[6] M. Streshinsky *et al.*, "A compact bi-wavelength polarization splitting grating coupler fabricated in a 220 nm SOI platform," *Opt. Express*, vol. 21, no. 25, pp. 31019–31028, Dec. 2013.

[7] X. Xiong, C.-L. Zou, X.-F. Ren, and G.-C. Guo, "Integrated polarization rotator/converter by stimulated Raman adiabatic passage," *Opt. Express*, vol. 21, no. 14, pp. 17097–17107, Jul. 2013.

[8] Y. Wakabayashi, T. Hashimoto, J. Yamauchi, and H. Nakano, "Short waveguide polarization converter operating over a wide wavelength range," *J. Lightw. Technol.*, vol. 31, no. 10, pp. 1544–1550, May 15, 2013.

[9] M. Aamer *et al.*, "CMOS compatible silicon-on-insulator polarization rotator based on symmetry breaking of the waveguide cross section," *IEEE Photon. Technol. Lett.*, vol. 24, no. 22, pp. 2031–2034, Nov. 15, 2012.

[10] J. Wang and D. Dai, "Ultra-small silicon polarization beam splitter based on cascaded asymmetry directional couplers," in *Proc. Conf. Opt. Fiber Commun.*, Mar. 2013, pp. 1–3, paper OTh4I.1.

[11] D. Dai and J. E. Bowers, "Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires," *Opt. Express*, vol. 19, no. 11, pp. 10940–10949, May 2011.

[12] W. Yuan *et al.*, "Mode-evolution-based polarization rotator-splitter design via simple fabrication process," *Opt. Express*, vol. 20, no. 9, pp. 10163–10169, Apr. 2012.

[13] M. Komatsu, K. Saitoh, and M. Koshiba, "Compact polarization rotator based on surface plasmon polariton with low insertion loss," *IEEE Photon. J.*, vol. 4, no. 3, pp. 707–714, Jun. 2012.

[14] J. N. Caspers, M. Z. Alam, and M. Mojahedi, "Compact hybrid plasmonic polarization rotator," *Opt. Lett.*, vol. 37, no. 22, pp. 4615–4617, 2012.

[15] L. Chen, C. R. Doerr, and Y. K. Chen, "Compact polarization rotator on silicon for polarization-diversified circuits," *Opt. Lett.*, vol. 36, no. 4, pp. 469–471, 2011.

[16] H. Fukuda, K. Yamada, T. Tsuchizawa, T. Watanabe, H. Shinojima, and S. I. Itabashi, "Ultrasmall polarization splitter based on silicon wire waveguides," *Opt. Express*, vol. 14, no. 25, pp. 12401–12408, Dec. 2006.

[17] D. Dai, Y. Tang, and J. E. Bowers, "Mode conversion in tapered submicron silicon ridge optical waveguides," *Opt. Express*, vol. 20, no. 12, pp. 13425–13439, May 2012.

[18] Y. Huang, G. Xu, and S.-T. Xu, "An ultracompact optical mode order converter," *IEEE Photon. Technol. Lett.*, vol. 18, no. 21, pp. 2281–2283, Nov. 1, 2006.

[19] A. Mekis *et al.*, "A grating-coupler-enabled CMOS photonics platform," *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 3, pp. 597–608, May/Jun. 2011.

[20] W. D. Sacher, T. Barwicz, B. J. F. Taylor, and J. K. S. Poon, "Polarization rotator-splitters in standard active silicon photonics platforms," *Opt. Express*, vol. 22, no. 4, pp. 3777–3786, Feb. 2014.