Dot PIN Photodiodes With a Capacitance Down to 1.14 aF/μm^2

B. Goll, *Member, IEEE*, K. Schneider-Hornstein, and H. Zimmermann, *Senior Member, IEEE*

***Abstract*— PIN photodiodes with small half-spherical cathodes are investigated. They combine a large light-sensitive area with a very small capacitance. Dot photodiodes without and with shallow-trench isolation are compared. Also, the influence of an optical window on the responsivity is examined. The dot photodiodes were fabricated in 0.18 μm high-voltage CMOS without needing process changes. Capacitances down to 0.8 fF are achieved at a light-sensitive area of 706.9 μm^2. Responsivities in the range of 0.35 A/W to 0.4 A/W were observed for a wavelength of 635 nm. The −3dB cut-off frequencies for 675 nm light reach up to 300 MHz for reverse voltages up to 30 V. The rise and fall times reduce to about 0.8 ns and 1.0 ns, respectively, also at 30 V reverse bias.**

***Index Terms*— CMOS, integrated photodiode, low capacitance, PIN photodiode.**

I. Introduction

THE capacitance of a photodetector should be small for a high bandwidth (high data rate), high transimpedance and low noise (high sensitivity) of optical sensors and receivers [1]. Also integrated sensors [2], receivers [3], [4] and image sensors [5] benefit from a low photodiode capacitance. However, the detector's capacitance of ∼1 fF in image sensors is linked to a light-sensitive area of ∼1 μm^2 [5]. The capacitance of P/N-junctions increases proportional to the photodiode area and it is inversely proportional to the width of the space-charge region W [6]. A thin silicon-on-insulator (SOI) layer and non-standard processing for hole patterning to increase the responsivity were used for a 12.5 Gb/s 30-μm photodiode with a capacitance of 60 fF at 15 V, where W was 1.4 μm [7]. A thick low-doped absorption region, however, leads to a large W and can provide a low capacitance of a PIN photodiode. Usually, the light-sensitive area of a PIN photodiode is given by the P/N-junction area. Therefore, the P/N-junction area and the light-sensitive area need to be decoupled to be able to reduce the capacitance further, but without reducing the light sensitive area. This is possible by using also lateral depletion.

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The authors are with the Institute of Electrodynamics, Microwave and Circuit Engineering, Technische Universität Wien, 1040 Vienna, Austria (e-mail: bernhard.goll@tuwien.ac.at; kerstin.schneider-hornstein@tuwien.ac.at; horst.zimmermann@tuwien.ac.at).

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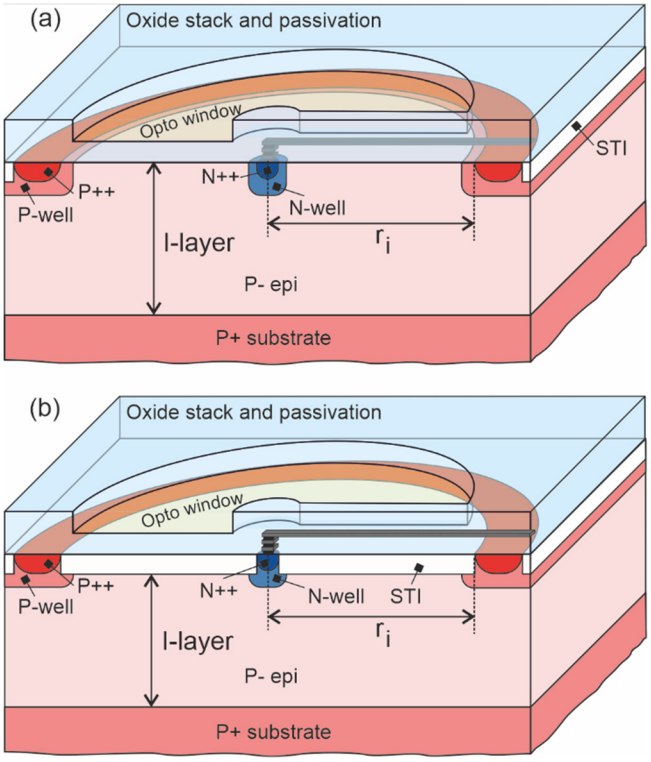

Fig. 1. Dot PIN-photodiodes with opto window. (a) Device 1. (b) Device 2 with STI.

The area capacitance of a PIN diode with an N$^+$ cathode having the size of 30 × 30 μm^2 and an I-layer thickness of 10 μm is 9.5 fF (note: a perimeter capacitance adds). A further capacitance reduction can be achieved using finger photodiodes [8]. For a 30 × 30 μm^2 lateral PIN diode using one N$^+$finger between two P$^+$ stripes in silicon (ε = 11.9), we can estimate a value of 6 fF. The next capacitance reduction follows when shrinking the cathode finger to a cathode dot. When we take a half-sphere as cathode dot with a radius $r = 1$ μm and use $C = 2\pi\varepsilon\varepsilon_0 r$ as a good approximation [9] for much thicker epi-layer and surface anode ring radius r_i(see Fig. 1) than r, we obtain C = 0.67 fF. This looks promising and the resulting structure is described in section II. Sections III, IV, and V present DC, capacitance, and AC properties, respectively. Section VI concludes the letter.

II. Structure of DOT PIN Photodiodes

The three-dimensional structure of the dot PIN photodiodes is presented in Fig. 1. The dot PIN photodiodes are fabricated in a thick low-doped epitaxial layer with a grown thickness of

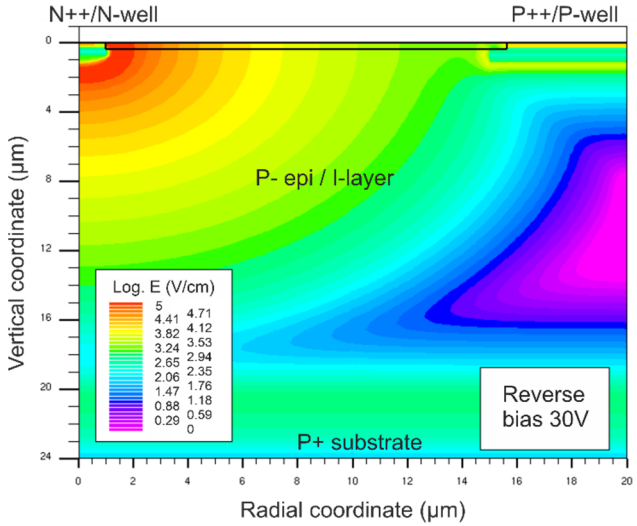

Fig. 2. Logarithmic electric field in device 2 with STI.

24 μm having a boron doping of about 1.5×10^{13} cm^{-3}. The bulk of the wafer is highly P$^+$ doped. The dot photodiodes are cylinder symmetrical. No process modifications were applied. The cathode dots consist of an N-well with a radius of 1.0 μm and the contact is made on an N+ region utilizing the source/drain doping of the 1.8 V N-channel MOSFET in the 0.18 μm high-voltage CMOS technology used. A ring P-well/P$^+$ anode with an inner radius r_i of 15 μm and a bottom P$^+$ substrate anode are applied in the dot photodiodes. The ring P-well/P$^+$ anode has a width of 5 μm.

In the first version of the dot PIN photodiodes, the P$^-$ intrinsic zone (I layer) reaches up to the vertical coordinate y = 0. In the second version, shallow-trench isolation (STI) is located between cathode dot and surface ring anode (Fig. 1(b)). The STI is 0.4 μm thick and the P$^-$ intrinsic zone reaches up to y = 0.4 μm (The vertical y coordinate is positive into the depth, see Fig. 2).

Both types of dot PIN photodiodes are covered by the complete isolation (SiO_2) and passivation (Si_3N_4) stack or a hole is etched into the passivation layer within the opto window. So, for each of the two types of dot PIN photodiodes, two different cover layers were tested: complete isolation-passiva-tion stack and opto-window. Figures 1(a) and 1(b) show the versions with the opto window. The central cathode requires a metal line leading over the I region in the highest metal level to keep its capacitance towards the substrate low. Therefore, the opto window has to be recessed from the metal line.

III. DC Characterization

Measurements showed that the breakdown voltage of the dot PIN photodiodes is larger than 60 V. The reverse current in darkness is below 1 pA (corresponding to 140 nA/cm^2) up to a reverse bias of 30 V. The responsivity was measured with a cut single-mode fiber carrying the light from a 635 nm laser diode. The optical power was set with an attenuator to below 1 μW and determined with an Ophir Nova power meter and a calibrated PD300-UV sensor. The photocurrent was measured with a Keysight B2987A electrometer. The results are listed in Table I for the four different dot PIN photodiodes.

TABLE I
Responsivities (R) at 635 nm

	R of device 1		R of device 2	
Reverse voltage	No opto window	Opto window	No opto window	Opto window
(V)	(A/W)	(A/W)	(A/W)	(A/W)
0	0.379	0.387	0.351	0.382
20	0.386	0.405	0.355	0.390
25	0.383	0.401	0.356	0.390
30	0.383	0.405	0.360	0.395

The devices with the opto-window possess a somewhat better responsivity at 635 nm due to less pronounced reflections in the insulating cover layers than the devices with the complete isolation and passivation stack. Device 1 shows a slightly higher responsivity than device 2 with the STI. The responsivities do not increase significantly from 20 V to 30 V. Therefore, impact ionization as used in [10] for a SPAD (avalanche photodiode in Geiger mode), is still negligible at 30 V reverse bias despite the small cathode radius of 1 μm.

The electric field within the dot PIN photodiodes was investigated by device simulation using the ATLAS tool [11]. Figure 2 shows the contour plot of the electric field strength of device 2 with the STI at a reverse bias of 30 V. The field distribution looks quite well as part of a sphere and the intrinsic zone is well depleted inside the surface anode ring.

Since the electric field drops rapidly at a depth of around 5 μm below the P-well/P$^+$ anode ring (from r = 15 μm to r = 20 μm), we do not count the area of the surface anode ring to the light- sensitive area of the devices and the light-sensitive area is determined by the inner radius r_i (15 μm) of the P-well/P$^+$ anode ring. So, the light-sensitive area is 706.9 μm^2.

To allow for a more detailed impression, the electric field strength along a vertical (at a radial position r = 0) and a horizontal cutline (at the silicon surface of the intrinsic zone) are plotted in Figs. 3 and 4, respectively. The extension of the electric field to a depth of about 19 μm in Fig. 3 suggests that r_i may be increased also to about 19 μm (with a certain loss in bandwidth). The bump in Fig. 3 between 19 and 24 μm is from boron diffusion from the P+ substrate. The electric field strength in the intrinsic zone of device 1 is slightly larger than in device 2 (see Figs. 3 and 4). Concluding, we can expect that device 1 should have a somewhat higher bandwidth and a low capacitance of the devices can be expected due to full depletion.

IV. Capacitance

The capacitance of devices 1 and 2 was calculated with the ATLAS TCAD tool [11]. For an AC small-signal analysis at 1 MHz, the results are shown in Fig. 5. At 30 V, the capacitance of device 1 reduces to 0.903 fF. At the same reverse voltage, the capacitance of device 2 with the STI is 0.806 fF.

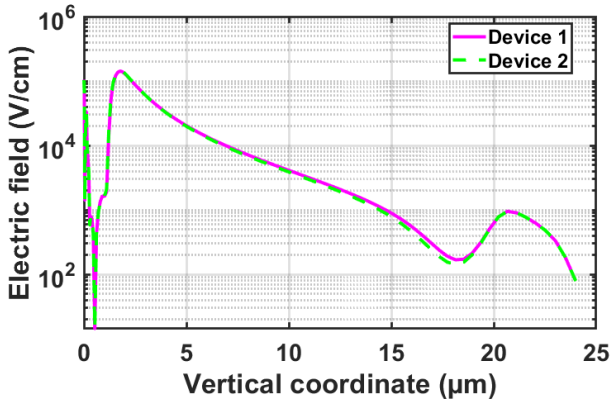

Fig. 3. Electric field in the center (r = 0) of devices 1 and 2 at 30 V reverse voltage.

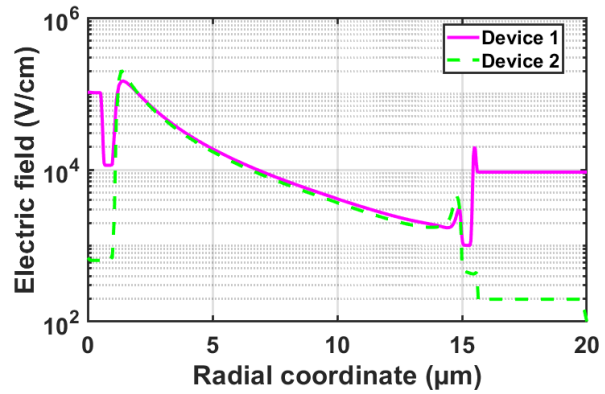

Fig. 4. Electric field in devices 1 and 2 along the silicon surface (device 1: y = 0, device 2: y = 0.4 μm) at 30 V reverse voltage.

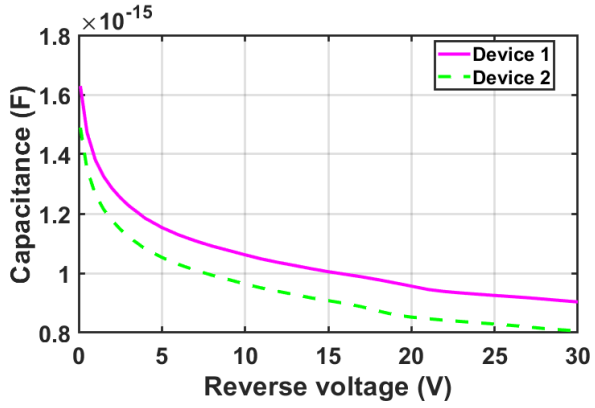

Fig. 5. Capacitance of devices 1 and 2.

Since both devices possess the same N-well and N$^+$ doping regions, the STI in device 2 reduces its P/N-junction area and this causes its lower capacitance. Considering the light-sensitive area of 706.9 μm^2, we obtain 1.28 aF/μm^2 for device 1 and 1.14 aF/μm^2 for device 2.

The capacitance values of devices 1 and 2 are somewhat larger than the value of 0.67 fF estimated in the introduction. This can be explained by the diffusion of the N-well during the process. So, the real cathode radius is a few 100 nm larger than the N-well design radius of 1.0 μm.

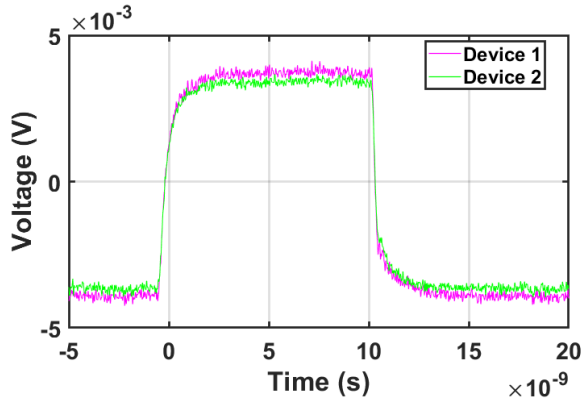

Fig. 6. Comparison of measured step responses of devices 1 and 2 at 30 V reverse bias.

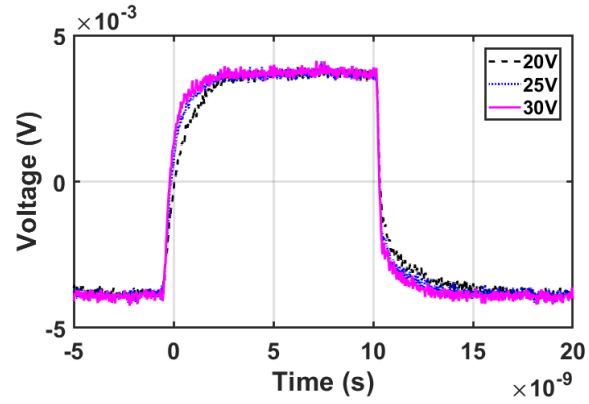

Fig. 7. Measured step responses of device 1.

V. Transient and Frequency Responses

The step response of the dot PIN photodiodes was determined with a 675 nm laser diode, modulated with a rectangular signal from a Sympuls bit pattern generator BMG 12GIG. The light from the laser diode with an optical power of 190 μW was coupled into the dot PIN photodiodes using a 50/125 μm multi-mode fiber. A 5530B bias-tee from Picosecond supplied the DC reverse bias to the dot PIN photodiodes. The transient response was recorded via a ground-signal probe and the bias-tee by a Tektronix TDS 6124C oscilloscope with an analog bandwidth of 12 GHz.

Figure 6 compares the measured transient responses of devices 1 and 2 (both with opto window). The rise and fall times of both devices seem to be quite similar, with a slight advantage of device 1. Because of the small differences in the electric field (Figs. 3 and 4) and in the step response (Fig. 6), we show only the voltage dependence of the step response of device 1 in Fig. 7. Table II lists the extracted rise and fall times (not corrected for the laser rise and fall times) also in comparison to device 2. Due to the low doping concentration in the epitaxial layer, the rise/fall times are already as short as about 1.5 ns at 20 V reverse voltage. The rise and fall times of device 1 are a little bit shorter than those of device 2, as expected above.

The frequency responses were measured with a vector network analyzer ZNB8 from Rohde&Schwarz, which modulated the 675 nm laser. The light from the 675 nm laser was coupled

TABLE II
RISE AND FALL TIMES (10%-90%) FOR 675 nm

	Device 1		Device 2	
Reverse voltage	Rise time	Fall time	Rise time	Fall time
(V)	(ns)	(ns)	(ns)	(ns)
20	1.23	1.68	1.41	1.50
25	1.05	1.43	1.31	1.44
30	0.80	1.05	0.83	1.06

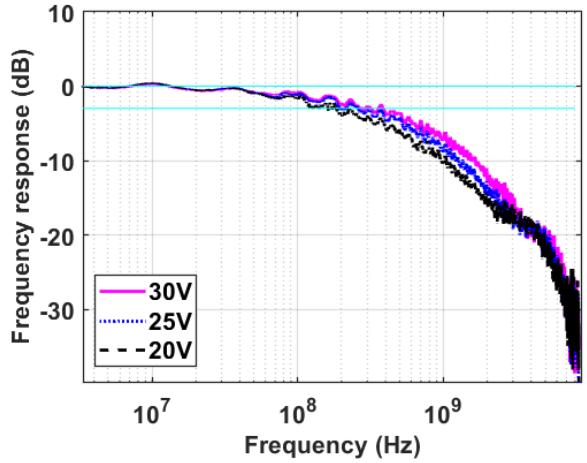

Fig. 8. Measured frequency responses of device 1.

TABLE III
−3dB CUT-OFF FREQUENCIES FOR 675 nm

Reverse voltage	Device 1 f_{-3dB}	Device 2 f_{-3dB}
(V)	(MHz)	(MHz)
20	170	110
25	250	180
30	310	300

into the dot PIN photodiodes with a mean optical power of 200 μW using a 50/125 μm multi-mode fiber. The generated photocurrents were measured with a 50-Ω ground-signal probe connected via a bias-tee to the 50-Ω input of the vector network analyzer. The DC reverse bias voltage was supplied to the devices via the 5530B bias-tee from Picosecond, which supports a frequency band from 20 kHz to 12.5 GHz. Figure 8 shows the measured frequency response of device 1 for three reverse voltages. A −3dB cut-off frequency of about 310 MHz is achieved at 30V reverse bias. Table III compares the extracted bandwidths of devices 1 and 2. Device 1 possesses somewhat larger bandwidths than device 2.

VI. COMPARISON AND CONCLUSION

The small cathode dots reduce the capacitance by factors of 8.2 and 9.2 compared to 10.5aF/μm^2 of a usual PIN photodiode, however at the cost of bandwidth reduction (from 625 MHz at 3 V to 300 MHz at 30 V) [12] due to exploitation of lateral depletion. The finger photodiodes of [8] in 0.6 μm BiCMOS had a capacitance of larger than 6.9 aF/μm^2. A SPAD with a cathode radius of 0.6 μm achieved a capacitance of 6.4 aF/μm^2 [10]. The corresponding value of finger photodiodes in SOI was even 92 aF/μm^2 [13]. In [14], for a PIN detector with a 40 μm epitaxial layer, a capacitance of 3 aF/μm^2 (neglecting the perimeter capacitance) was achieved.

The dot PIN photodiodes combine high bandwidths, respectively short rise/fall times at acceptable reverse voltages, with a very low capacitance at an interesting light-sensitive diameter of 30 μm. The STI reduces the capacitance, however at a small loss of bandwidth. The opto window increases the responsivity slightly for 635 nm. The noise of transimpedance amplifiers and optical receivers with integrated dot PIN photodiodes up to several hundred Mbit/s can be reduced thanks to the low capacitance. In a next step, multi-dot PIN photodiodes will be investigated to enable even larger light sensitive areas.

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