Keynote Addresses

Opening & Keynote I

Tuesday, January 21, 08:30 – 10:00

"All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure"

Dr. Ivo Bolsens

Senior VP and CTO, Xilinx, U.S.A.

Abstract: Today's FPGAs have become 'All Programmable SOC Platforms' that integrate in one single device multi-core CPU's, programmable DSP functions, programmable IO and programmable logic, all immersed in a rich and configurable interconnect network. These programmable platform FPGA's allow for the implementation of heterogeneous multi-core architectures that combine traditional CPU's with application-specific processing cores and dedicated data transfer and storage functions. This is enabled by tools that guide designers during the partitioning and mapping of high-level specifications onto a combination of software running on embedded processors and hardware implemented in programmable logic.

FPGAs are well placed to continue to benefit from Moore's law. Advances in process scaling will be augmented with new circuit and architectural improvements along with innovations in system-in-package technology to solve IO challenges and integrate heterogeneous technologies. These innovations will allow designers to build higher performance and lower power systems that optimally exploit the programmable FGPA architecture.

As FPGA platforms continue to deliver more performance at lower cost and lower power, they are becoming the heart of embedded applications such as complex packet processing for networks with line rates of 400+ Gbps; high performance digital signal processing in novel wireless baseband and radio functions; and high flexibility to enable programmable networking and data storage functions in cloud infrastructure.

Keynote II

Wednesday, January 22, 08:30 – 09:30

"Designing Analog Functions without Analog Transistors"

Prof. Georges Gielen

Katholieke Universiteit Leuven, Belgium

Abstract: Analog functions are indispensable for most electronic applications, ranging from telecom to biomedical or automotive applications. Yet, designing the analog circuits has become a large burden, especially in advanced CMOS technologies where reduced voltage headrooms and increased variability and reliability problems challenge the design of power-efficient analog circuits. Together with the lack of adequate EDA tools this also jeopardizes efficient analog circuit design. This keynote describes a possible way forward. The industry clearly has reached a bifurcation point. Many applications will leave the scaling race, and adopt older or nonstandard (e.g. flexible organic) technologies for the analog circuits, offering the increased functionality essentially through heterogeneous integration. Many other applications will stick to advanced CMOS, but will shift the analog design paradigm from analog-heavy to digital-heavy minimalistic-analog circuits. The presentation will discuss and illustrate the challenges and solutions in such approach to design analog functions without analog transistors.

Keynote III

Thursday, January 23, 08:30 – 09:30

"Beyond Charge-Based Computing"

Prof. Kaushik Roy

Purdue Univ., U.S.A.

Abstract: The trend towards ultra low power logic and low leakage embedded memories for System-On-Chips, has prompted researcher to consider the possibility of replacing charge as the state variable for computation. Recent experiments on spin devices like magnetic tunnel junctions (MTJ's), domain wall magnets (DWM) and spin valves have led to the possibility of using "spin" as state variable for computation, achieving very high density on-chip memories and ultra low voltage logic. High density of memories can be exploited to develop memory-centric reconfigurable computing fabrics that provide significant improvements in energy efficiency and reliability compared to conventional FPGAs. While the possibility of having on-chip spin transfer torque memories is close to reality, several questions still exist regarding the energy benefits of spin as the state variable for logic computation. Latest experiments on lateral spin valves (LSV) have shown switching of nano-magnets using spin-polarized current injection through a metallic channel such as Cu. Such lateral spin valves having multiple input magnets connected to an output magnet using metal channels can be used to mimic "neurons". The spin-based neurons can be integrated with CMOS and other devices like Phase change memories to realize ultra low-power data processing hardware based on neural networks, and are

suitable for different classes of applications like, cognitive computing, programmable Boolean logic and analog and digital signal processing. Note, for some of these applications, CMOS technologies may not be suitable for ultra low power implementation. In this talk I will first discuss the advantages of using spin (as opposed to charge) as state variable for both memory and logic and then present how a cellular array of magneto-metallic devices, operating at terminal voltages ~20mV, can do efficient hybrid digital/analog computation for applications such as cognitive computing. Finally, I will consider recent advances in other non-charge based computing paradigm such as magnetic quantum cellular automata.

Banquet Keynote

Wednesday, January 22, 18:30 – 21:30

"The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies"

Mr. Ulf Schneider

Managing Director, Lantiq Asia Pacific/President, SSIA, Singapore

Abstract: Since the mid 1960's Singapore has been an important pillar of the worldwide semiconductor industry, reinventing its portfolio, focus and strategy a few times to keep up with overall trends. Preparing for the next decade, Singapore's industry, research and academia has to put up again the right directions and strategy to keep up with the pace in a more and more competitive global environment. The talk will cover some of the really unique opportunities which Singapore has in this aspect.