A HARDWARE PROTOTYPE FOR INTEGRATION, TEST AND VALIDATION OF AVIONIC NETWORKS

José-Philippe Tremblay[1],
Yvon Savaria[1], Claude Thibeault[2],
Safwen Bouanen[2] & Guchuan Zhu[1]

1. École Polytechnique de Montréal
2. École de Technologie Supérieure

Outline

1. **Introduction**
2. Network architecture
3. Global approach
4. Implementation details
5. Prototype validation
6. Conclusion

1. Introduction

- Current trends in the avionics domain
  - Ever increasing number of functions
  - Information flow increase
  - Stringent reliability requirements
  - Diversity in the transducers market
  - Migration to IMA architecture

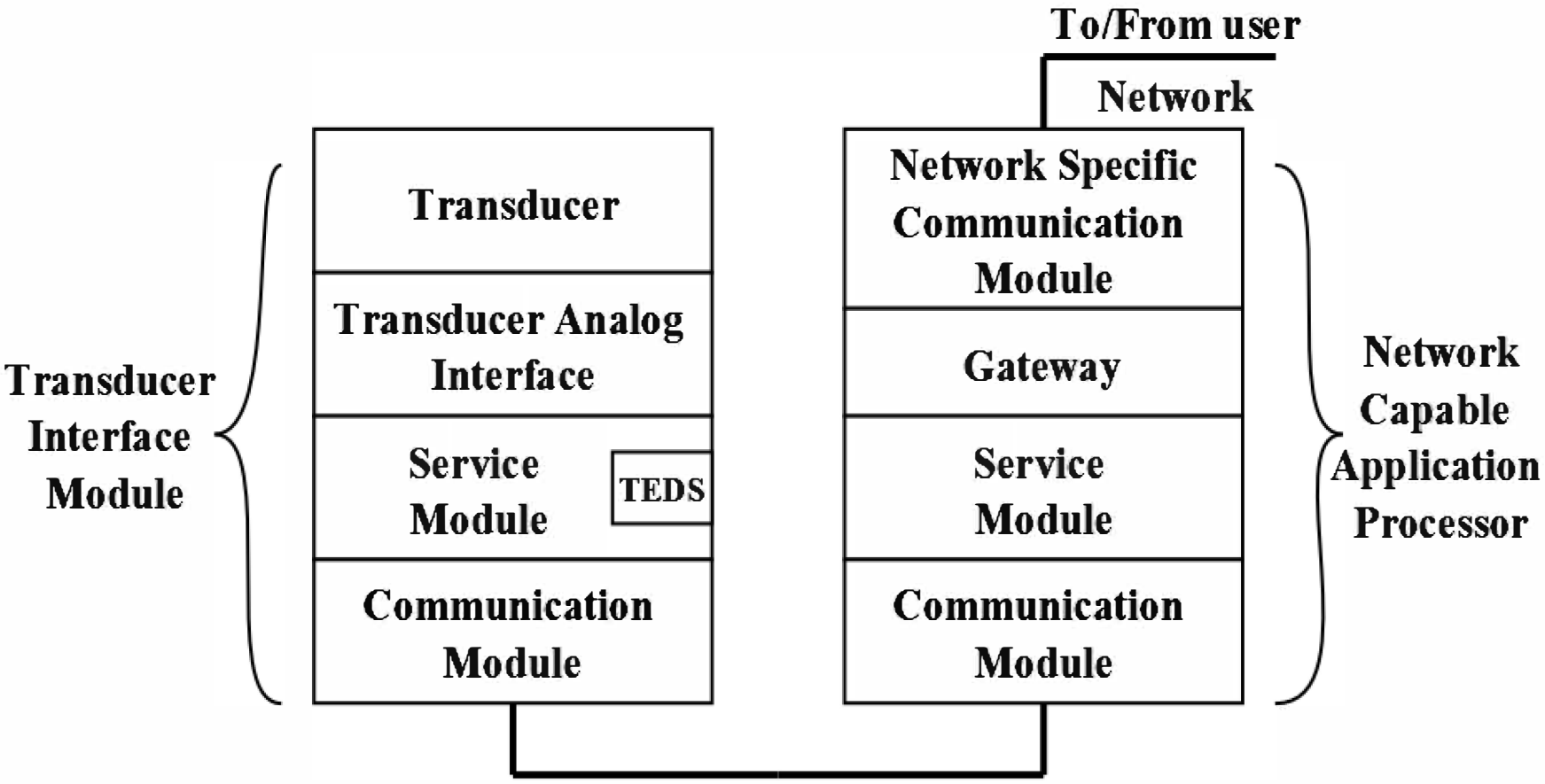
1.2 Introduction

- Main issues in transducer's integration
  - Different types of transducers
  - Different communication protocols
  - Significant design effort
  - Very costly and time consuming
- Solution
  - Systematic design approach
  - Normalized interfaces
  - Prototyping flexibility

2.1 IEEE 1451

- IEEE Standard for a Smart Transducer Interface for Sensors and Actuators
- Adoption Advantages
  - Increased compatibility
  - Reduced design effort
  - Reduced effort for installation, update, replacement or movement
- Considered but not yet adopted by the avionics domain

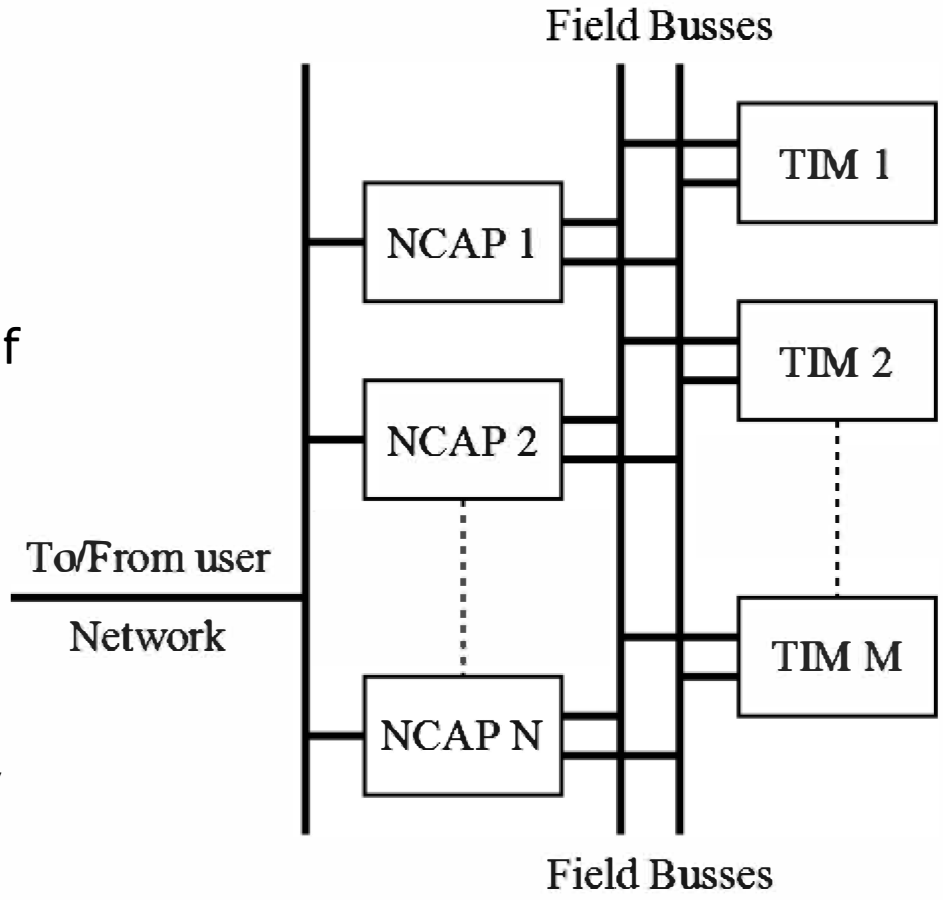
2.2 IEEE 1451



IEEE 1451 Reference Model

2.3 Network Architecture

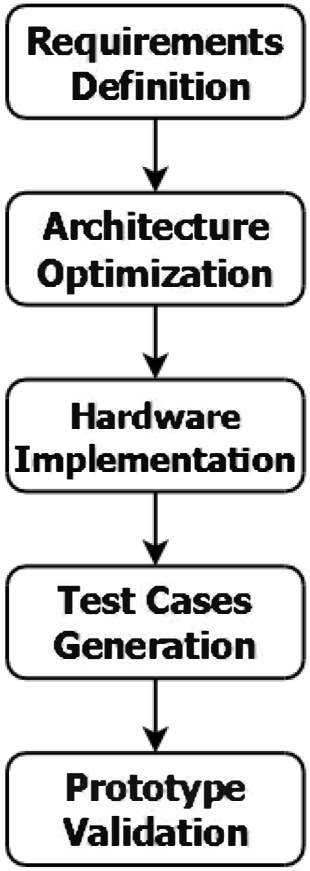
- Improvements over the basic IEEE 1451
  - Improved reliability
    - Adjustable by the number of NCAP and Busses
  - Improved performances
  - Improved resources utilization
  - Completely generic for any class of application
  - Reconfigurable



Generic Architecture

3.1 Global approach

- Main objective
  - Proposition of a systematic approach to validate new technological choices and their integration under important constraints
- Particular consideration for a compatibility with any certification process such as DO-254/DO-178
  - Compatible with current an future design
  - Supports new verification constructs
  - Tests should be easy to create, maintain and alter



3.2 Global approach

- Requirements definition
  - Modeled on traditional avionics requirements
- Architecture optimization
  - Generation of a configuration matching the specified requirements

Requirement	Constraint
Failure Rate	$< 10e^{-6}$
Load	< 50%
Determinism	Fully Deterministic
Frame's Latency	< 2ms
Bandwidth	1 Mbit/s

$$Load = \frac{\sum (Frame's\ Lenght * Nb\ of\ Frame)}{Transmission\ Interval * Bandwidth}$$

Typical ARINC 825 requirement

3.3 Global approach

- Hardware Implementation
  - Connectivity: COTS sensor, transducer emulator, commercial software and PC platform
- Test Cases Generation
  - Validation of custom fault management mechanisms
  - Supports specific purpose such as any certification process, maintenance or integration of new components
  - Motivation behind a custom latency measurement system
    - Customized tools best suited for global approach
    - Provides a better visualization at the system level

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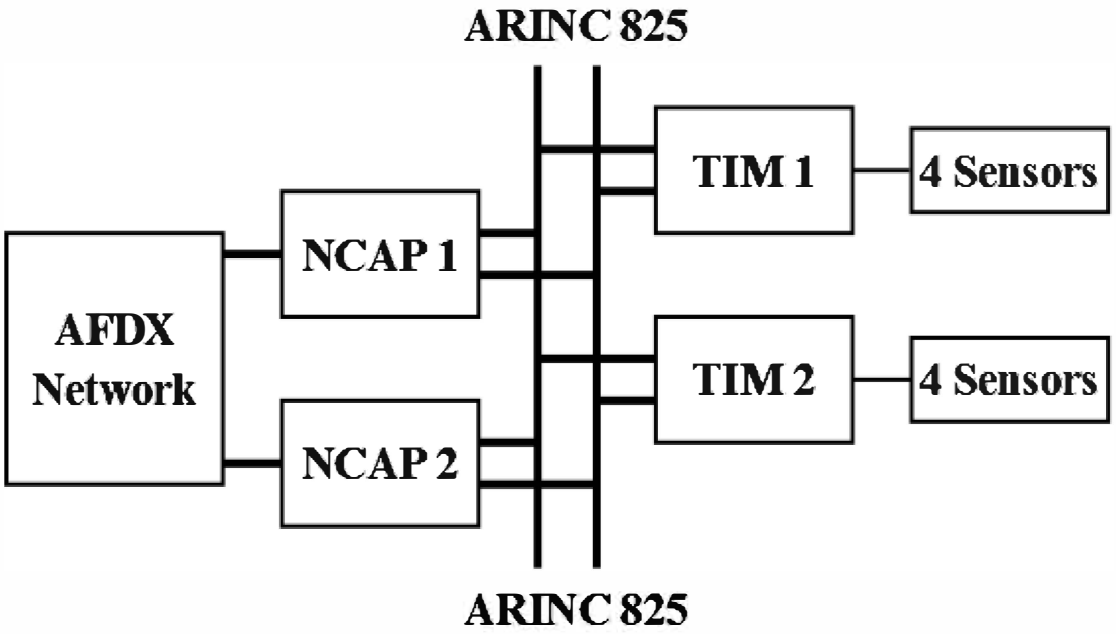
4.1 Implementation

- Architecture optimization
  - Configuration for the connection of 4 sensors to the main network for a critical system



Network architecture

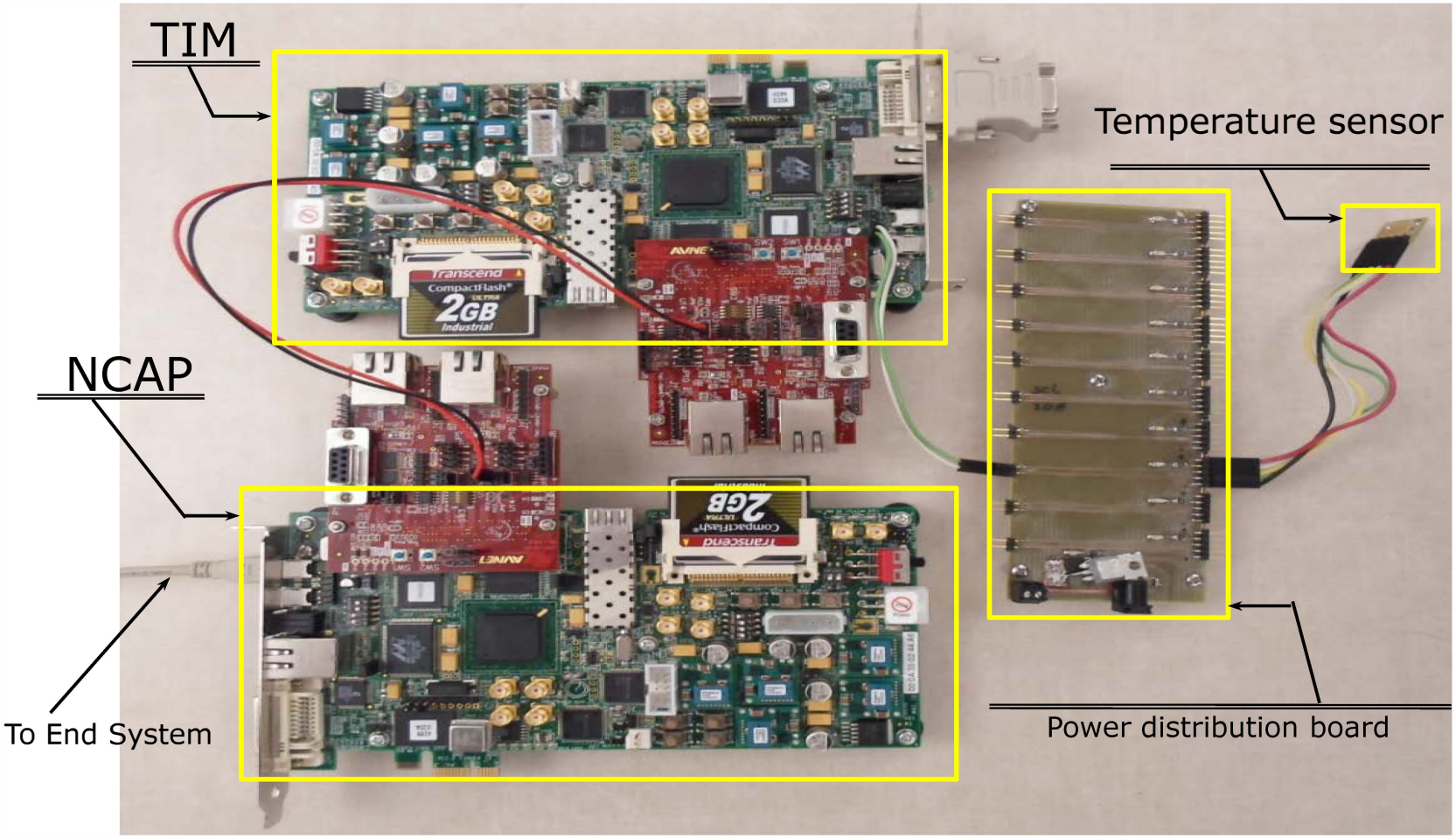
4.2 Implementation

- Prototype platform
  - 2 SP605 Xilinx FPGA Boards
  - 2 ISM Networking Boards
- Implementation of selected protocols
  - Field bus: ARINC825
  - Sensor Interface: I2C

Module	LUT		Registers	
Single ARINC 825 Controller	856	2%	1101	4%
Dual ARINC 825 Controller	1831	3%	2126	8%
TIM's Service Module	5975	11%	11198	41%
NCAP's Service Module	1112	2%	850	3%
TIM	7806	14%	13324	49%
NCAP	2943	5%	2976	11%
Total Architecture	21498	10%	24522	11%

Architecture's complexity

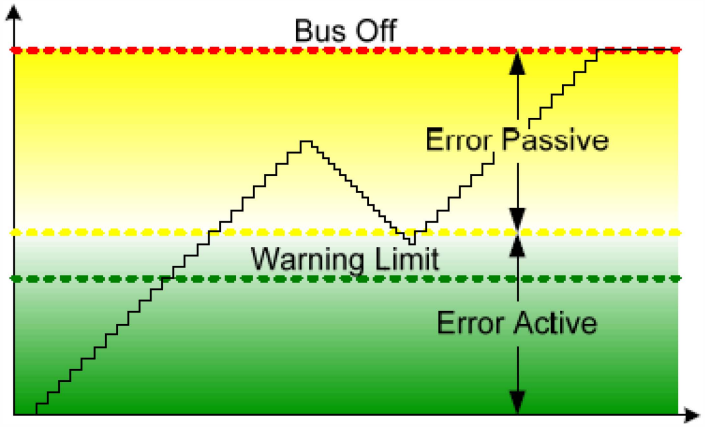
4.3 Implementation



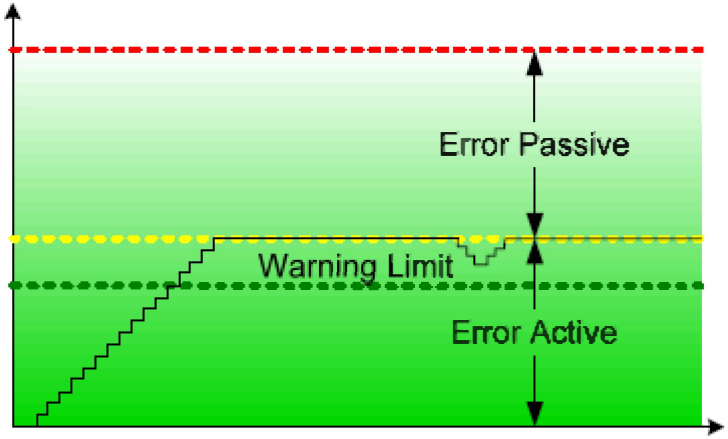
Prototype Implementation

4.4. Implementation

- The VHDL custom implementation allowed the inclusion of novel fault management schemes
- Redundancy management is based on the error containment system
  - Bus is shut off upon the degradation on bus on either transmission or reception



Transmitter Error Count Vs Mode of error



Receiver Error Count Vs Mode of error

5.1 Prototype Validation

- Test Cases Generation
  - Specific test designed for selected requirements at the required level
- Connection with commercial software ADS2
  - Bandwidth validation of ARINC 825
  - Tests generation at higher levels of abstraction
- Custom latency measurement
  - Integrated to the time synchronization mechanism of ARINC 825
  - Compensation for extra transmission time due to bit stuffing

5.1 Prototype validation

- Validation of the requirements
  - The maximum latency is inferior to 2 ms
  - The maximum load in normal mode is inferior to 50%
  - The slight variation of latency for each frame during each transmission cycle indicates a deterministic traffic

Field Bus Condition	Max Latency (us)	Load
Normal	0.65	33%
1 bus off	1.05	53%

Network Load

Sensor	Latency (Cycle)	Latency (us)
1A	2698	337
2A	3342	417
3A	4421	552
4A	5090	636
1B	2699	337
2B	3594	449
3B	4432	554
4B	5104	638

Average Frame's Latency

5.2 Prototype validation

- Identification of an unforeseen problem in our custom fault management mechanism
  - Upon degradation of a bus, retransmissions caused frames to miss their deadline
  - None of our models predicted this worst case situation occurring only during reconfiguration
- Final improvement
  - Modification over the original scheme to correct the problem and respect the requirements
  - A better knowledge of the standard is helpful in the identification and correction of this problem

6.1 Conclusion

- New approach for design and validation of an avionic network
  - The prototyping platform grants an increase connectivity and flexibility
  - The proposed approach is compatible with any certification process
- Future work
  - Automatic optimization of the architecture under a specific set of constraints
  - Validation of new algorithms and novel sensor designs

6.2 Questions