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An Efficient Grid-Connected Three-Phase Single-Stage Boost Current Source Inverter

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ABSTRACT The proposed three-phase boost Current Source Inverter (CSI) is equipped with Reverse-Blocking IGBTs (RB-IGBT) and the Phasor Pulse Width Modulation (PPWM) switching pattern to provide system efficiency greater than 92% and high boost ratios (V_{LL}/V_{dc}) up to 3.5 in a single stage. The boost CSI results in elimination of dc-dc boost converter or a step-up transformer needed in dc-ac converters operating with a dc input voltage lower than the output line-to-line voltage. In this paper, the relationship between the fundamental component of the inverter output current and the PPWM modulation index is derived and then confirmed by simulation and experimentally obtained data in both stand-alone and grid-tied modes of operation. In this work, a $\mathbf{2\,kW, 208\,V_{LLrms}, 60-120\,V_{dc}}$ RB-IGBT-based boost CSI is prototyped to explore capabilities of the grid-tied boost CSI in terms of efficiency and THD for various input dc voltage and output power levels.

INDEX TERMS Current source inverter, efficiency, grid-connected operation, reverse-blocking IGBT, single-stage boost inverter, steady-state characterization.

I. INTRODUCTION

The continuous growth in energy demand around the globe and limited availability of fossil fuels along with the increased awareness in the society about the impact of these fossil fuels on the environment has resulted in exploring of renewable energy sources (e.g. photovoltaic (PV) cells, fuel cells, wind turbines, etc.). These renewable energy sources are integrated into the existing power grid through grid-tied inverters. Typically, voltage source inverters (VSIs) are used in these applications. Since VSI is a buck converter, small dc sources such as PV panels need to be connected in series. A drawback of using a series connection of dc sources is that a dc source with the lowest current limits the current in the entire series connection [1], [2]. The main environmental reason for such uneven currents is partial shading of the PV panels [3]. In contrast to VSIs, single-stage boost inverter can operate with a low input voltage, and therefore, can employ a parallel connection of small dc sources (e.g. PV panels or fuel cells [4]–[7]).

Several power electronics circuit topologies for converting low dc voltage source outlets to a higher ac voltage have been proposed in the literature, where the majority of these circuit topologies employ the conventional voltage source inverter. A VSI is a buck (step-down) converter, i.e. $V_{dc} > V_{(LL,rms)}$, whereas a current source inverter (CSI) can operate as a boost converter. For example, a $60V_{dc}$ can be converted and boosted to $208V_{(LL,rms)}$ in a single stage using the boost CSI (shown in Fig. 1), whereas a conventional VSI requires a dc-bus voltage of 350V in order to create a three-phase $208V_{(LL,rms)}$. Furthermore, although the boost inverter borrows the CSI topology, a special switching pattern must be employed to create a single-stage boost inverter. Notice that a conventional CSI is either operated based on selected harmonic elimination (SHE) modulation or space vector pulse width modulation (SVPWM) switching pattern. The SVPWM switching pattern for CSI is formulated based on line-current space-vectors [8]–[11]. In an SHE based CSI, the shoot-through state is prevented, and thus, it does not have the capability to boost the input voltage [12]. However, the SVPWM based CSI has a charging state, making it capable of boosting the input voltage. The boost ratio (V_{LLrms}/V_{dc}) obtained from an SVPWM based CSI is low (being slightly more than 1.1) compared to the boost ratio as high as 3.5, using a PPWM based boost CSI.

FIGURE 1. Picture of the prototype 2kW 208V (240V) three-phase single-stage boost CSI.

Recently, several investigations have been reported on three-phase boost inverter and its application for renewable energy conversion systems. Kazerani *et al.* (1995) introduced the need for the shoot-through state to convert a dc voltage to higher ac voltage amplitude in a single-stage boost inverter [13]. However, their switching pattern required a relatively large dc-link inductor, i.e. 100mH, at Pulse Width Modulation (PWM) frequency of 1.2 kHz to obtain the boost ratio of 3.3, $V_{(LL,rms)}/V_{dc}$. Sahan *et al.* (2008), used conventional SVPWM built on inverter output currents to identify the switching pattern for a single-stage boost inverter [14]. However, their switching pattern required a dc-link current regulator loop and a high PWM frequency, i.e. $25kHz$, to achieve a total harmonic distortion (THD) of 4.5% for output currents. Mirafzal *et al.* (2011) presented a modified space vector PWM switching pattern for the boost inverter with a high boost ratio [15]. However, in their work, the THD of the output voltage and current waveforms exceeded 5% for R-L load. Additionally, there was no investigation on the system efficiency, the grid-tied inverter was not tested, and system characterization equations were not developed. Furthermore, the inverter presented used a series combination of IGBT and diode as switching devices which will decrease the overall system efficiency.

In a three-phase single-stage boost CSI, a path must always exist in which dc-link current can circulate. Also, the switching pattern is based on the assumption that solid-state switches can turn on and off instantly. In reality, however, a solid-state switch has a finite switching time. In VSIs, the finite turn-off time may cause a short-circuit of the dc-bus. Therefore, dead-times must be implemented to avoid commutation overlaps between switches. On the contrary, the presence of a dead-time in a boost CSI during a commutation can result in a huge voltage spike across the switches causing overvoltage failure. Kavimandan and Das (2013) suggested the use of a circuit containing a switch and antiparallel diode across the dc-link inductor to resolve this problem [16]. However, this circuit adds additional switch to the inverter which will contribute to the system losses. Singh *et al.* (2015) proposed an overlap-time in order always to guarantee a path for the dc-link current [17]. In their work, the dynamic state-space models of the boost CSI are presented in dq-domain, whereas the steady state efficiency and grid-connected operation have not been investigated.

Despite many investigations on the efficiency of boost rectifiers and single-phase boost inverters, only few reports can be found concerning the efficiency of three-phase boost inverters verified by experimental data. Zhou and Huang (2012) presented a three-phase boost inverter topology made of a coupling inductor, two diodes, two capacitors, and an inductor in the dc-side of a VSI [18]. In their work, a maximum efficiency of 83.4% was reported for a boost ratio of 2 (at the line-line output voltage of $220V_{rms}$) and a switching frequency of $8kHz$. Anand *et al.* (2014) presented a transformer-less grid-connected CSI with dc-bus capacitors, dc-link inductors, and an extra leg compared to the CSI topology [19]. However, this inverter provided a boost ratio of about 1.33 (at the line-line output voltage of $400V_{rms}$) with a switching frequency of $7.5kHz$, and high efficiency of the inverter was only possible without the boost capability. Brito *et al.* (2015) presented a tri-state buck-boost integrated boost inverter, which is a two-stage inverter, made of a cascaded dc-dc converter with a SVPWM based CSI [20]. In their work, an overall efficiency of 90% was reported for a boost ratio of 1.27 (PV module output of $\sim 100V$ is boosted to a line-line output voltage of $127V_{rms}$). The boost inverters reported so far either have a low boost ratio or have a low efficiency. This paper presents a PPWM based boost CSI with high boost ratio ($V_{(LL,rms)}/V_{dc}$) ranging to about 3.5 and also has a high system efficiency using Reverse Blocking IGBTs (RB-IGBTs), see Fig. 1.

In the next section, the inverter is characterized by deriving the relationship between the fundamental component of the inverter output current, the modulation index, and the dc-link current. The fundamental component of the inverter output current formula is then used to form the relationship between active power injected to the grid and modulation index. Simulation and experimental results confirming high performance of the boost CSI, and validating the equations derived in Section II are presented in Sections III and IV, respectively. In Section IV, the performance of a $2kW, 208V_{LLrms}, 60-120V_{dc}$ PPWM/RB-IGBT based boost CSI is examined in terms of the overall system efficiency, converter efficiency, and THD of output current with respect to power transferred

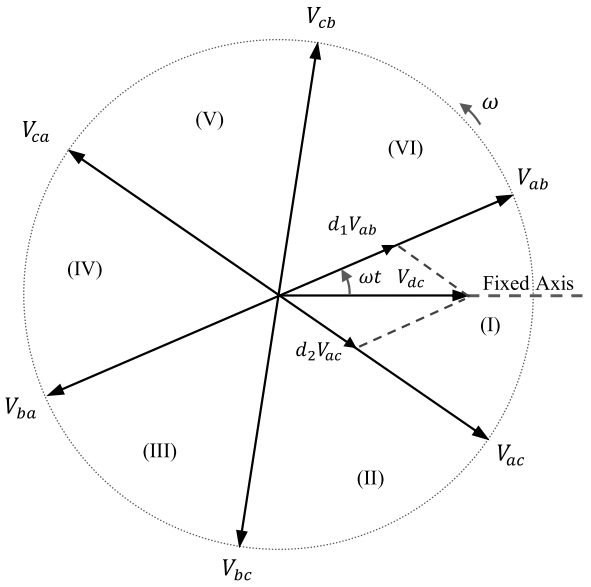


FIGURE 2. **Line-to-line voltage phasors and the associated sectors.**

to the grid and input dc-voltage. Lastly, a conclusion section completes the paper.

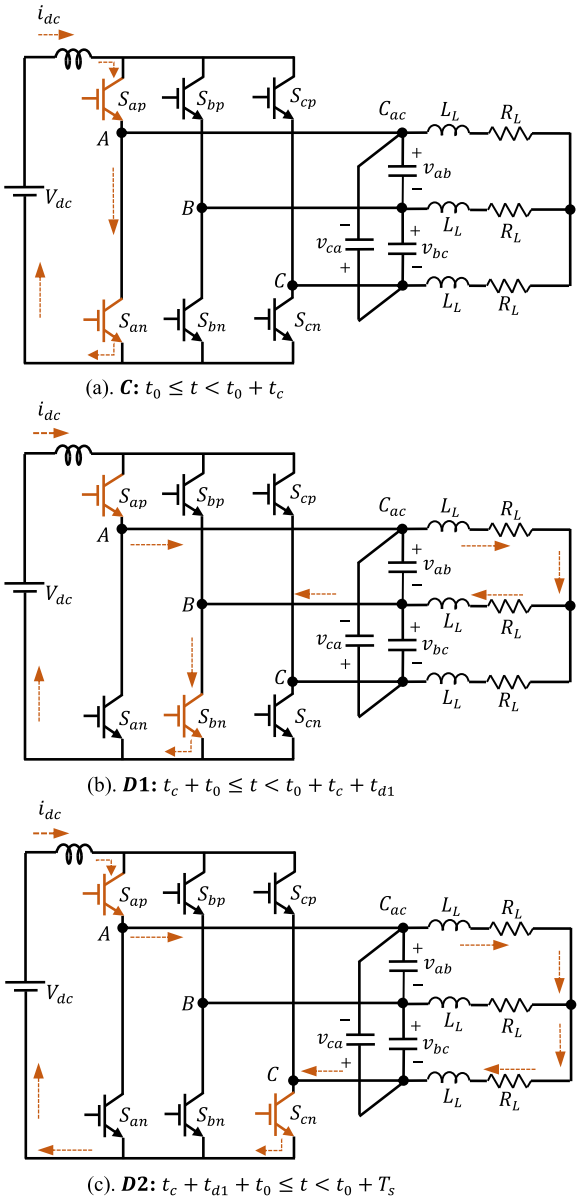
II. CHARACTERIZATION OF BOOST CSI

This section is divided into two subsections. In the first subsection, the Phasor Pulse-Width Modulation (PPWM) switching pattern for the boost CSI is reviewed as a background for deriving equations given later in this section. In the second subsection, an expression for the fundamental component of injected current and an expression for the transferred power to the grid are formulated as a function of the PPWM modulation index.

A. BOOST CSI SWITCHING PATTERN

In spite of similarities between PPWM for the boost CSI and SVPWM for VSI, there are fundamental differences. These differences can be herein summarized as (i) PPWM is formulated based on phasor quantities (line-to-line voltages), not space-vectors, (ii) in SVPWM, six main switching states, and two zeroes exist with three switches conducting at any given instant, however, in PPWM, six discharging and three charging states are present, with only two switches conducting at any given instant, (iii) in SVPWM, six vectors based on six switching states are stationary, and the desired space vector is formed by switching between these states and zeroes, while in PPWM, a stationary V_{dc} is known and line-to-line voltage phasors are formed by switching the dc-link current, as shown in Fig. 2. For further clarification, the charging and discharging states are described as follows:

State - C: In this state, the dc circuit is shorted through two switches from a same leg. For example, in Sector I (refer to Fig. 2 and Table 1) S_{ap} and S_{an}, are closed and the dc-link inductor is being charged over t_c. Fig. 3(a) shows



(a). **C:** $t_0 \le t < t_0 + t_c$

(b). **D1:** $t_c + t_0 \le t < t_0 + t_c + t_{d1}$

(c). **D2:** $t_c + t_{d1} + t_0 \le t < t_0 + T_s$

FIGURE 3. **Equivalent circuit of the boost inverter during (a) state C: charging time interval, (b) state D1: first discharging time interval, and (c) state D2: second discharging time interval of Sector I.**

the equivalent circuit of the converter and path of the dc-link current for this state in which voltage across L_{dc} equals V_{dc}.

State - D1: During the first discharging time-interval, t_{d1}, the inductor current is directed into phase A and returned from phase B in Sector I (refer to Fig. 2 and Table 1), when S_{ap} and S_{bn} are closed. Fig. 3(b) depicts the equivalent circuit of the boost CSI during t_{d1} when the voltage across L_{dc} equals to $V_{dc} - V_1 = V_{dc} - v_{ab}$.

State - D2: During the second discharging time-interval, t_{d2}, the inductor current is directed into phase A and returned from C, when S_{ap}, and S_{cn} are closed (see Fig. 2 and Table 1). Fig. 3(c) depicts the equivalent circuit of the boost CSI during t_{d2} when voltage across L_{dc} equals to $V_{dc} - V_2 = V_{dc} - v_{ac}$.

TABLE 1. Sectors and switching states in PPWM.

Sector	V_1	V_2	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}
(I)	V_{ab}	V_{ac}	T_s	t_c	0	t_{d1}	0	t_{d2}
(II)	V_{ac}	V_{bc}	t_{d1}	0	t_{d2}	0	t_c	T_s
(III)	V_{bc}	V_{ba}	0	t_{d2}	T_s	t_c	0	t_{d1}
(IV)	V_{ba}	V_{ca}	t_c	T_s	t_{d1}	0	t_{d2}	0
(V)	V_{ca}	V_{cb}	0	t_{d1}	0	t_{d2}	T_s	t_c
(VI)	V_{cb}	V_{ab}	t_{d2}	0	t_c	T_s	t_{d1}	0

From the voltage-second balance law for the dc-link inductor voltage at steady-state conditions, one can write $V_{dc}T_s = V_1\ t_{d1} + V_2\ t_{d2}$, where, V_1 and V_2 are different line-to-line voltages in each sector, as shown in Table 1. Dividing this equation by T_s, yields:

$$V_{dc} = V_1 d_1 + V_2 d_2 \tag{1}$$

where, $d_c = t_c/T_s$, $d_1 = t_{d1}/T_s$ and $d_2 = t_{d2}/T_s$, are the charging and discharging duty ratios, which are related as follows:

$$d_c = 1 - (d_1 + d_2) \tag{2}$$

The discharging ratios, d_1 and d_2, are obtained from the Law of Sines as $d_1 = m\ sin(\pi/3 - \theta)$ and $d_2 = m\ sin(\theta)$. Using (2), d_c is calculated as

$$d_c = 1 - m\ sin(\theta + \frac{\pi}{3}) \tag{3}$$

where, m is known as the modulation index. In order to improve the quality of generated ac voltages, a discretised version of phasor pulse width modulation (PPWM) is used based on constant charging time over each sector and staircase patterns for discharging time intervals. In the discretised PPWM, (i) averaged charging duty ratio, D, remains constant over each sector (one-sixth of the power cycle) and (ii) discharging times are discretised. In the discretised method, the numbers of points associated with the discharging time intervals are approximated by increasing and decreasing staircase functions. In this technique, n_c is obtained as $n_c = \lfloor D.N_T \rfloor$ where, $\lfloor\rfloor$ is the floor function, and N_T is mainly limited by the bandwidth of D/A converters when implementing PPWM on hardware. Herein, n_1, n_2, and n_c are the number of sampling points in the discharging and charging time intervals. The relationship between m, and D can be obtained by taking the average value of d_c over one sector as follows:

$$D = \frac{3}{\pi}\int_0^{\pi/3}\{1 - m\ sin(\theta + \frac{\pi}{3})\}d\theta = 1 - \frac{3}{\pi}m \tag{4}$$

The switching patterns of all switches over 18msec, i.e. slightly more than one power cycle, are shown in Fig. 4. The selection of N_T is also very important in maintaining symmetrical switching pattern and ensuring quarter-wave symmetry in the output voltage and current waveforms. Therefore, N_T must be chosen such that $N_T/6M$ becomes an integer number,

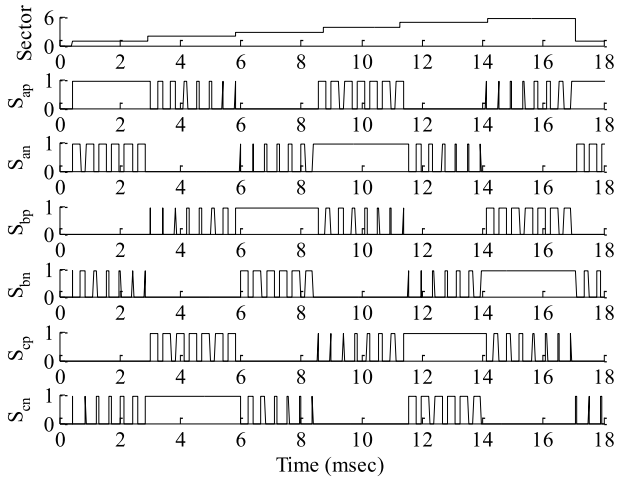


FIGURE 4. Switching pattern obtained from using PPWM.

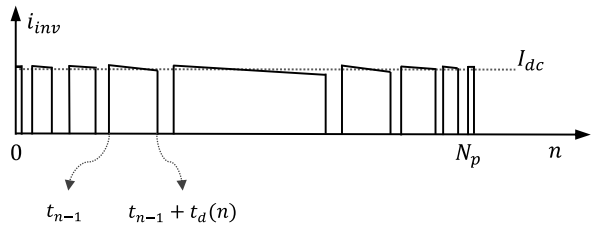


FIGURE 5. Output current waveform before ac-capacitor filter of phase a over a positive half cycle, in this figure $N_p = 9$.

where M is the number of step (discretised) changes, in n_1 and n_2, over one sector. As mentioned earlier, a path must always exist for the dc-link current in a single-stage boost CSI [16], [17]. This problem is resolved by employing an overlap-time, t_∇, i.e. a small duration when the three switches associated with a commutation process are conducting before turning off a switch.

B. BOOST CSI FUNDAMENTAL COMPONENT OF OUTPUT CURRENT, $I_{inv}^{rms}(f_1)$

In this subsection, the fundamental component of the inverter output current is calculated. For simplicity, the inverter output current is assumed to have rectangular-shape pulses, which implies that the dc-link current is ripple free, and thus, the inverter current over a positive half-cycle can be depicted as shown in Fig. 5, and expressed as follows:

$$i_{inv} = \begin{cases} I_{dc}, & t_{n-1} \le t \le t_{n-1} + t_d(n) n = 1, 2, \ldots, N_p \\ 0 & \text{Otherwise} \end{cases} \tag{5}$$

where $t_n = nT_s$ for $n = 1, 2, 3, \ldots, N_p$, and N_p is the number of pulses in any half-cycle, see Fig. 5. Also, $t_d(n) = d(n)T_s$ is the duration of discharging time, where $d(n)$ is the discharging duty ratio in the n^{th} pulse of the PWM pattern. Assuming that the PWM switching frequency is much higher than the line-frequency, from Fig. 5 and Fourier series expression, the rms value of i_{inv} fundamental component can be obtained

as follows:

$$I_{inv}^{rms} = \frac{1}{\sqrt{2}}\frac{4}{T_1}\int_0^{T_1/2} i_{inv}(t)sin(\omega_1 t)dt \tag{6}$$

where, ω_1 is the angular frequency of the grid voltage and can be related to N_p as $\omega_1\, T_s N_p = \pi$. Note that $\omega_1 t = \theta$, and θ here is same as that in (3). Now, the integral in (6) can be rewritten in a discrete format as follows:

$$I_{inv}^{rms} = \frac{1}{\sqrt{2}}\frac{4}{T_1}\sum_{n=0}^{N_p} I_{dc}d(n)sin(\frac{\pi}{N_p}n) \tag{7}$$

where, $N_p = T_1/(2T_s)$. Herein, the summation over $d(n)$ has to be calculated over half power cycle, and can be calculated for a phase (e.g. phase-A) and then generalized. For the positive half-cycle of phase-A, sectors VI, I, and II should be analyzed (see Table1). $d(n)$ is computed for each sector (sectors VI, I, and II for phase A) and shifted to the positive cycle resulting in

$$d(n) = \begin{cases} msin(\frac{\pi}{N_p}n); & 0 \le n < N_p/3 \\ 2msin(\frac{\pi}{3} + \frac{\pi}{N_p}n); & N_p/3 \le n < 2N_p/3 \\ msin(\frac{\pi}{3} - \frac{\pi}{N_p}n); & 2N_p/3 \le n < N_p \end{cases} \tag{8}$$

where, $n = 1, 2, \ldots, N_p$. Substituting (8) into (7) and then changing the variable to shift all the summations to the interval of $0 \le n < N_p/3$ yields

$$I_{inv}^{rms}(f_1) = \frac{\sqrt{2}I_{dc}m}{N_p}\sum_{n=0}^{\frac{N_p}{3}-1}\frac{3}{2} = \frac{\sqrt{2}I_{dc}m}{N_p}(\frac{3}{2}\frac{N_p}{3}) \tag{9}$$

which can be further simplified as

$$I_{inv}^{rms}(f_1) = \frac{I_{dc}}{\sqrt{2}}m = \frac{\pi}{3}\frac{I_{dc}}{\sqrt{2}}(1-D) \tag{10}$$

As can be observed from (10), the fundamental component of the inverter output current can be regulated by controlling the modulation index, m (or D). The equation $I_{inv}^{rms}(f_1)$ can serve as the knowledge base for steady-state analysis of the boost CSI. The detailed derivation of $I_{inv}^{rms}(f_1)$ is presented in Appendix V. The validity of (10) is confirmed using simulated and experimentally obtained data given in Sections III and IV. Also, the dc-link current varies with D, the input dc voltage, V_{dc}, and the grid voltage, V_{LL}. From the following dynamic equation [17]:

$$v_{dc} = (R_{dc} + 2R_{ON})i_{dc} + L_{dc}\frac{di_{dc}}{dt} + \frac{\sqrt{3}}{2}mv_q \tag{11}$$

Neglecting the dc-link current ripple and substituting $V_q = \sqrt{2}V_{LL}$ leads to the steady-state equation of I_{dc} as follows:

$$I_{dc} = \frac{V_{dc} - \sqrt{\frac{3}{2}}mV_{LL}}{R_{dc} + 2R_{ON}} = \frac{V_{dc} - \frac{\pi}{\sqrt{6}}(1-D)V_{LL}}{R_{dc} + 2R_{ON}} \tag{12}$$

where, R_{dc} is the dc-side resistance, R_{ON} is the on-state resistance of the IGBTs. By substituting (12) into (10) and neglecting the losses, the transferred active power to the grid can be written as

$$P_g = \frac{V_{dc}^2 - \frac{\pi}{\sqrt{6}}(1-D)V_{LL}V_{dc}}{R_{dc} + 2R_{ON}} \tag{13}$$

From (13), it can be observed that the active power transferred to the grid linearly varies with the averaged charging duty ratio, D, as will be demonstrated using experimental results later in Section IV. From (11) or (13), one can also find the minimum value of D for given input and output voltage levels as; $D_{min} = 1 - (\sqrt{6}/\pi)(V_{dc}/V_{LL})$, which can be validated from the experimental results given in Section IV. To achieve a low total harmonic distortion (THD) of the inverter output voltage and current, the inverter must operate in continuous conduction mode (CCM). The minimum inductance, L_{dc}, required to keep the inverter in CCM can be obtained from [21]:

$$L_{dc} > \frac{1}{2}\frac{1}{f_s}V_{dc}\frac{R_{dc} + 2R_{ON}}{V_{dc} - \sqrt{3/2}mV_{LL}}(1 - \frac{\sqrt{3}}{2}m) \tag{14}$$

TABLE 2. Circuit parameter values.

L_{dc}	C_{ac}	L_{ac}	f_s
$7.5mH$	$20\mu F$	$5mH$	$3.6kHz$

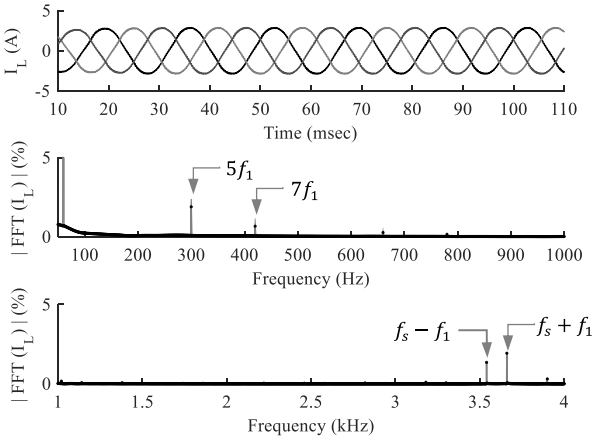


FIGURE 6. Phase current waveform for $N_T = 60$ and its FFT spectrum with THD = 3.23% for $V_{dc} = 65V$, and $R_{load} = 70\Omega$.

III. SIMULATION RESULTS

In this section, the validity of the proposed switching pattern and the developed formulas is verified using simulated results. The validity of the proposed switching pattern is evaluated through a set of simulations performed on the boost CSI in stand-alone (feeding local loads) and grid-tied modes of operation. The case study circuit parameters are given in Table 2.

As discussed in Section II, a proper choice of N_T can result in quarter-wave symmetry in inverter's current waveforms. Fig. 6 demonstrates the line current and its frequency spectrum for $N_T = 60$. This value of N_T provides an equal and

TABLE 3. Measured and calculated parameters of the grid-tied boost inverter (simulated results) for $P_g = 600W$.

$v_{dc}(V)$	D	$I_{dc}(A)$ Measured	$I_{inv}^{rms}(A)$ Measured	$I_{inv}^{rms}(A)$ Calculated
60	0.791	10.63	1.589	1.645
65	0.773	9.76	1.593	1.640
70	0.755	9.029	1.589	1.638
75	0.737	8.408	1.594	1.637

TABLE 4. Measured and calculated parameters of the stand-alone boost inverter (simulated results) for $V_L = 208\ V_{LLrms}$.

$v_{dc}(V)$	D	$I_{dc}(A)$ Measured	$I_{inv}^{rms}(A)$ Measured	$I_{inv}^{rms}(A)$ Calculated
60	0.66	13.44	3.286	3.384
65	0.63	11.87	3.251	3.252
70	0.54	9.226	3.116	3.143
75	0.50	8.592	3.126	3.181

integer number of sample points per sector, which results in quarter-wave symmetry in the inverter's current waveforms. In this study, $M = 10$ and $f_s = N_T f_1 = 3.6kHz$. It can be observed from Fig. 6 that there is no even harmonic component present in the current waveform.

The measured and calculated inverter fundamental current $I_{inv}^{rms}(f_1)$, using simulation as well as the expression in (10) are given in Tables 3 and 4 for grid-tied and stand-alone modes, respectively. In the stand-alone case, the inverter output voltage is regulated at $208V$ for several input dc-voltage values. As can be seen, the calculated results are in good agreement with the simulated results with less than 3% deviation. In the case of grid-tied conditions, the inverter injected $600W$ active power to the grid again for different input dc-voltages. The results are given in Table 4. As one can see, the difference between the measured and calculated values stays below 3.5%.

IV. EXPERIMENTAL RESULTS

In this section, the validity of the developed characterization equations is evaluated using a laboratory scale $2kW$, $208V(240V)$, $60Hz$ three-phase single-stage boost CSI shown in Fig. 1. Also, the efficiency of the overall system is calculated at different stages through a set of experiments for different input voltages and power levels.

The boost CSI was designed and built using six individual reverse-blocking IGBTs (RB-IGBTs) [17], [22]–[24]. The inverter prototype, shown in Fig. 1, contains two printed circuit boards called (i) control board and (ii) power board. The inverter is a self-powered device with control board powered directly by the dc input voltage. The IGBTs used in the boost CSI are RB-IGBTs from Fuji, i.e. FGW85N60RB. The inverter switching is generated by Altera's DE0 FPGA, which receives a control signal from dSpace 1103. The prototype boost CSI was tested for various input dc-voltage, V_{dc}, values and load impedances. In these tests, the discretized switching

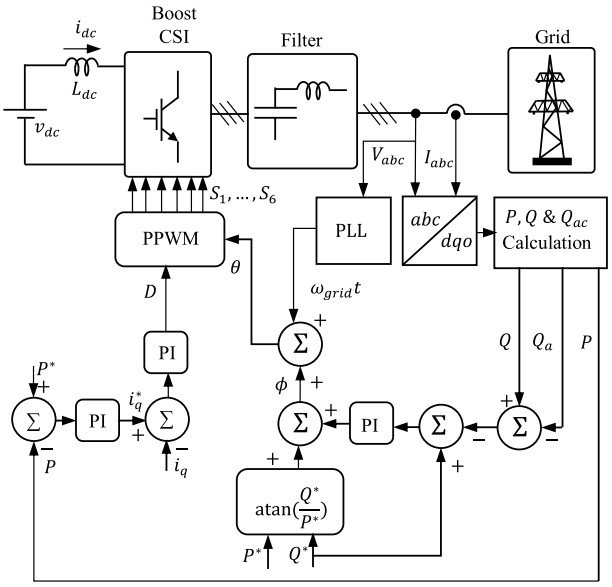


FIGURE 7. Block diagram of the system controller used for active and reactive power control injected into the grid.

TABLE 5. Measured and calculated parameters of the grid-tied boost inverter (experimental results) for $P_g = 600\ W$.

$v_{dc}(V)$	D	$I_{dc}(A)$ Measured	$I_{inv}^{rms}(A)$ Measured	$I_{inv}^{rms}(A)$ Calculated
60	0.80	10.98	1.56	1.63
65	0.78	10.11	1.59	1.64
70	0.765	9.41	1.61	1.64
75	0.74	8.71	1.61	1.68

pattern described earlier in Section II was implemented. In these tests, the fundamental and switching frequencies were set to $f_1 = 60Hz$ and $f_s = 3.6kHz$, respectively, with $M = 10$ and $N_T = 60$ in the discretized PPWM. The switching signals are generated by the FPGA using D and θ inputs, which are generated by the dSpace interface. In this work, a simple direct PQ control scheme was implemented for the purpose of steady-state analysis of grid-tied boost CSI. The control scheme is shown in Fig. 7. Basically, to build the closed-loop control scheme, the grid-side line-to-line voltages and line currents are measured as feedback signals. First, the desired reactive and active power injected into the grid are compared to the actual active and reactive power calculated from the measured line-to-line voltages and line currents. Then the charging duty ratio, D and the inverter switching pattern reference angle, θ are computed through PI controllers using the dSpace. The computed values of D and θ are then provided as input signals to the FPGA in order to generate the PPWM switching pattern described in Section II. The measured and calculated quantities for grid-tied and stand-alone modes of operation are summarized in Tables 5 and 6, respectively. The measured dc-link current was used to estimate $I_{inv}^{rms}(f_1)$ from (10). In order to verify

TABLE 6. Measured and calculated parameters of the stand-alone boost inverter (experimental results) for $V_L = 208\ V_{LLrms}$.

$v_{dc}(V)$	D	$I_{dc}(A)$ Measured	$I_{inv}^{rms}(A)$ Measured	$I_{inv}^{rms}(A)$ Calculated
60	0.66	14.53	3.66	3.59
65	0.64	13.57	3.62	3.54
70	0.60	10.88	3.22	3.37
75	0.58	9.87	3.07	2.99

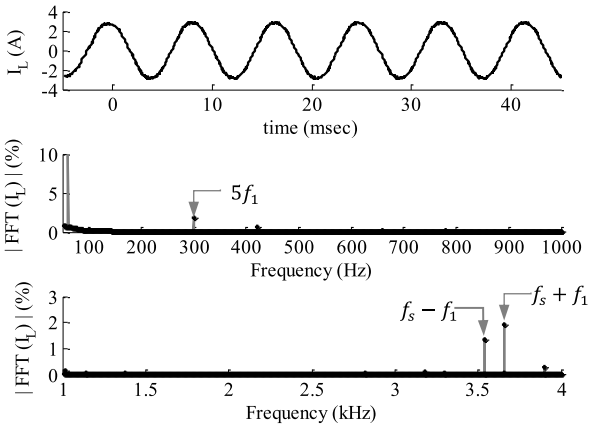


FIGURE 8. Experimentally obtained waveform of inverter phase a current when the inverter is operating with $V_{dc} = 80V$ and injecting $800W$ active power into the grid, and the current FFT.

the stand-alone case, the inverter was made to convert input dc-voltage to output $208V$ rms line-to-line voltage feeding a load. In the grid-tied test, the inverter injected active power to the grid for different input dc-voltages, where the desired reactive power was set to zero.

Fig. 8 shows the experimentally obtained waveform of the current injected into the grid and its FFT. The inverter was operated using $V_{dc} = 80V$ and was injecting $800W$ active power into the grid. The results presented in Fig. 8 show the quality of the inverter current is maintained using PPWM technique in grid-connected mode of operation. The measurements were performed for many operating points and the results are given in Tables 5, and 6, as well as Figs. 9, 10, and 11. It can be observed from the results given in Tables 5 and 6 that the measured quantities closely match the calculated quantities with errors being less than 4%. During the grid-tied mode, efficiency of the entire system, inverter with filter, and just inverter were also calculated. It can be observed from Fig. 9 that the overall system has an efficiency from $91 - 92\%$, for the entire operational range of the input dc voltage. The efficiency of the system, excluding the dc-link inductor loss, is about 94%. Also, the dc-link inductor contributes to about 2.75% to 3% of the system efficiency reduction, while the filter capacitor and inductor contribute to 1% to 1.5% of the overall system efficiency reduction. The dc-link inductor therefore contributes to about 34% loss incurred in the system and the loss contribution from the ac filter is about 17%. The inverter switching and conduction losses contribute to about 49% of the system losses, and the developed RB-IGBT based inverter is about 95% efficient, as shown in Fig. 9(a). Also, Fig. 9(b) shows efficiency of the overall system, inverter and ac filter, and inverter only versus the power injected to the grid for a constant input voltage, herein $V_{dc} = 80V$. It can be observed from Fig. 9 that the system efficiency is higher than 91% for the entire operating range. The efficiency of just inverter is higher by about 12%, 3%, and 0.5% than the efficiency reported for single-stage and two-stage boost inverters in [18], [19] and [25], respectively. The efficiency of the prototype boost inverter is comparable to the three-phase two-stage boost inverters [25], [26].

In Fig. 10, the relationship between the power flow and the averaged charging duty ratio, D, is examined using experimentally obtained data. Fig. 10 also shows the variation of system efficiency and the THD of current injected to the grid with respect to power injected to the grid through experimental data. The variations of the power injected to the grid, P_g, versus the charging ratio are demonstrated in Fig. 10(a). Herein, two main observations can be indicated; (i) an increase in the charging ratio will result in an increase in the power flow from the dc-source to the grid. In other words, the larger charging ratio means the more injected power to the grid, and (ii) the D-P relationship is almost linear as indicated earlier by (13). Also, the tested boost CSI demonstrates a superior performance regarding its controllability for the boost ratios below $208V_{LLrms}/60V_{dc} = 3.47$. Fig. 10(b) shows the relationship between input power at the dc-source and the power injected to the grid for different values of input dc-voltage. It can be observed from Fig. 10(b) that P_{dc} and P_g have a linear relationship regardless of the input

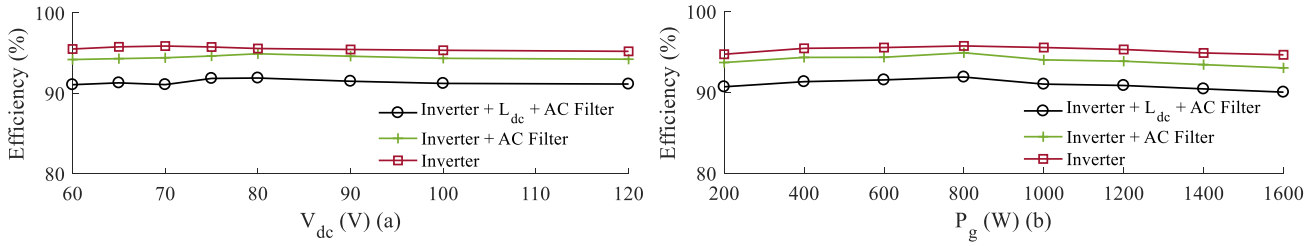


FIGURE 9. Experimentally obtained efficiency of the prototype boost inverter versus (a) input dc-voltage for the grid voltage of $208V_{LLrms}$, and $P_g = 600W$, and (b) power injected to the grid for the input dc-voltage of $V_{dc} = 80V$.

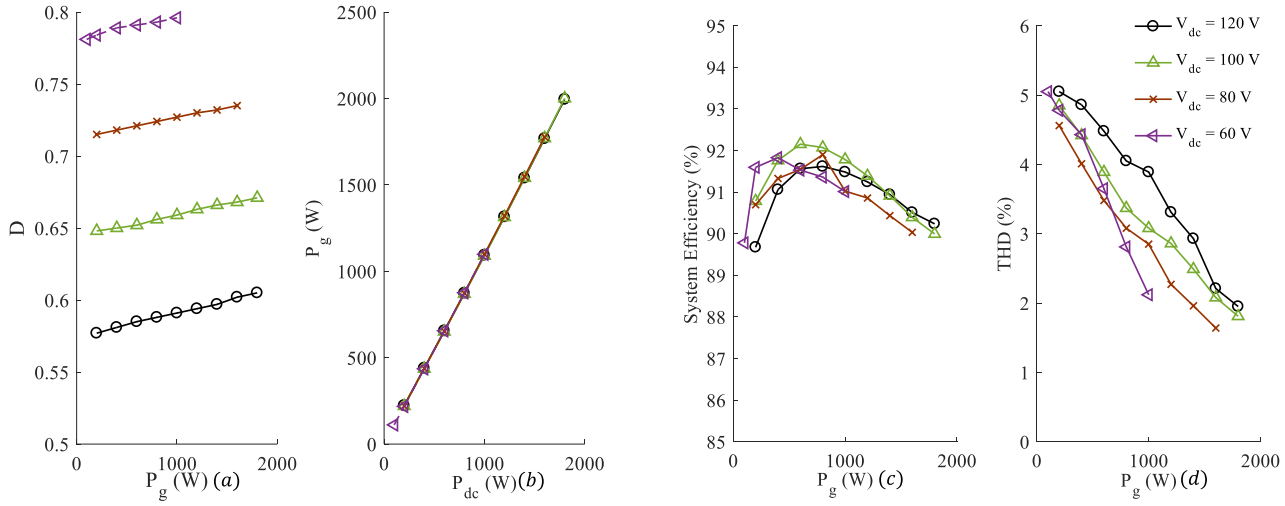


FIGURE 10. **Experimental results for the variations of the boost inverter (a) charging duty ratio, D, vs. input power, P_{dc}, (b) charging duty ratio vs. output power, P_g, (c) system efficiency, η, vs. output power injected to grid, and (d) THD of injected current to the grid vs. power for different input dc voltages.**

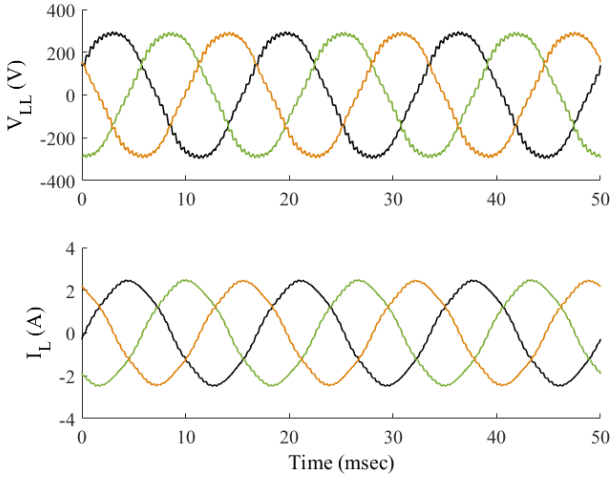


FIGURE 11. **Measured line-to-line voltage and line current waveforms of the prototype boost inverter when $P_g = 650\ W$ with $V_{dc} = 80V$.**

dc-voltage level. Fig. 10(c) shows the variation of the overall system efficiency versus P_g. It should be noted that this is the combined efficiency of the inverter, the dc-link inductor, and the ac filter. As can be seen, the system efficiency for the PPWM/RB-IGBT based single-stage boost CSI is higher than overall efficiency reported for the single-stage three-phase boost CSI in [18], and for the current source inverter in [19], with similar ratings. It can be further deducted from Fig. 10(c) that the tested system is optimal for operating around $P_g = 1kW$. Since there exists a maximum in the efficiency curves, it can be optimized by changing parameters in Table 2 for higher output power. Finally, Fig. 10(d) represents the variation of THD versus the transferred power to the grid for different input dc-voltages. As can be seen, THD of less than 5% was successfully achieved for all the operating points in the grid-tied mode of operation. It can be further observed that THDs for $V_{dc} = 120V$ and $60V$ are higher than for $V_{dc} = 80 or 100V$. This indicates that the optimal operating input voltage (in terms of THD level) is between $80V$ and $100V$ for the tested inverter. Fig. 10(d) also shows that the current THD reaches almost 5% for higher boost ratios and the inverter operates best for boost ratios less than 3.5. The inverter output current waveforms and the line-to-line voltage waveforms at the point of common-coupling, when the inverter is injecting $650W$ of active power into the grid, are presented in Fig. 11. The input dc voltage for the inverter during this test is $80V$. The line current THD for is measured to be about 4.71%. The THD for the wider operating region of the inverter is presented in Fig. 10(d). It can be observed from Figs. 11 and 10(d) that the inverter current THD for the operating range remains below 5%.

V. CONCLUSION

This paper provides the knowledge base for the steady-state analysis of the boost CSI. The switching technique generates desired inverter output waveforms with THDs below 5% from low-voltage dc-sources, with higher efficiencies in comparison with two-stage dc-ac boost converters. Furthermore, characterization equations have been derived and verified using simulation and experimental results. In this paper, a relationship between inverter averaged charging ratio, D and active power transferred to the grid is established. The simulation and experimentally obtained data has been presented in order to validate the derived equation for both stand-alone and grid-tied modes of operation. The efficiency of the overall circuit, and the inverter with the filter has also been examined using simulation and experimentally obtained data. It has been verified experimentally that the efficiency of the

prototype inverter and filter is comparable to commercial three-phase boost converters. The family of curves representing power injected to the grid with varying the charging duty ratio has been also presented for different input dc-voltages in this paper. The presented results demonstrate that the PPWM based three-phase single-stage boost CSI is an efficient alternative for two stage dc-ac boost converters, typically used in photovoltaic or fuel cells applications.

APPENDIX A
$I_{inv}^{rms}(f_1)$ DERIVATION

In this appendix, the detailed derivation of the fundamental component of the inverter output current is presented. From equation (6), $d(\theta)$ can be obtained for each sector in terms of θ as follows (using Table 1 and shifting to positive cycle)

$$d(\theta)=\begin{cases} msin(\theta); & 0 \le \theta < \pi/3 \\ m(sin(\theta+\frac{\pi}{3})+sin(\frac{2\pi}{3}-\theta)); & \pi/3 \le \theta < 2\pi/3 \\ msin(\frac{\pi}{3}-\theta+\frac{2\pi}{3}); & 2\pi/3 \le \theta < \pi \end{cases} \tag{15}$$

which on discretizing similar to (7) and further simplification yields:

$$d(n)=\begin{cases} msin(\frac{\pi}{N_p}n); & 0 \le n < N_p/3 \\ 2msin(\frac{\pi}{3}+\frac{\pi}{N_p}n); & N_p/3 \le n < 2N_p/3 \\ msin(\frac{\pi}{N_p}n); & 2N_p/3 \le n < N_p \end{cases} \tag{16}$$

where, $n = 1, 2, \ldots, N_p$. Substituting (16) into (7) yields

$$I_{inv}^{rms}=\left[\frac{I_{dc}^2 m}{N_p}\left\{\sum_{n=0}^{N_p/3-1} sin(\frac{\pi}{N_p}n)+2\sum_{n=N_p/3-1}^{2N_p/3-1} sin(\frac{\pi}{3}+\frac{\pi}{N_p}n) + \sum_{n=2N_p/3-1}^{N_p-1} sin(\frac{\pi}{N_p}n)\right\}\right]^{1/2} \tag{17}$$

changing the variables to shift to interval $0 \le n \le N_p/3$ and further simplification yields

$$I_{inv}^{rms}=\left[\frac{I_{dc}^2 m}{N_p}\left\{\sum_{n=0}^{N_p/3-1} sin(\frac{\pi}{N_p}n)+\sqrt{3}\sum_{n=0}^{N_p/3-1} cos(\frac{\pi}{N_p}n)\right\}\right]^{1/2} \tag{18}$$

Using the following trigonometric identities

$$\sum_{n=0}^{N} sin(nx) = \frac{sin(\frac{Nx}{2})sin(\frac{1}{2}(N+1)x)}{sin(\frac{x}{2})}$$

$$\sum_{n=0}^{N} cos(nx) = \frac{cos(\frac{Nx}{2})sin(\frac{1}{2}(N+1)x)}{sin(\frac{x}{2})}$$

(18) can be simplified to

$$I_{inv}^{rms}(f_1) = \frac{\sqrt{2}I_{dc}m}{N_p}\sum_{n=0}^{\frac{N_p}{3}-1}\frac{3}{2} = \frac{\sqrt{2}I_{dc}m}{N_p}(\frac{3}{2}\frac{N_p}{3}) \tag{19}$$

which can be further simplified as

$$I_{inv}^{rms}(f_1) = \frac{I_{dc}}{\sqrt{2}}m = \frac{\pi}{3}\frac{I_{dc}}{\sqrt{2}}(1-D) \tag{20}$$

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