Received 8 October 2018; accepted 28 January 2019. Date of publication 22 April 2019; date of current version 24 June 2019. Disital Object Identifier 10.1109/JPETS.2019.2902067

# Capacitance of UR-Core and C-Core Common Mode Inductors

# SCOTT D. SUDHOFF<sup>®1</sup> (Fellow, IEEE), HARSHITA SINGH<sup>®1</sup> (Student Member, IEEE), VEDA SAMHITHA DUPPALLI<sup>2</sup> (Member, IEEE), AND ROBERT R. SWANSON<sup>1</sup>

<sup>1</sup>School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA <sup>2</sup>Cummins Inc., Minneapolis, MN 55432 USA

CORRESPONDING AUTHOR: H. SINGH (singh341@purdue.edu)

This work was supported in part by the Department of Energy Contract DE-AC36-08GO28308 through the National Renewal Energy Laboratory under Subcontract ZEJ-6-62142-01, and in part by Continuous Solutions under U.S. Naval Air System Command Contract N00253-16-P-0235.

**ABSTRACT** An important aspect of all power processing equipment is common-mode current generation. Common-mode current leads to electromagnetic noise and potential equipment malfunction. Common-mode inductors are often used to reduce common-mode current. However, their effectiveness is limited by their capacitance. In this paper, common-mode capacitance models of two related classes of common mode inductors are set forth. These models include an improved method of calculating the layer-to-layer capacitance. Means of reducing capacitance by use of multiple inductors is discussed. The methodology for calculating capacitance is experimentally validated using several common mode inductors. Finally, the use of the model in a multi-objective optimization-based common mode inductor design algorithm is demonstrated.

**INDEX TERMS** Capacitance, common-mode inductors, common-mode chokes, common-mode current.

# I. INTRODUCTION

Power electronics-based power conditioning equipment is becoming ubiquitous in power systems. Equipment such as solar PV inverters can generate substantial common mode current [1]. Common mode current is undesirable because it can lead to electromagnetic noise and equipment malfunction. One approach to mitigate common mode current is through the use of common-mode inductors. However, the maximum frequency of effectiveness is limited by their common mode capacitance [2]. Thus, common-mode capacitance must be considered in the design process.

One approach to predict capacitance is through the use of electrostatic Finite Element Analysis (FEA). However, doing so requires representing structures with dimensions on the order of the wire insulation thickness. Further, since the common mode voltage varies along the coil, 3D analysis is required.

Today, many components are designed using poly-physics multi-objective optimization [3]. Examples including EI-core inductors [4], permanent magnet inductors [5], electric machinery [6], and converters [7] are widespread. Since such an approach requires  $10^4 - 10^7$  design evaluations, computationally efficient methods of calculating capacitance are desirable, and are thus the focus of this paper.

Several approaches for calculating different capacitance contributions for various types of inductors have been set forth in the literature. An analytical approach to predict self-capacitance as a function of inductor geometry is presented in [2]. This method is based on representation of the winding structure as unit cells. However, it doesn't include the impact of insulation between winding layers, the lowfrequency (inductive) voltage distribution on the conductors, or structural aspects such as coil-to-coil capacitance. A different approach is taken in [8] to calculate capacitance of a single-layer differential-mode solenoid air-core inductor. Ideas similar to those in [2], [8] are used in [9]-[11] to find turn-to-turn and turn-to-core capacitances for singlelayer differential-mode inductors. In [12], the common-mode capacitance of a single-layer common-mode toroidal inductor is considered.

This work considers capacitance in UR-Core and C-Core common-mode inductors. This class of inductor is easier to wind than toroidal inductors in the case of high-current applications, though suffer from the disadvantage of a small air gap due to surface roughness where the core halves come together. Coil-to-coil, coil-to-core, turn-to-turn, and layer-to-layer capacitances are considered. Contributions of this paper include calculation of coil-to-coil capacitance (which is unique to this geometry), consideration of the average core voltage in the coil-to-core capacitance calculation, and a new and more accurate means of calculating layer-tolayer capacitance in the presence of layer-to-layer insulation. In addition, means of reducing capacitance through multiple inductors is discussed.

This paper is organized as follows. First, the configuration of the two common mode inductor topologies considered is described (Section II). Next, four capacitance mechanisms will be considered. These include coil-to-coil capacitance (Section III), coil-to-core capacitance (Section IV), turn-toturn capacitance (Section V), and layer-to-layer capacitance (Section VI). Means of reducing the common-mode capacitance using multiple inductors is discussed in Section VII. Experiment validation of the model is set forth in Section VIII for five different common mode inductors. The use of the model in multi-objective common mode inductor design is demonstrated in Section IX.



FIGURE 1. Common mode inductor configuration.

# **II. CONFIGURATION**

The assumed configuration of a common mode inductor is shown in Fig. 1. Therein,  $v_{in}$  and  $v_{out}$  are the differential mode input and output dc rail voltages,  $v_{ui}$  and  $v_{li}$  denote the upper and lower rail input voltages relative to an equipotential plane (node 0, which can be thought of but need not be ground) and  $v_{uo}$  and  $v_{lo}$  are the upper and lower rail output voltages relative to that same plane. Literals 0-4 denote node numbers. The currents in the upper and lower rail are denoted  $i_u$  and  $i_l$ , respectively. Ideally, in the absence of common mode current,  $i_l = -i_u$ .

The input common mode voltage, output common mode voltage, and common mode current are defined as [13]

$$v_{cmi} = (v_{ui} + v_{li})/2$$
 (1)

$$v_{cmo} = (v_{uo} + v_{lo})/2$$
 (2)

$$i_{cm} = i_u + i_l \tag{3}$$

Figs. 2 and 3 depict cross sections of a UR-core CMI. Looking downward in Fig. 2 to the position of the dashed line yields the cross section shown in Fig. 3; looking upward in Fig. 3 to the position of the dashed line yields the cross section in Fig. 2. In Figs. 2 and 3 the inductor can be seen to be comprised of two contacting cores (grey) and two coils (orange). These two coils do not correspond to the two coils in Fig. 1. Rather each coil has two windings (upper rail and lower rail). The windings on the left coil in Fig. 2 are



FIGURE 2. UR core inductor.



FIGURE 3. UR core inductor.









tied in series with corresponding winding on the right side of Fig. 2.

Fig. 4 and 5 depict cross sections of a C-core CMI. The overall configuration is similar to that of the UR-core arrangement except that C-cores replace the UR core. This can be advantageous when using, for example, a nanocrystalline core which are generally tape wound as opposed to a UR-core which is commonly pressed (or machined) from ferrite.



FIGURE 6. Coil cross section.



FIGURE 7. Connections for common mode analysis.

The tape wound core can be constructed without an airgap though winding becomes more difficult.

Fig. 6 depicts a cross section of one side of one coil. Note the interleaving of upper (blue) and lower (yellow) rail conductors. As can be seen, the two windings of each coil are physically wound together as if they were parallel strands of the same winding in order to minimize differential mode inductance. A region of layer-to-layer insulation or open space (pink) may exist between winding layers to reduce capacitance. Coil metrics of interest in Fig. 6 include the number of strands per conductor (of one winding in a coil),  $N_{sc}$ , number of turns per layer,  $N_{tl}$ , number of layers,  $N_l$ , and number of turns in one of the two coils, N. In the example shown in Fig. 6, each turn consist of 2 stands of the upper rail winding and 2 strands of the lower rail winding.

In order to deduce the common mode properties of the inductor, from Fig. 1 and definitions (1)-(3) it can be seen that connecting the device as shown in Fig. 7 allows the common mode properties (inductance and capacitance) to be readily measured. Therein, the node numbering scheme of Fig. 1 is preserved. The connections shown in Fig. 7 also facilitate the numerical analysis of the common mode properties. The key feature is that the two windings in Fig. 1, can be viewed as parallel conductors of a single winding in Fig. 7.

### **III. COIL-TO-COIL CM CAPACITANCE**

One source of common mode capacitance results from the difference in potential between the two coil structures. In the case the UR-core CMI, the coils are cylinders. It can be shown [14] that the capacitance between two cylinders representing the outside of the windings in Fig. 3 may be expressed

$$C_{cc0} = \frac{\pi \varepsilon_0 d_W}{\ln\left(\frac{d}{2r_{wo}} + \sqrt{\left(\frac{d}{2r_{wo}}\right)^2 - 1}\right)}$$
(4)



FIGURE 8. Electric field lines for two rectangles.



FIGURE 9. Coil geometry transformation.

where  $\varepsilon_0$  is the permittivity of free space,

$$d = w_s + 2r_c \tag{5}$$

and the remaining quantities are geometrical parameters defined in Fig. 2 and Fig. 3.

In the case of the C-core CMI, first consider the electrostatic interaction between two rectangular prisms whose cross sections are as shown in Fig. 8. The prisms extend a distance  $d_w$  into the page. Therein,  $E_1$ ,  $E_2$ , and  $E_3$  show the assumed path of electric field lines.

For each of these field components, the assumed path of the field lines is assumed to consist of circular arcs and straight lines as shown. With the indicated paths, one obtains a capacitance of

$$C_{cc0} = \varepsilon_0 d_w \left[ \frac{h}{s} + \frac{2}{\pi} \ln\left(1 + \frac{\pi w}{s}\right) + \frac{1}{\pi} \ln\left(1 + \frac{\pi h}{\pi w + s}\right) \right]$$
(6)

The difficulty in applying (6) to compute the coil-to-coil capacitance directly is that the outside of each coil is not a rectangle; it is a rectangle with rounded corners, as can be seen in Fig. 5. In order to apply (6), consider Fig. 9 which includes a cross section of the coils. Therein, the pink coil rectangle ( $w_{clr}$  by  $l_{clr}$ ) defines the cross sectional shape of the coil which is no closer than  $r_{wi}$  to any point on the coil rectangle and no further than  $r_{wo}$  to the closest point on the coil rectangle. The approach will be to apply (6) by computing the rectangles which have the same centroid and cross section as the actual coil.

Using geometry, this may be accomplished using the sequence

$$a = w_{clr} l_{clr} + 2r_{wo} [w_{clr} + l_{clr}] + \pi r_{wo}^2$$
(7)

$$b = -[l_{clr} + w_{clr} + 4r_{wo}]$$
(8)

$$c = [w_{clr} + 2r_{wo}] [l_{clr} + 2r_{wo}] - a$$
(9)

$$\Delta = \frac{1}{2} \left[ -b - \sqrt{b^2 - 4c} \right] \tag{10}$$

$$w = w_{clr} + 2r_{wo} - \Delta \tag{11}$$

$$h = l_{clr} + 2r_{wo} - \Delta \tag{12}$$

$$s = c_{cc} + \Delta \tag{13}$$

Thus, with the values of w, h, and s calculated from (7)-(13),  $C_{cc0}$  may be found using (6).

While (4) represents an exact result, the expression given by (6) is approximate. A 2D FEA study was implemented in ANSYS Maxwell 16.0.0 to validate the value of coil-tocoil static capacitance per unit length  $C_{cc0}/d_w$  for a common mode inductor design. The geometric parameters in meters used in the study were:  $l_{clr} = 2.13$  cm,  $w_{clr} = 1.66$  cm,  $r_{wo} = 1.66$  cm,  $r_{wi} = 1.35$  cm,  $w_{cmc} = 2.23$  cm,  $l_{cmc} =$ 2.69 cm and  $c_{cc} = 0.52$  cm. Using (6), one obtains a capacitance of 78.1 pF/m; from the FEA analysis a value of 85.2 pF/m is obtained; a difference of 8.33%. Further validation is given in Section VIII.



FIGURE 10. Coil-to-coil and coil-to-core capacitance.

The value of  $C_{cc0}$  computed from either (4) for the UR-core CMI or (6) for a C-core CMI does not, on its own, accurately capture the coil-to-coil capacitance. This is because (4) and (6) are based on the assumption that the voltage between the two coils is constant when in reality, the voltage varies as one moves along the length of the coils. To this end, consider Fig. 10 which depicts the layered winding structure. Therein, the grey area represents the core. In Fig. 10, keep in mind the inductor connections are shown as in Fig. 7; in reality the path shown consists of two parallel but separate windings – one for the upper rail and one for the lower rail.

The voltage between coils may be expressed in the form

$$v_{cc}(x) = v_{cm} \left[ \alpha + \beta \frac{x}{l} \right] \tag{14}$$

The effective value of coil-to-coil capacitance is obtained using energy arguments. In particular, equating the energy stored as a lumped capacitance with that of a distributed capacitance,

$$\frac{1}{2}C_{cc}v_{cm}^2 = \frac{1}{2}\int_{0}^{d_w} \frac{C_{cc0}}{d_w}v_{cc}^2(x)dx$$
(15)

Substitution of (14) into (15) yields

$$C_{cc} = C_{cc0} \left[ \alpha^2 + \alpha \beta + \beta^2 / 3 \right]$$
(16)

In Fig.10, for the assumed set of connections  $v_{cc}(0) = v_{cm}$ and  $v_{cc}(l) = [1 - 1/N_l] v_{cm}$ . For the winding configuration shown, with external connections made on the outermost layer,  $\alpha = 1$  and  $\beta = -1/N_l$  so that

$$C_{cc} = C_{cc0} \left[ 1 - \frac{1}{N_l} + \frac{1}{3} \left( \frac{1}{N_l} \right)^2 \right]$$
(17)

It is interesting to observe that this component of capacitance decreases as the number of layers increases.

#### **IV. COIL-TO-CORE CM CAPACITANCE**

The electric coupling between the coil and the core also leads to capacitance. In this case the electric field lines extend from the core to each of the coils.

UR-core CMI are typically constructed of ferrite. Although the resistivity of ferrite is much higher than magnetic steels, it is still conductive enough that at high frequencies it may be viewed as a conductor. In the case of the UR-core CMI, the core and a coil form a cylindrical capacitor. It is readily shown that the capacitance may be expressed

$$C_{cr0} = \frac{2\pi\varepsilon_b d_w}{\ln\left(r_{wi}/r_c\right)} \tag{18}$$

where  $\varepsilon_b$  is the permittivity of the winding bobbin or material between the winding and the core.

In the case of the C-core CMI, the process is more involved. In this case, the first step in calculating the coil-to-core capacitance is to simplify the geometry. To this end, the rectangular cross section of the core (width  $w_{cmc}$  by length  $l_{cmc}$ ) is represented as a rectangle with rounded corners that is concentric with the inside of the inner coil layer. This rounded rectangle consists of the outer boundary of those points a distance  $r_{ce}$ from the coil rectangle (width  $w_{clr}$  by length  $l_{clr}$ ). The corner radius  $r_{ce}$  is established by equating the area of the rounded rectangle approximation to the core cross section with that of the core cross section using the sequence

$$d = 2 \left[ l_{clr} + w_{clr} \right] / \pi \tag{19}$$

$$e = \left[l_{clr}w_{clr} - l_{cmc}w_{cmc}\right]/\pi \tag{20}$$

$$r_{ce} = \left[\sqrt{d^2 - 4e} - d\right]/2\tag{21}$$

Assuming the equipotential surfaces are also rounded rectangles a distance r from the coil rectangle, where r varies between  $r_{ce}$  and  $r_{wi}$ , the coil-to-core capacitance for the C-core arrangement may be expressed

$$C_{cr0} = \frac{2\pi \varepsilon_b d_w}{\ln\left(\frac{2\pi r_{wi} + 2(w_{clr} + l_{clr})}{2\pi r_{ce} + 2(w_{clr} + l_{clr})}\right)}$$
(22)

In the case of the UR-core CMI, the expression given by (18) is exact, whereas the expression for the C-core CMI is approximate. In order to gain insight into the amount of error that may exist a study is performed for C-core CMI D121 considered in Section VIII. For this study,  $C_{cr0}/d_w$  was calculated using (22) and using FEA with  $\varepsilon_b = \varepsilon_0$ . The analytically estimated value (22) is 123 pF/m; using FEA analysis a value of 118 pF/m is obtained. Thus the error in (22) for this set of parameters is 4.24%. Further validation is carried out in Section VIII.

As in the case of the coil-to-coil capacitance, the fact that the voltage varies along the length of the core must be taken into account. To do this, once again consider the configuration of Fig. 7 as well as the layer winding diagram shown in Fig. 10. Consider points 1, 2, 3, and 4. Denote  $v_x$  where  $x = \{1, 2, 3, 4\}$  to represent the voltage of each of the points relative to the negative terminal of the common mode voltage (node 3,4 of Fig. 7); and  $v_{xc}$  to be the voltage of each point on the coil relative to the core. Let  $v_c$  denote the core voltage relative to the negative terminal of the common mode voltage.

It can be shown that

$$\begin{bmatrix} v_1 & v_2 & v_3 & v_4 \end{bmatrix} = \frac{v_{cm}}{2N_l} \begin{bmatrix} N_l - 1 & N_l & N_l + 1 \end{bmatrix}$$
(23)

Since the net current into the core is zero it follows that

$$v_c = \frac{1}{4} \left[ v_1 + v_2 + v_3 + v_4 \right] = \frac{v_{cm}}{2}$$
(24)

From (23) and (24)

$$\begin{bmatrix} v_{1c} & v_{2c} & v_{3c} & v_{4c} \end{bmatrix} = \frac{v_{cm}}{2N_L} \begin{bmatrix} -1 & 0 & 0 & 1 \end{bmatrix}$$
(25)

Assuming a linear variation in coil voltage between the indicated points, and using energy arguments (and considering both coils), the effective value of coil-to-core capacitance  $C_{cr}$ is expressed

$$C_{cr} = \frac{C_{cr0}}{6N_l^2} \tag{26}$$

As in the case of the coil-to-coil capacitance, the coil-to-core capacitance decreases with the number of layers.

#### V. TURN-TO-TURN CM CAPACITANCE

It can be shown that the turn-to-turn capacitance per unit turn length between cylindrical conductors on the same layer may be calculated using the sequence [2]

$$\theta = a \cos\left(1 - \frac{\varepsilon_{ei}}{\varepsilon_{si}} \ln\left(1 + \frac{t_{si}}{r_{sc}}\right)\right)$$
(27)  
$$\hat{C}_{tt0} = \frac{\varepsilon_{si}\theta}{\ln\left(1 + t_{si}/r_{sc}\right)} + \varepsilon_{ei} \left[\cot\left(\frac{\theta}{2}\right) - \cot\left(\frac{\pi}{12}\right)\right]$$
(28)

In (27)-(28),  $\varepsilon_{si}$  and  $\varepsilon_{ei}$  are the permittivity of the strand insulation and the region between conductors, and  $r_{sc}$  and  $t_{si}$  are the radius of a strand conductor (w/o insulation) and thickness of the strand insulation, respectively. These expressions are based on an orthocyclic winding arrangement but are also appropriate for turn-to-turn capacitance calculation between conductors on the same layer since most of the capacitance results from the region where conductors are closest together.

Using energy arguments, and noting that the voltage between adjacent turns is given by  $v_{cm}/(2N)$ , the total turn-to-turn capacitance may be expressed

$$C_{tt} = \frac{\hat{C}_{tt0} \left(N_{tl} - 1\right)}{2N^2} \sum_{i=1}^{N_l} l_{t,i}$$
(29)

where  $l_{t,i}$  is the length of a turn of the *i*'th layer. It should be noted that the turn-to-turn capacitance is in many cases negligible except when the number of turns is low and there is a single layer.



FIGURE 11. Assumed field lines for layer-to-layer capacitance.

#### VI. LAYER-TO-LAYER CM CAPACITANCE

The calculation of the layer-to-layer capacitance is based on the geometry shown in Fig. 11. Therein,  $r_o$  denotes the radius of a strand with insulation, and the thickness of the layer-tolayer insulation is denoted  $t_{lli}$ . The permittivity of the layerto-layer insulation is  $\varepsilon_{lli}$ .

For a path starting at an angle  $\theta$  in Fig. 11 the electric field line is assumed to travel radially from the conductor material through the strand insulation, follow a semicircular arc from the strand insulation to the layer-to-layer insulation, and then proceeds in a straight line through the insulation and then a symmetric path back to the opposite conductor. The radius and center of the arc are such that ends of the arc are normal to both the strand insulator and layer-to-layer insulation. It can be shown that the radius of this arc is given by

$$r_a(\theta) = r_0 \frac{1 - \cos\theta}{\sin\theta} \tag{30}$$

and that the angular span of the arc is  $\theta$ . Based on this path, the capacitance per length of turn and per unit length in the x-direction (see Fig. 10) may be expressed

$$\hat{C}_{ll0} = \int_{\varepsilon}^{\pi/3} \frac{1}{2r_0 \ln \left( r_o/r_{sc} \right) / \varepsilon_{si} + 2r_a(\theta)\theta / \varepsilon_p + t_{lli}/\varepsilon_{lli}} d\theta \quad (31)$$

In (31),  $\varepsilon$  is a small number, for example  $10^{-6}$ , and is used to avoid a singularity (30) when evaluated at zero. The integrand is not ill-conditioned however, since it remains finite in the limit as  $\theta$  goes to zero. The upper limit is established by the fact that at  $\theta = \pi/3$  the electric field line extends a distance  $r_0$  in the *x*-direction. The upper limit in (30) is also consistent with avoiding overlapping field lines when considering the turn-to-turn capacitance.

It is interesting to consider a practical example. To this end, parameters are selected in accordance with those listed for inductor D193 of Table 1 from Section VIII, Validation. Using FEA analysis, a value of  $17.8 \text{ nF/m}^2$  is obtained. Using (31), a value of  $17.1 \text{ nF/m}^2$  is calculated. This is an error of 4.1%.

In practice, it is doubtful if the layers will be aligned as shown in Fig. 11. Using FEA analysis, if the lower conductors are shifted by a strand radius, the capacitance changes to 15.5 nF. The average of the FEA estimates of the fully aligned and unaligned cases is 16.7 pF; the error between the average FEA results and the analytical method is 2.7%.

It is assumed that a standard winding configuration is used in which once a layer is wound, the next layer is wound starting where the previous layer ended and ending where the previous layer started. In such a configuration, there is zero voltage between layers on the end with the connection, and twice the layer voltage at the far end. With this arrangement, and considering that there are two series connected coils, the net layer-to-layer capacitance may be expressed

$$C_{ll} = \frac{\hat{C}_{ll0}d_w}{3N_l^2} \left[ l_1 + 2\sum_{i=2}^{N_l-1} l_i + l_{N_l} \right]$$
(32)

In (32), as in (29),  $l_{t,i}$  is the length of a turn on the *i*'th layer.

# VII. REDUCING CM CAPACITANCE WITH MULTIPLE INDUCTORS

As discussed in the introduction, the capacitance of the common mode inductor is the major limitation in determining the useful frequency band. Thus, reducing common-mode capacitance is of considerable interest. One means of reducing common mode capacitance is to use multiple common mode inductors in series.

At first, such an idea, may seem counterintuitive. The resonant frequency of an inductor with inductance  $L_1$  with

shunt capacitance  $C_1$  is given by

$$f_r = \frac{1}{2\pi\sqrt{L_1C_1}}\tag{33}$$

If one ties N such inductors together in series, the effective inductance becomes  $NL_1$ , the effective capacitance becomes  $C_1/N$ , and the resonant frequency is unchanged. What such an argument misses is that the capacitance is dependent upon the inductance.

Suppose a total common mode inductance of  $L_{cm}^*$  is desired. Now suppose this desired inductance is split between  $N_{cmi}$  common mode inductors. The needed inductance of each individual common mode inductor is thus

$$L_{cmi} = L_{cm}^* / N_{cmi} \tag{34}$$

Now, for the purposes of explanation only, suppose a single common mode inductor with inductance  $L_{cm}^*$  has a common mode capacitance  $C_{cm}^*$ . Assuming that for inductors of similar voltage and current ratings that capacitance is proportional to inductance, then the capacitance associated with an inductor of inductance  $L_{cmi}$  is given by

$$C_{cmi} = C_{cm}^* / N_{cmi} \tag{35}$$

The total series inductance and capacitance of the  $N_{cmi}$  inductors in series is thus  $L_{cm}^*$  and  $C_{cm}^*/N_{cmi}^2$ , respectively, so that the self-resonant frequency of the inductor becomes

$$f_r = \frac{N_{cmi}}{2\pi\sqrt{L_{cm}^*C_{cm}^*}} \tag{36}$$

As can be seen, the use of multiple inductors increases the resonant frequency. However, the terminations can lead to a larger system at some point.

#### **VIII. VALIDATION STUDIES**

In order to validate the results, the common-mode capacitance of five common-mode inductors was measured. The relevant parameters of each inductor is listed in Table 1. Inductors D193, D10, and D144 were each rated for a differential mode current of 50 A; Inductors D150 and D121 were rated for a differential mode current of 12.8 A. Also, Inductors D193, D150, D10, and D144 are UR-core based; Inductor D121 is C-core based. A photograph of common mode inductor D10 appears in Fig. 12.

In each case, the common mode inductance is determined by performing a small-signal frequency response. To this end, an impedance analyzer is connected to the common mode inductor as configured in Fig. 7. Then, from the frequency response, the parameters are fit to the equivalent circuit shown in Fig. 13. Therein,  $C_{cm,m}$  and  $L_{cm,m}$  denoted the measured values of common mode capacitance and inductance. The series and parallel frequency dependent resistances  $R_{s,m}$ and  $R_{p,m}$  represent winding and core losses respectively.

The resistances are assumed to vary as

$$R_{s,m} = R_{so} \left( \omega / \omega_b \right)^{n_s} \tag{37}$$

Parameter	D193	D150	D121	D10	D144
$d_s$ (cm)	8.48	6.18	n/a	5.41	7.56
$w_s$ (cm)	3.86	1.97	n/a	3.76	2.67
$d_w$ (cm)	16.5	11.9	10.70	10.32	14.62
$w_w$ (cm)	1.03	0.66	1.18	0.94	0.43
$d_c(\mathrm{cm})$	1.60	1.00	n/a	2.37	2.47
$r_c$ (cm)	1.39	1.21	n/a	2.03	1.76
$r_{wi}$ (cm)	1.79	1.41	1.00	2.43	2.16
$r_{wo}$ (cm)	2.82	2.06	2.18	3.36	2.59
$w_{cmc}$ (cm)	n/a	n/a	2.75	n/a	n/a
$l_{cmc}$ (cm)	n/a	n/a	2.75	n/a	n/a
$W_{clr}$ (cm)	n/a	n/a	2.75	n/a	n/a
$l_{clr}$ (cm)	n/a	n/a	2.75	n/a	n/a
$N_{sc}$	2	1	2	1	1
$N_l$	3	3	1	2	1
N	33	78	23	22	16
$r_{sc}$ (mm)	1.63	1.03	0.58	2.1	2.1
$t_{si}$ (µm)	50	50	50	50	50
$\mathcal{E}_{si}$	$3.54\varepsilon_0$	$3.54\varepsilon_0$	$3.54\varepsilon_0$	$3.54\varepsilon_o$	$3.54\varepsilon_o$
$\mathcal{E}_{ei}$	$\mathcal{E}_0$	$\mathcal{E}_0$	$\mathcal{E}_0$	$\mathcal{E}_0$	$\mathcal{E}_0$
$\boldsymbol{\mathcal{E}}_{b}$	$3.14\varepsilon_o$	$3.14\varepsilon_o$	$2.4\varepsilon_0$	$3.14\varepsilon_o$	$3.14\varepsilon_o$
$oldsymbol{arepsilon}_{lli}$	$3.7\varepsilon_0$	$3.7\varepsilon_0$	n/a	$3.7\varepsilon_0$	n/a
$t_{lli}$ (µm)	762	127	n/a	760	n/a
$t_{lc}$ (µm)	0	0	0	0	0

#### TABLE 1. Inductor parameters.



FIGURE 12. Common mode inductor D10.

and

$$R_{p,m} = R_{po} \left( \omega / \omega_b \right)^{n_p} \tag{38}$$

where  $\omega$  is the radian excitation frequency and  $\omega_b = 1$  rad/s. Since  $R_{s,m}$  and  $R_{p,m}$  are series and shunt with respect to the inductance, the losses associated with both (37) and (38) both increase with frequency.

The circuit parameters (Fig. 13) may be vectorized as

$$\Theta = \left[ L_{cm,m} \ C_{cm,m} \ R_p \ n_p \ R_s \ n_s \right]$$
(39)



FIGURE 13. Common mode inductor equivalent circuit.



FIGURE 14. Common mode inductor D10 frequency response.

TABLE 2. CMI CM capacitance.

\_

Parameter	D193	D150	D121	D10	D144
$C_{cc,c}(\mathrm{pF})$	6.72	7.54	2.26	2.98	2.20
$C_{cr,c}$ (pF)	2.10	2.50	5.26	4.16	20.8
$C_{tt,c}$ (pF)	0.488	0.123	0.680	1.01	1.18
$C_{ll,c}$ (pF)	62.0	86.4	n/a	49.0	n/a
$C_{cm,c}$ (pF)	71.3	96.6	8.20	57.1	24.2
$C_{cm,m}$ (pF)	76.5	107.3	10.5	54.6	25.3
$L_{cm,m}$ (mH)	42.8	41.5	27.7	41.3	12.8
C error (%)	6.80%	9.97%	21.9%	4.58%	4.35%
RF error(%)	3.58%	5.39%	13.2%	2.21%	2.25%

and are calculated as

$$\Theta = \arg\min\left(\sum_{i} \left|\frac{Z_{m,i} - Z_{p,i}(\Theta)}{Z_{m,i}}\right|^2\right)$$
(40)

where  $Z_{m,i}$  is the measured impedance at radian frequency,  $\omega_i$ , and  $Z_{p,i}(\Theta)$  is the predicted impedance at that frequency based upon the parameter values (40) and the equivalent circuit shown in Fig. 13

Fig. 14 illustrates the measured and fitted impedance for common mode inductor D10. As can be seen, the magnitudes and phases correspond well. In the final trace, the series and shunt resistances are shown.

Table 2 depicts a comparison between measured and predicted inductor capacitance. Therein, the ',c' in a subscript indicates calculated value, and the ',m' indicates the measured value obtained from (40). The relative contribution of each form of capacitance can be seen. The final two rows depict the percent error in the total calculated common mode capacitance, and the corresponding error in the resonant frequency as defined by (33). The capacitance is underestimated in most cases. This is expected, since stray capacitance will increase the total capacitance. Despite this, the error in the predicted resonant frequency (RF) is reasonable.

# IX. COMMON MODE INDUCTOR OPTIMIZATION

In order to demonstrate that the proposed capacitance is appropriate for optimization based design, the proposed capacitive analysis is used in the multi-objective optimization-based design of a common mode inductor for a 1 kV, 50 kW solar photovoltaic converter system [15]. While a comprehensive formulation of the inductor design will be presented in a forthcoming paper, this study demonstrates the intended use of the model.

Three studies were performed. In each study, the design variables included the airgap, depth of core base, post width, coil-to-coil clearance, layer-to-layer insulating paper type and thickness, conductor cross section, strands per conductor, number of turns, maximum number of turns per layer, ferrite material, and heat sink fin height. The metrics to be minimized were the circumscribing volume and loss. Constraints included the maximum allowed mass, maximum height, maximum flux density, minimum resonant frequency, maximum current density, maximum peak common mode current, maximum rms common mode current, maximum winding temperature, maximum bobbin temperature, and maximum core temperature.



FIGURE 15. Pareto-optimal fronts.

In Study 1, the resonant frequency was left unconstrained. In Study 2, the minimum resonant frequency was set to 100 kHz. In Study 3, two inductors in series were considered in lieu of one with the same constraint on resonant frequency as in Study 2. For this case, the value of volume and loss plotted includes both inductors. The resulting Pareto-optimal fronts are depicted in Fig. 15. It may be seen from the figure that a resonant frequency constraint results in higher loss for an equal circumscribing volume design. The resonant frequency constraint creates pressure to reduce capacitance. One way to do this is the introduction of layer-to-layer insulation, but this increases the thermal resistance from the coil interior to air, and this in turn results in a larger inductor.

As discussed, the use of multiple inductors is advantageous in terms of achieving a high resonance frequency. However, there is also an effect that for the same loss one inductor can be made to be smaller than two in series [16]. For the specifications used herein, the size penalty of two inductors outweighed the advantage in lowering the capacitance. Had the required resonant frequency been higher, this may have not been the case.

Computationally, each study took approximately 1.25 hours using an 8 core Dell Precision T5610 with Intel® Xeon® E5-2687W v2 @ 3.4 GHz running Windows 7 and Matlab 2016a. The primary computational aspect was the magnetic-electrical-thermal analysis; the contribution of the capacitance calculation to the total runtime was inconsequential.

## X. CONCLUSION

This paper has set forth a means of computing the capacitance of two classes of common mode inductors. Specific aspects of the calculation were validated through FEA; total capacitances were validated experimentally using five different inductors. Means of reducing capacitance using series connected inductors were explored, and the use of the capacitance calculation in a multi-objective optimization based design was demonstrated. Details of the latter aspect of the work will be set forth in future publications.

# REFERENCES

- W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage current calculation for PV inverter system based on a parasitic capacitor model," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8205–8217, Dec. 2016.
- [2] A. Massarini and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 671–676, Jul. 1997.
- [3] S. D. Sudhoff, "Power magnetic devices: A multi-objective design approach," in *IEEE Press Series on Power Engineering*. Piscataway, NJ, USA: IEEE Press, 2013.
- [4] J. Cale, S. D. Sudhoff, and R. R. Chan, "Ferrimagnetic inductor design using population-based design algorithms," *IEEE Trans. Magn.*, vol. 45, no. 2, pp. 726–734, Feb. 2009.
- [5] G. M. Shane and S. D. Sudhoff, "Design paradigm for permanent-magnetinductor-based power converters," *IEEE Trans. Energy Convers.*, vol. 28, no. 4, pp. 880–893, Dec. 2013.
- [6] B. N. Cassimere and S. D. Sudhoff, "Population-based design of surfacemounted permanent-magnet synchronous machines," *IEEE Trans. Energy Convers.*, vol. 24, no. 2, pp. 338–346, Jun. 2009.
- [7] B. Zhang, S. Sudhoff, S. Pekarek, and J. Neely, "Optimization of a wide bandgap based generation system," in *Proc. IEEE Electric Ship Technol. Symp. (ESTS)*, Arlington, VA, USA, Aug. 2017, pp. 620–628.
- [8] G. Grandi, M. K. Kazimierczuk, A. Massarini, and U. Reggiani, "Stray capacitances of single-layer solenoid air-core inductors," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1162–1168, Sep. 1999.
- [9] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "Three-phase common mode inductor design and size minimization," in *Proc. IEEE Transp. Electrif. Conf. Expo*, Dearborn, MI, USA, May 2016, pp. 1–8.

- [10] A. Massarini, M. Kazimierczuk, and G. Grandi, "Lumped parameter models for single-and multiple-layer inductors," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 1996, pp. 295–301.
- [11] S. W. Pasko, M. K. Kazimierzuk, and B. Grzesik, "Self-capacitance of coupled Toroidal inductors for EMI filters," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 2, pp. 216–223, Apr. 2015.
- [12] M. Kovacic, Z. Hanic, S. Stipetic, S. Krishnamurthy, and D. Zarko, "Analytical wideband model of a common-mode choke," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3173–3185, Jul. 2012.
- [13] A. D. Brovont and S. D. Pekarek, "Derivation and application of equivalent circuits to model common-mode current in microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 297–308, Mar. 2017.
- [14] H. A. Haus and J. R. Melcher. (2018). Electromagnetic Fields and Energy. [Online]. Available: http://web.mit.edu/6.013\_book/www/ chapter4/4.6.html
- [15] A. Singh *et al.*, "Development and Validation of a 20C based 50-kW Grid-Connected PV Inverter," in *Proc. IEEE Energy Convers. Congr. Expo*, Sep. 2018, pp. 23–36.
- [16] S. D. Sudhoff and R. Sahu, "Metamodeling of rotating electric machinery," *IEEE Trans. Energy Convers.*, vol. 33, no. 3, pp. 1058–1071, Sep. 2018.



**HARSHITA SINGH** received the B.E. degree in electrical engineering (EE) from the PEC University of Technology, India, in 2014, and the M.S. degree in electrical and computer engineering from Purdue University, in 2017, where she is currently pursuing the Ph.D. degree in EE. Her research work focuses on the design of magnetic components for naval systems.



**VEDA SAMHITHA DUPPALLI** (S'13) was born in Hyderabad, India, in 1991. She received the B.E. degree in electrical engineering from the Birla Institute of Technology and Science, Pilani-Hyderabad, India, in 2013, and the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2018. Since 2018, she has been with Cummins Inc., Fridley, MN, USA. Her research work includes modeling high-frequency effects in magnetic com-

ponents, genetic algorithm-based optimization, inverter filter design, and DC-DC converter modeling.



**SCOTT D. SUDHOFF** received the B.S. (Hons.), M.S., and Ph.D. degrees in electrical engineering from Purdue University, in 1988, 1989, and 1991, respectively. He is currently the Michael and Katherine Birck Professor of electrical and computer engineering with Purdue University. His research interests include electric machinery, power electronics, marine and aerospace power systems, applied control, and evolutionary computing. Much of his current research focuses on

genetic algorithms and their application to power electronic converter and electric machine design.



**ROBERT R. SWANSON** received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2011 and 2013, respectively. He is currently a Staff Research Engineer with the School of Electrical and Computer Engineering, Purdue University. His research interests include power electronics and electric machines.

• • •