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PMU Multilevel End-to-End Testing to Assess Synchrophasor Measurements During Faults

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ABSTRACT This paper introduces a framework for comprehensive testing and evaluation of the phasor measurement units (PMUs) and synchrophasor systems under normal power system operating conditions, as well as during disturbances such as faults. The evaluation is suggested to be accomplished using three different testing approaches, namely, type testing, application testing, and end-to-end testing, for each of which, systematic characterization of the hardware and software modules is presented in detail. Through the proposed approach of PMU testing in a controlled environment and detailed analysis of different estimation techniques used in PMU algorithms, one can gain insights on which estimation technique is most accurate for a certain end-use application. This hypothesis has been validated through series of realistic test scenarios on a 23-bus system running on an Opal Real Time simulator using the hardware-in-the-loop interface. In addition, the impact of synchrophasor estimation errors and their propagation from the PMU toward the end-use applications has been quantified for a fault location algorithm that uses only PMU measurements.

INDEX TERMS Application testing, calibration, end-to-end testing, fault location, hardware-in-the-loop (HIL), phasor measurement unit (PMU), synchrophasor, type testing.

I. INTRODUCTION

Significant research efforts on the use of PMUs in power systems have been reported in the literature, particularly on the Wide Area Measurement Systems (WAMS) for monitoring, control, and protection applications [1]–[6]. IEEE Standards Association has issued several standards and guidelines providing information on how to test and safeguard mission-critical infrastructure such as PMUs and Phasor Data Concentrators (PDCs) [7]–[13]. Accordingly, a standard-compliant PMU should meet all the steady state and dynamic performance requirements in IEEE standard 37.118.1a [9]. *Type-Tests* are conducted in a controlled environment where the PMUs are exposed to *known* input waveforms defined in the IEEE standards. Many organizations, national agencies, and researchers have developed calibration and testing facilities for performance evaluation of PMUs and PMU-embedded devices (e.g., relays and recorders) according to standard requirements [14]–[23]. For instance, a team at the Bonneville Power Administration (BPA) in collaboration with the Pacific Northwest National Laboratory (PNNL) was involved in testing the PMUs in laboratory and field environments under both static and dynamic conditions [14], [15]. Complementary to field evaluations [14], PMU responses to the dynamic *Type-Test* inputs generated in the laboratory environment was also tested at BPA [15]. In [16], several issues related to PMU measurements under transient conditions were discussed and procedures for PMU testing under such scenarios were proposed. The National Institute of Standard and Technology (NIST) developed an advanced calibration facility for testing PMUs according to the latest IEEE standards [17]. Furthermore, PMU testing laboratories have been developed and used to evaluate PMUs in Brazil [18], China [19], Europe [20], Canada [21], and in USA [22]–[24].

While compatibility of commercial PMUs with the IEEE standard C37.118.1a-2014 is expected, calibration laboratory tests reveal noticeable inconsistencies among the measurements obtained by PMUs from various manufacturers due to different phasor estimation techniques [14], [15]. Our paper

recognizes that such performance irregularities necessitate careful assessment of measurement errors not only under the standard-defined *Type-Test* conditions, but also the real-world scenarios encountered in the field. Consequently, a framework for implementing *Application Tests* is defined and an advanced analytical platform for such testing procedures is developed. The proposed test toolset enables analyzing the performance of different design alternatives in a standalone PMU (e.g., length of phasor estimation windows, type of filtering windows, reporting rates, etc.). Furthermore, once the PMUs are deployed in the field along with other assemblies (e.g., GPS receiver, PDCs, and communication gear) feeding various end-use applications, there is no guaranty that the integrated system would work properly. Hence, a test procedure for end-to-end performance evaluation of the overall synchrophasor system spanning from the PMUs to the applications is also suggested and implemented in this paper.

The contribution of this work is threefold: 1) A highly accurate test toolset is developed for testing not only the standalone PMU devices but also the PMU when incorporated in the end –to –end system. 2) Assessment is accomplished under both, standard known inputs as well as under fault conditions. 3) Proposed hypothesis that performance results of PMU under type testing will well predict the behavior of PMUs under the real-world field scenarios is confirmed.

The paper is structured as follows: Section II introduces the background on the various PMU testing techniques; Section III and Section IV, respectively, present the developed toolset, implementation procedure, and performance evaluation for PMU *Type-Testing* in laboratory environment and *Application Testing* under fault conditions using HIL infrastructure. Through a developed end-to-end testing platform, the performance of a selected fault location algorithm using PMU data is fully evaluated in Section V. Section VI finally summarizes contributions and provides conclusions.

II. TESTING PARADIGMS FOR SYNCHROPHASOR SYSTEMS

Typical synchrophasor systems are quite complex with multiple components (GPS receivers, PMUs, PDCs, etc.) influencing the performance and accuracy of the end-use applications. This signifies a need for multilevel testing and evaluation of the PMU measurements. Fig. 1 depicts the proposed synchrophasor testing framework. The measurement evaluation is accomplished in three layers: *type* testing, *application* testing, and *system end-to-end* testing.

- *Type-Tests* are conducted in a calibration laboratory environment where the PMUs are exposed to known signal patterns defined in the IEEE standard 37.118.1a and the PMU response to such static and dynamic patterns is assessed. Comprehensive evaluation of PMUs assesses performance of different design alternatives such as length of the phasor estimation windows, type of the filtering windows (i.e., Raised Cosine, Hamming, Flat-Top, Blackman, etc.), reporting rates, etc. by subjecting PMUs to known waveforms. Our hypothesis is that such testing will reveal the performance of a PMU design and well predict the response under the real-world field scenarios.
- *Application-Tests* are conducted to evaluate the PMU performance under faults and other disturbances in power systems. At this stage of testing, the performance of the stand-alone PMU device is evaluated when PMU is exposed to a set of input waveforms from the field. In our example, various fault scenarios are generated and the PMU under test is exposed to faulty signals with no pre-set waveform characteristics. Phasor estimates and frequency measurements of the DUT are compared with those estimated from the reference PMU (with very accurate algorithm). Accuracy of the reference algorithm was confirmed in the calibration laboratory and the estimation error is at least one order of magnitude better than standard requirements (TVE<0.0x %) which makes this algorithm valid reference even under the unknown inputs. Our proposed hypothesis is that such tests will reveal additional, rather unknown, performance characteristics that are crucial for the overall application assessment, nevertheless still in alignment with the results acquired for the type-tests.
- *System End-to-End Tests* are conducted by feeding the end-use synchrophasor applications with the measurements from real PMUs and quantifying the impact of measurement errors on the application of interest (e.g., fault location in the example we used).

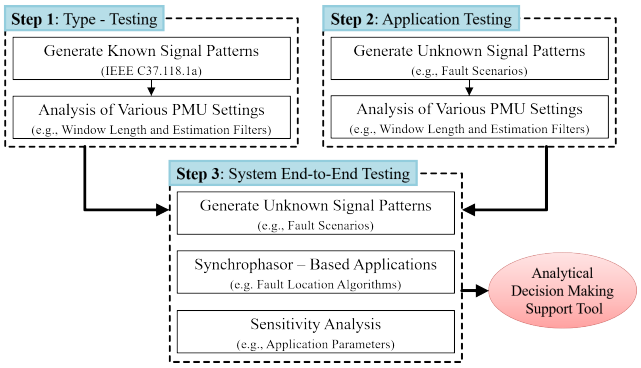

FIGURE 1. Proposed architecture for multilevel testing of synchrophasor systems.

III. TYPE-TESTING FOR PMU PERFORMANCE ASSESSMENT AGAINST STANDARD REQUIREMENTS

A. TESTING METHODOLOGY

Type-Testing of the PMUs involves (a) exposing them to known input signals generated according to IEEE standards reflecting static and dynamic conditions and (b) evaluating the PMU errors according to the standard. The static *Type-Tests* include the magnitude and frequency sweep, harmonic distortion, out-of-band (OOB) inter-harmonic distortion, as well as latency tests, in which all signal parameters (i.e., magnitude, phase angle and frequency) possess constant

values during the testing period. Dynamic *Type-Tests* include the frequency ramping, modulation and step change in both magnitude and phase angles [10]. In particular, the *Type-Test* implementation is done based on mathematical signal models defined in the standard using very accurate signal generators to replay the generated waveforms into the device under test. The measurements acquired from the device under test are compared against the true phasor values derived from the signal model as specified in the relevant standard.

According to the IEEE C37.118.1 Standard [7], metrics used for PMU performance evaluation at this stage of testing are Total Vector Error (TVE), Frequency Error (FE), and Rate of Change of Frequency Error (RFE). TVE is defined as the deviation of the synchrophasor estimates from the reference true values and contains errors in both magnitude and phase angles that should not exceed 1% across a set of tests [7]. The FE and RFE are defined as the absolute values of the estimated frequency (Hz) and rate of change of frequency (Hz/s) deviation from the true values at the same time instant.

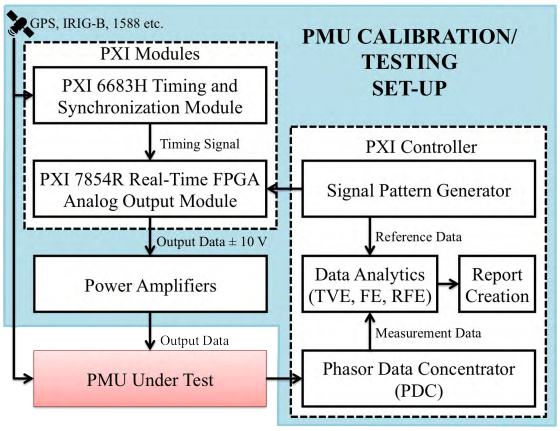

FIGURE 2. The developed PMU calibration and automated testing set up.

B. CALIBRATION AND TESTING LABORATORY SET-UP

In order to implement the PMU *Type-Tests*, a synchrophasor testing and calibration set-up is developed using the National Instrument (NI) PXIe-1062Q Chassis equipped with the following PXI boards: (a) PXIe-8105n 2.0 GHz Dual Core controller; (b) PXI-6683H Synchronization module, and (c) PXI-7854R FPGA-based IO module; all controlled in graphical system design software platform, LabVIEW. Full testing of PMUs on 50/60Hz for each reporting rate defined in the IEEE standard [7] and considering various PMU communication protocols is automated. Functional architecture of the implemented test set-up is depicted in Fig. 2. Using the PXI controller, signal pattern generator calculates the waveform parameters according to the IEEE C37.118.1 std. definitions [7]. Parameters are then transferred to the Virthex-5 LX110 FPGA board and six voltage and current waveforms are generated using the PXI-7854R analog I/O module equipped with eight 16-bit digital-to-analog converters (DACs). Generated waveforms are low-level signals (±10V) with a sampling rate controlled with 40MHz clock that are amplified to a given nominal value ($70V_{rms}$ for three phase voltage and $5A_{rms}$ for the current signals). Synchronization and time alignment with respect to the Coordinate Universal Time (UTC) of all modules are ensured in the calibration system through the PXI 6683H module with the accuracy of higher than 100 ns. PMU measurements are then directed over Ethernet or Serial communication ports back to the PXI system, where they are parsed in a local PDC developed on the PXI controller. Received measurements are compared against the reference values and the TVE, FE and RFE performance metrics are calculated. Values of the reference phasors are compensated, through compensation factors, to take into account the influence of the hardware response (signal generator and power amplifiers) and correspondingly the induced errors.

C. QUALITY ASSESSMENT OF THE CALIBRATION SET-UP

To ensure the validity of the testing and calibration procedure, systematic characterization of the testing hardware and software modules is carried out in all stages of testing. Overall accuracy of the calibration system depends on (a) the accuracy and stability of the timing reference, and (b) the ability to curtail the angle and magnitude uncertainties in the generated waveforms. Impact of uncertainties in the developed signal generation and synchronization modules is carefully studied and the results are presented as follows:

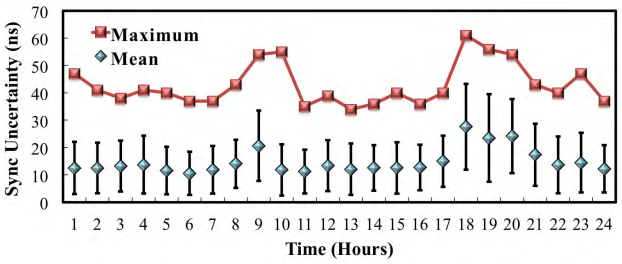

FIGURE 3. Synchronization error of the calibration system over a 24-hour period.

1) TIMING REFERENCE

with the onboard temperature-compensated crystal oscillator (TCXO) that can be disciplined with the GPS source, 6683H module allows the long-term stability of the real time calibration system. We evaluate the quality of the timing reference by measuring the maximum synchronization error with respect to the UTC reference over a 24-hour period. Fig. 3 reflects the maximum uncertainty and the corresponding mean and standard deviation. It can be seen that the maximum uncertainty over the entire range of measurements is limited to 60 ns, which in turn, causes a maximum phase angle error of less than 1.3 *mdeg*. for the reference system.

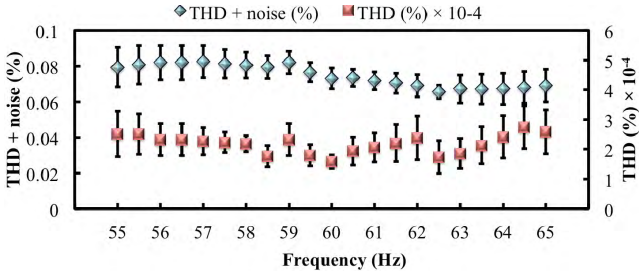

FIGURE 4. Total Harmonic Distortion (THD) of the test waveforms over a frequency range of 55-65 Hz.

FIGURE 5. Signal to noise distortion ratio (SINAD) (dB) over the set of *Type-Tests* defined in the IEEE standard for M-class PMUs.

2) SIGNAL GENERATION

we used two metrics to assess the power quality of the generated waveforms: (a) total harmonic distortion (THD) over the first 50 harmonics, and (b) signal to noise and distortion ratio (SINAD). Measurements are taken using the very accurate oscilloscope [25] equipped with a software for power quality assessments and interfaced with the testing software module where the metrics are assessed. For THD evaluation, the nominal frequency is swept in the range from 55 to 65 Hz (for nominal system frequency of 60Hz), while keeping the voltage/current values at nominal ($70V_{rms}/5A_{rms}$, respectively). According to Fig. 4, observations revealed that the THD is independent of the nominal frequency and is limited to 4e-4%, which is two orders of magnitude better than specified in the standard. Furthermore, we evaluated the quality of the generated signals by measuring the THD with noise. Similarly, the results confirmed the accuracy of the designed calibration set-up for PMU testing, and that the impact of the THD is negligible. Next, the SINAD metric is calculated as presented in Fig. 5. One can see in Fig. 5 that the SINAD keeps around 70 dB for all tests performed, but the harmonic distortion and OOB interference tests where the interfering components with magnitude equal to 10% of the fundamental are added to the fundamental component.

3) MAGNITUDE AND PHASE ANGLE ERROR

As mentioned before, the reference synchrophasors are derived from the mathematical models defined in the IEEE C37.118.1 std. [7]. The ''true'' values are compared against the oscilloscope measurements and the offsets, resulting from the DAC and power amplifier responses to generated signals, are compensated in the calibration system software module.

D. PMU SETTINGS AND PHASOR ESTIMATION FUNCTIONS

A PMU device may offer the user a possibility to change the estimation algorithm parameters such as the length of the estimation window (WL), type of filtering window, reporting rate, etc. The filters used in the PMUs may seriously affect the accuracy of the output estimates by introducing magnitude attenuation and phase offset [26]. In this study, the PMU under test has a built-in setting allowing the user to select between four windowing functions, namely the Raised-Cosine, Flat-Top, Hamming, and Blackman.

Selecting the most appropriate settings for synchrophasor measurement depends on the target end-use application, which involves a compromise on the filter characteristic (e.g. bandwidth, the amplitude accuracy, and the decrease rate of the *spectral leakage* into other frequencies). Additionally, WL influences the frequency response of the functions as well. As WL increases, the main-lobe narrows, providing a better frequency resolution with no impact on the side-lobes, but at the same time introduces the additional delay in estimate.

The PMU device under test has an option to choose WL from set of {1,2,3,4,5,6} cycles of fundamental frequency. Furthermore, the reporting rate of the synchrophasor estimates is selected by taking values from a set of {10,12,15,20,30,60} frames per second (fps) as required by the IEEE standard when considering a nominal frequency of 60 Hz. Depending on the selected value, coefficients of the filter functions vary which in return influence the overall performance of the PMU.

E. TYPE-TESTS RESULTS AND DISCUSSIONS

Full set of static and dynamic *Type-Test*s according to the IEEE C37.118.1 Std. [7] and following the test procedures defined in the IEEE Test Suit Specification [10] is carried out considering various settings for the PMU under test. In order to assess the impact of different settings, only one parameter was changed at a time while the rest remained unchanged. Fig. 6 illustrates the sample results of one static (i.e., out-of-band test) and one dynamic *Type-Test* (i.e., frequency ramping test). The selected settings of the PMU under test for the presented results in Fig. 6 are given in Table 1. The PMU is evaluated applying the requirements for the M performance class. For the OOB compliance test, frequency of the fundamental power signal is set equal to the system nominal frequency; measurements are not evaluated in the ''excluded frequency range'', defined as the nominal frequency half of the reporting rate (i.e., 30-90 Hz). Frequency ramping compliance for the M-class PMU is executed with the ramp of frequency applied to three phase balanced input signals in the range of ±5 Hz, with the rate of 1 Hz/s.

The TVE and FE metrics evaluated for four different window functions reveal a significant difference in their performance while exposed to test signals. The Raised-Cosine is attributed the worst performance in all the fulfilled tests, mainly due to its low frequency resolution and the

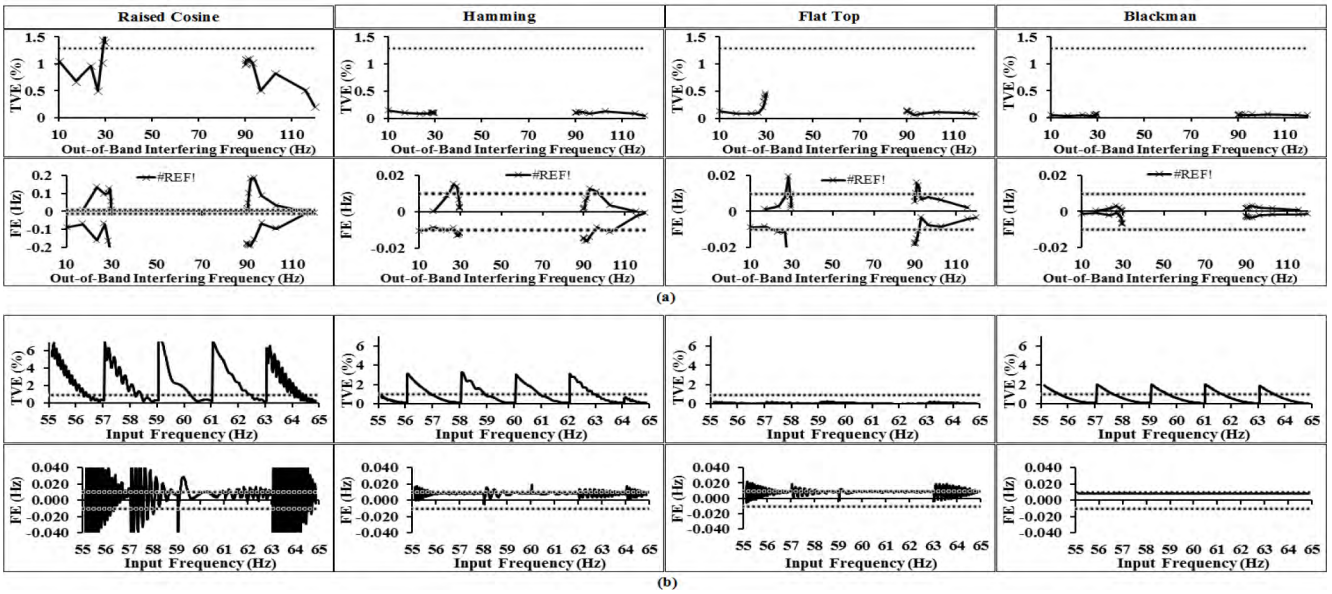

FIGURE 6. TVE and FE metrics for PMU performance assessment during the standard static and dynamic *Type-Tests*. (a) Out-of-band distortion test. (b) Frequency ramp test.

TABLE 1. Selected settings of the PMU under test.

Nominal Frequency (*Hz*)	60	Window Length (*cycles of nominal frequency*)	6
Reporting Rate (*frames per second*)	60	Window Function	Variable

lowest side-lobe attenuation. The Hamming window function revealed a better performance, but was still prone to off-nominal frequencies during dynamic tests where it violated the desired estimation error. The Flat-Top window demonstrated reasonable performance in measuring the magnitude and phase angles in all tests, while the frequency measurements were not as accurate compared to that of the Blackman window.

One can also see that decreasing the WL degrades the estimation accuracy while the phasor estimates are available faster in time. Once again, trade-offs between the required accuracy and the estimation speed should be made depending on the target application of interest. From the results obtained in this testing stage, one can foresee that a synchrophasor-based fault location algorithm based on only voltage/current estimates will have the best performance and accuracy if the Flat-Top window function is implemented in the corresponding PMU. This hypothesis will be verified in the next stages of the proposed testing framework.

IV. APPLICATION TESTS FOR ASSESING SYNCHROPHASOR ESTIMATION DURING FAULT CONDITIONS

A. FAULTS AND FAULT LOCATION IN POWER SYSTEMS

Fast and accurate fault location plays a key role in facilitating the restoration time mitigating consequences to public safety and power apparatus damage. Significant number of studies has focused on the fault location algorithms in the past, some of which are solely based on the synchrophasor measurements. A detailed review of various fault location techniques is reported in [6] and [27]. The ability of the synchrophasor-based techniques to pin-point the exact fault locations mainly relies on the accuracy of the measurements fed into the algorithms. PMU performance under such prevailing conditions needs to be judiciously investigated to ensure that the PMU measurements are accurately estimated.

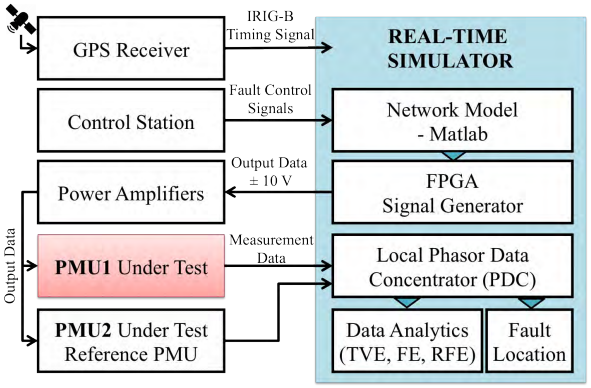

FIGURE 7. The synchrophasor testbed developed for *Application Testing*.

B. TEST-BED INFRASTRUCTURE FOR APPLICATION TESTS THROUGH HIL

The Synchrophasor Testbed has been used for conducting the *Application Tests* as well as *System End-to-End Tests*.The testbed implementation is illustrated in Fig. 7. Network models are developed using the graphical system design software in MATLAB 2013a which run on a real time (RT) platform.

RT simulator is equipped with an I/O FPGA board used to generate the voltage waveforms that are amplified to the nominal level of the PMUs. PMU streams the measurements back to the simulator over fast Ethernet communications for further analysis. An external GPS receiver generates the un-modulated IRIG-B signal that is connected to simulator's spectracom card (TSync-PCIe), providing accurate time-stamps to the RT model allowing local PDC to collect and align the incoming measurements.

C. REFERENCE ALGORITHM FOR PMU PERFORMANCE EVALUATION

An undeniable challenge for PMUs is the need to preserve high and acceptable estimation accuracy, while exposed to non-ideal input signals in presence of noise, numerous power system disturbances, and imbalances. In response to such transients, loss of generation or transmission facilities, or temporal imbalance between generation and load, the system frequency may deviate from its nominal value. When a disturbance such as faults occur, different types of signal distortions (e.g., noise, harmonics, inter-harmonics, voltage sag or dip, etc.) are created and superimposed on the power grid voltage or current signals [28]. To be able to deal with such non-ideal signals, PMU has to first condition the input signal in order to separate the fundamental frequency component and then estimate its phasor using analog and digital signal processing features fairly accurately.

In contrast with the *Type-Test* procedures, where the measurements are compared against *known true values* of the input signals, *Application Tests* require a reference (i.e., more accurate) algorithm to assess the PMU measurements under faults and transients. The reference algorithm is developed via the National Instrument cRIO 9082 platform [29]. Accurate timing information required for the synchrophasor measurement is provided with GPS time stamping and synchronization module 9467 with the ns order of accuracy.

Synchrophasor applications require sampling with respect to an absolute time reference, so the data is acquired at fixed time intervals with the sampling rate of 50 kS/s. The A/D converted data with high sampling rate is sent through multistage filters, where the signal frequency is estimated followed by calculation of voltage/current phasors. Data processing is accomplished in two stages: (1) re-sampling and (2) phasor estimation. First, sampled data goes through digital low-pass filters, being decimated with factor 25, and then being sent at the rate of 2 kS/s. Next, data goes through equi-ripple Finite Impulse Response (FIR) Band-Pass Filters (BPF), with the 0.5 dB ripple in the pass band (58-62 Hz) at the 60 Hz nominal frequency, and attenuation of 55 dB in the stop band (55-65 Hz). The designed and developed filter is a 1320 order filter, coefficients of which are predefined and stored in the FPGA memory. Magnitude response of the BPF is depicted in Fig. 8.

Frequency is estimated using the sine interpolation utilizing the inverse tangent functions. Data is then re-sampled with the new estimated frequency and sent forward to the second stage where the phasors are estimated. Data passes through a two-stage low pass filter, and final corrections are compensated for the delays introduced by the signal processing. Further details on the implemented algorithm can be found in [30].

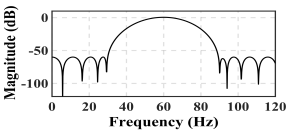

FIGURE 8. Magnitude response of the BPF in the reference algorithm.

D. ACCURACY OF THE REFERENCE PMU

Accuracy of the reference algorithm was confirmed in the calibration laboratory and its estimation error is at least one order of magnitude better than required by the standard for M-class PMUs (TVE<0.0x%). The same observations hold for the FE and RFE metrics. Comprehensive testing was carried out at each reporting rate {10,12,15,20,30,60} fps. Testing results on the reference PMU for the reporting rate of 60 fps are given in Table 2. With the achieved accuracy, it is apparent that the selected PMU algorithm is a good candidate to serve as a reference for the suggested *Application Testing*.

E. CASE STUDY AND FAULT SCENARIOS

The network used for simulating faults on transmission lines and studying the PMU responses under such conditions is a modified 23-bus model of a 500 kV transmission network with 7 generating units and 17 load points, the one-line diagram of which is illustrated in Fig. 9. The model is developed in MATLAB Simulink environment and simulated on the Opal-RT platform. The entire system is divided into three blocks, each running on separate cores, in order to achieve a fast execution with time steps of 50 us. The system behavior under different scenarios of symmetrical (three-phase) and asymmetrical (single line to ground, double line to ground, and line to line) faults is thoroughly studied. Different scenarios are fed with applied faults of diverse resistance values ranging from 0, 20 and 100 Ohms and different locations on 30%, 50% and 80% of the line length. Each fault scenario is simulated for 30 seconds. Local frequency is defined in (1), where $d\omega$ represents the rotor speed deviation.

$$f = \left(d\omega + 1\right) \cdot f_{nom} \tag{1}$$

The simulation results on the estimated frequency at the generation bus B8, when various fault types are applied on the line connecting busses B10 and B11, are depicted in Fig. 10(a). One can observe, from the simulation results in Fig. 10(a), that the frequency initially increases due to the generation-demand imbalance (load drop), and then returns to a new steady state value when the power is rerouted in an updated network topology. The worst-case scenario is during a three-phase fault when the entire demand at load points B11 and B12 is disconnected. This worst-case scenario

TABLE 2. Performance assessment of the reference PMU.

Type-Test Item	Reference PMU Under Test (@FPS=60)						IEEE Std. C37.118.1a		
	Mean Error			Maximum Error			M Class Limits (@ FPS=60)		
	TVE (%)	FE (Hz)	RFE (%)	TVE (%)	FE (Hz)	RFE (Hz/s)	TVE (%)	FE (Hz)	RFE (Hz/s)
Signal Magnitude Sweep (10%-200%)	0.0079	4.75e-5	0.0036	0.0297	2.29e-4	0.0192	1		
Signal Frequency Sweep (55-65 Hz)	0.0058	3.45e-5	0.0023	0.0163	5.70e-5	0.0032	1	0.005	0.1
Harmonic Distortion (up to 50th)	0.0045	3.00e-5	0.0026	0.0145	1.34e-4	0.0178	1	0.025	-
Out-of-Band Interference (f_0=57 Hz)	0.1033	7.1e-4	0.0374	0.1771	1.56e-3	0.1042	1.3	0.01	-
Out-of-Band Interference (f_0=60 Hz)	0.0817	4.9e-4	0.0422	0.1558	1.08e-3	0.1004	1.3	0.01	-
Out-of-Band Interference (f_0=63 Hz)	0.0581	8.5e-4	0.1210	0.1555	1.71e-3	0.1210	1.3	0.01	-
Frequency Ramp (positive; rate=1 Hz/s)	0.0063	1.54e-4	0.0078	0.0163	7.8e-4	0.0346	1	0.01	0.2
Frequency Ramp (negative; rate=1 Hz/s)	0.0171	1.57e-4	0.0079	0.0292	3.7e-4	0.0361	1	0.01	0.2
Amplitude Modulation (0.1Hz <f_{mod}< 5Hz)	0.0973	5.4e-4	0.0175	0.3418	1.46e-3	0.0474	3	0.3	14
Phase Modulation (0.1 Hz<f_{mod}< 5Hz)	0.0583	1.73e-2	0.6510	0.2497	5.82e-2	2.9877	3	0.3	14

	Response Time (sec.)			Response Time to meet limit X* (sec.)		
	TVE	**FE**	**RFE**	**TVE**	**FE**	**RFE**
Magnitude Step (10% of nominal value)	0.0259	0.0724	0.1035	0.1167	0.2333	0.2333
Phase Step (10% of nominal value)	0.0483	0.0917	0.1227	0.1167	0.2333	0.2333
X*: TVE=1%; FE=0.005Hz; RFE=0.1Hz/s (0.4 Hz/s for P-class PMU)						
PMU Reporting Latency (sec.)	0.1039			0.1167		

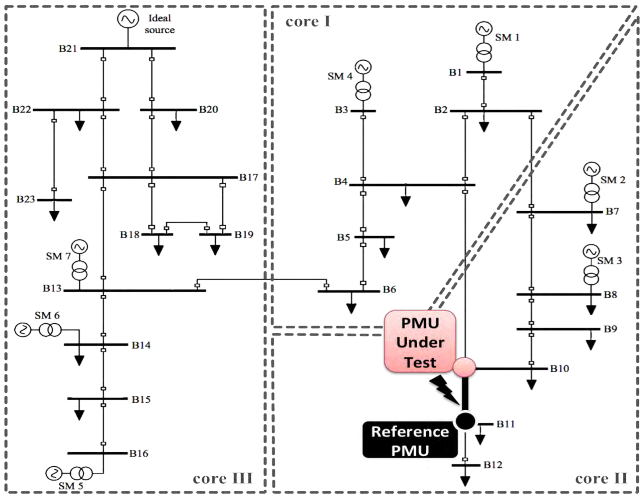

FIGURE 9. Case Study: 23-bus model of a 500 kV transmission network.

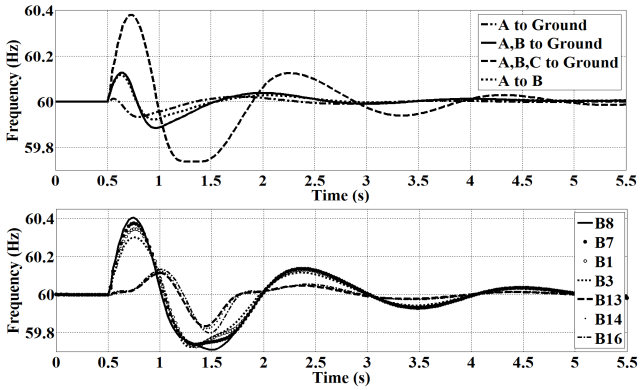

FIGURE 10. (a) Frequency measurements at bus B8 during various fault types, (b) Frequency measurements for three-phase fault on the generator buses.

reveals the maximum expected errors and, hence, is studied for assessment of the PMU estimation errors (*Application Tests*) as well as evaluating the impact on the fault location applications (*End-to-End Tests*).

F. APPLICATION TEST RESULTS AND DISCUSSIONS

Occurrence of a fault on a transmission line triggers a sudden change in the system frequency. One can see, from Fig. 10(b), that the frequency at the buses closer to the fault is more affected compared to that measured further away from the fault inception. This leads to a conclusion that the accuracy of PMU measurements located in vicinity of the fault will be more susceptible, and hence, will impose a higher risk to the trustworthiness of the end-use application outcomes.

We now investigate the performance of four different filtering functions in PMUs as well as the WL under the studied fault scenarios. The metrics used for such performance evaluation are the same as those used in *Type-Tests* and true values for comparison are taken to be measurements of the reference PMU (see Section IV.C). First, the influence of different fault types (A-G, AB-G, ABC-G and AB) as well as fault resistance on the FE and TVE metrics is investigated. According to results illustrated in Fig. 11, while variations of fault resistance (R) generally does not have a significant influence on the frequency estimation in most studied scenarios, FE increases as R increases. Its impact on the TVE is noticeable. With an increase in the fault resistance,

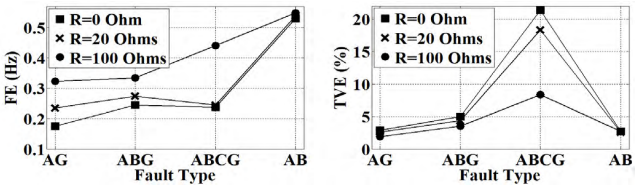

FIGURE 11. Impact of fault resistance on the FE and TVE metrics (d = 80% of line length from B10; Blackman window with length of 6 cycles).

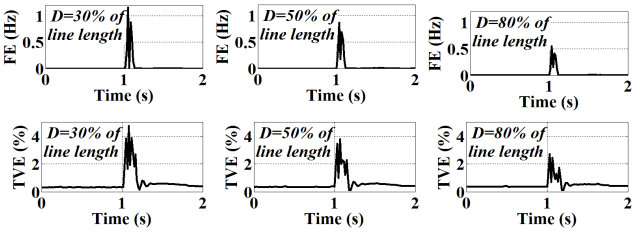

FIGURE 12. Impact of distance to the fault on the FE and TVE metrics (R = 100 Ohms; Blackman window with length of 6 cycles; AB fault).

the TVE decreases. In case of a three-phase fault, the TVE reaches its maximum among all studied scenarios, which complies with the previous observation where the highest frequency deviation from nominal value was resulted when an ABC-G fault was simulated. Conversely, the FE has its peak value for AB faults among all studied scenarios.

Next, the impact of the distance to the fault inception is studied where the faults are assumed to occur at 30%, 50% and 80% of the line. Fig. 12 demonstrates the results acquired during an AB fault, with the fault resistance of 100 Ohms. The distance to the fault from the bus where the PMU under test is located has a significant impact on the TVE metrics. The closer the fault is to the PMU location, the higher the TVE error is. The same observation is valid for FE metrics due to stronger variations in voltage/current signals closer to faults.

Most fault location algorithms use the voltage/current measurements as the input parameters; therefore, this study focuses on cases with potentially higher impacts on the TVE. For further testing, the fault is set to be closer to the PMU under test (D = 30% of the line length), with the resistance of R = 0 Ohm. Fig. 13 shows the impact of different windowing functions as the input filters. It can be seen that the best frequency estimate is achieved with the Hamming and Blackman filters, while presenting much higher TVE compared to other two filters. The Flat-Top filter has the best performance in terms of the TVE response, which closely matches the former observations in the *Type-Tests* (see Section III). The impact of the WL on the accuracy of frequency and phasor estimation is illustrated in Fig. 14. As WL increases, the higher TVE is noticed, while the FE decreases once more data samples are available for higher accuracy of the frequency estimation. In such cases, however, the measurements

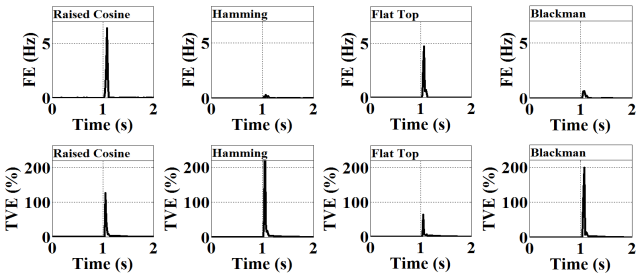

FIGURE 13. Impact of windowing functions on FE and TVE metrics; (d = 30% of line length from B10; R = 0 Ohm; ABC-G fault; window length of 6 cycles).

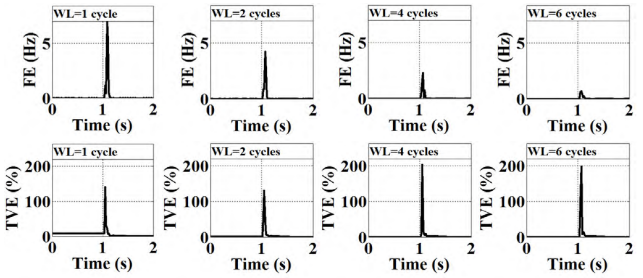

FIGURE 14. Impact of WL on the FE and TVE metrics (d = 30% of the line length from B10; R = 0 Ohm; ABC-G fault; Blackman window).

will be delayed which can be an issue for the applications that mandate a faster data update.

V. END-TO-END TESTING OF THE SYNCHROPHASOR-BASED FAULT LOCATION ALGORITHMS

Impedance based fault location algorithms can be classified into four sub-categories: single, double, multi–end, and wide area methods based on the available sources of data. A double-end fault location algorithm is investigated in this Section for *End-to-End Testing*. The studied algorithm [30] is implemented in MATLAB environment using synchrophasor measurements form real PMUs.

A. FAULT LOCATION ALGORITHM USING SYNCHROPHASOR DATA

The studied synchrophasor-based fault location algorithm employs synchronized measurements at both ends of the line. The goal is to demonstrate how to evaluate the impact of PMU response errors under fault conditions on the end-use fault location application using the HIL platforms. The studied fault location technique uses symmetrical components, specifically the negative- and positive-sequence voltage and current signals as the input. Distance to the fault is calculated in (2):

$$d\% = \frac{(V_1^+ - V_2^-)I_2^- - (V_1^- - V_2^+)I_2^+}{(V_1^+ - V_2^+)(I_1^- - I_2^-) - (V_1^- - V_2^-)(I_1^+ - I_2^+)} \times 100\% \quad (2)$$

where the following nomenclature applies:

d	Distance from Bus 1 to the fault location.
$V_{1,2}^{-}V_{1,2}^{+}$	Negative- and positive-sequence phase voltages at both terminals of the line
$I_{1,2}^{-}, I_{1,2}^{+}$	Negative- and positive-sequence phase currents at both terminals of the line.

Further details on the algorithm are available in [30].

B. END-TO-END TEST RESULTS AND DISCUSSIONS

The real PMU was exposed to a set of faulty signals while the set-up setting parameters (windowing functions and WL) were altered, so as to estimate the influence of such parameters on the accuracy of the synchrophasor measurements as well as the end-use application outcome. On studying the impact of windowing functions, the maximum error in all test scenarios appears to be during the symmetrical three-phase faults (ABC-G). The maximum error in fault location for a fault scenario with R=0 Ohm, d= 30% of the line length from bus B10, and fixed WL of 6 cycles, are tabulated in Table 3. It can be seen that the Raised-Cosine windowing function reveals the highest error in calculating the distance to the fault, mainly due to the low amplitude accuracy of the filter function. On the other hand, performance of the Flat-Top filter is most appealing for the fault location algorithm that uses voltage/current phasor estimates. However, one has to be careful in selecting the PMU settings in the field, as the Flat-Top function has a great performance for the phasor estimation while its frequency resolution is low, making the frequency estimates less accurate compared to other filters. In response to such low frequency resolution of the Flat-Top filter, one can use the Blackman filter that has a close enough phasor estimation with a more accurate frequency estimation compared to Flat-Top filters.

TABLE 3. Performance of different windowing functions on the fault location algorithm accuracy.

Filter Function	Raised Cosine	Hamming	Blackman	Flat-Top
Maximum Error (%)	3.76	3.12	1.54	0.97

TABLE 4. Impact of different windowing lengths on the fault location algorithm accuracy.

Window Length (× 16.66 ms)	1	2	4	6
Maximum Error (%)	4.14	2.05	1.78	1.54

Next, impact of the WL used for the synchrophasor estimation algorithm is studied. Four different values for the WL comprising 1, 2, 4, or 6 cycles are considered. Table 4 shows the impact of WL for the Blackman filter function and the maximum errors in the fault location estimates in case of a fault with R=0 Ohm, d= 30% of the line length from bus B10 are tabulated. It can be seen that the fault location algorithm has the highest accuracy (i.e., minimum error) in case where the WL is longer. However, the WL cannot be large as some synchrophasor applications mandate very fast measurement requirements in real time.

VI. CONCLUSION

The paper offers the following contributions:

- A comprehensive analytical toolset for automated type, application, and end-to-end testing of PMUs and synchrophasor systems is developed allowing assessment of the system-wide impact of synchrophasor measurement errors during faults.
- *Type-Testing* analysis and extensive PMU performance evaluation under standard static and dynamic test conditions is suggested, providing an early indication of the impact of the fault waveform processing options on the performance of the synchrophasor measurements.
- *Application Testing* analysis and PMU performance evaluation under faults and other prevailing conditions is implemented through a HIL testing mode, offering a realistic assessment of the PMU measurement errors in real-world field scenarios.
- *End-to-End Testing* analysis and a methodology on quantitative estimation of the impact of PMU measurement errors on trustworthiness of any synchrophasor application is proposed and illustrated, as an example, on a synchrophasor-based fault location algorithm under different fault scenarios.

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Authors' photographs and biographies not available at the time of publication.