Voltage Ripple-Based Passive Islanding Detection Technique for Grid-Connected Photovoltaic Inverters

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ABSTRACT One of the main challenges of integrating distributed generation into the power grid is islanding, which occurs when a disconnected power line is adversely energized by a local distributed generation source. If islanding is not quickly detected, it can present serious safety and hazardous conditions. Conventional passive detection techniques used today are entirely dependent on the parameters of the power system, which under certain operating conditions may fail to detect islanding. In this paper, a novel and efficient passive islanding detection technique for grid-connected photovoltaic-based inverters is presented. In this technique, the ripple content of the inverter output voltage at the point of common coupling is monitored for deviations using time-domain spectral analysis. Islanding is then detected whenever the ripple spectral content exceeds a preset threshold level for a certain period of time. The performance of this technique was extensively tested and quantified under a wide range of operating conditions. It was determined that the proposed technique did not exhibit any non-detection zone and was able to detect all types of islanding cases within 300 ms of the allowed delay time. Furthermore, the proposed technique was found to be robust and inherently immune to other degrading factors, since it is relatively independent of system parameters, power system scaling, or the number of distributed generation sources present within the islanding zone.

INDEX TERMS Anti-islanding, distributed generation, passive islanding detection, smart grid, spectral analysis.

I. INTRODUCTION

POWER grids around the world are subject to severe strain due to the increasing demand for electricity [1]. Typically, conventional power systems consist of centralized fossil-fuel plants delivering large amounts of power over long distance transmission lines [1]. Stringent environmental regulations coupled with prohibitive costs of new power plants have made distributed generation (DG) systems an attractive choice to complement the existing power system infrastructure. Furthermore, large-scale centralized power plants are prone to catastrophic blackouts since they represent a single point of failure affecting wide service areas. Due to these shortcomings, researchers and policy makers have advocated a holistic approach to integrate DG systems into the existing power system infrastructure [2], [3]. A DG unit is defined as an energy source connected to the power grid at the distribution level. Most DG units are considered

environmentally friendly since they use renewable energy that can deliver power closer to the end users [4], [5]. Solar-based DG systems are one of the most popular DG systems due to their cost-effective installation and low maintenance requirements. Moreover, photovoltaic (PV) systems are highly modular with power generation capacity ranging from few kWs to several MWs.

However, a major problem that can arise from using DG sources is the unintentional islanding phenomenon [6]. Islanding is a condition that occurs when a disconnected power line is unintentionally being fed by a DG source. Unintentional Islanding is dangerous since it can jeopardize people lives and cause damage to equipment. For instance, islanding has the potential to make the line voltage go out of synchronization with the grid. Reclosing under such conditions can cause severe damage due to high currents and large mechanical torques developed. Therefore, islanding must be

closely monitored and detected. Islanding detection is not only crucial to the operation of DG systems but also mandated by standard regulations [7], [8].

In recent years, considerable research has been conducted to develop fast and robust islanding detection techniques. These techniques are based on measuring local parameters or remote signals [9]–[12] thereby classified as local or remote techniques. Local techniques are further subdivided into passive techniques [13]–[20], active techniques [21]–[25], and neuro-computational based techniques [26]–[28]. Passive techniques monitor system parameters, such as voltage and frequency, at the point of common coupling (PCC) between the grid and the DG source. Techniques such as Over/Under voltage protection (OVP/UVP) and Over/Under frequency protection (OFP/UFP) typically detect islanding when the PCC voltage and frequency exceed a predefined threshold level [13]. Other techniques including phase jump detection (PJD) monitor the phase difference of the inverter's voltage and output current [13]. Rate of change of frequency (ROCOF) and Rate of change of power (ROCOP) are two other common parameters used to detect islanding [14]. Although passive techniques are easy to implement, they exhibit large Non-Detection Zones (NDZ) which may fail to detect islanding in case of small power mismatch [15]. Islanding may also be falsely detected due to power disturbances caused by other conditions such as capacitor switching or line faults [6]. Other techniques use modal analysis to detect islanding by extracting the waveform patterns of the different modes (frequency components) of the signal [16], [17]. In general, passive detection techniques use time domain analysis. However, frequency domain techniques were also proposed in the literature such as Wavelet transform [18], [19] and s-transform [20]. The frequency domain techniques require considerable amount of real-time computations thus, cannot be easily implemented into a DG protection scheme.

In power systems, under normal operating conditions, the amplitude of the PCC voltage is typically constant due to the stabilizing effect of the grid. However, during islanding, the absence of the grid stabilizing effect may cause the amplitude of the signal to undergo sudden and sustained fluctuations which can be used to detect islanding. In this paper, a computationally efficient passive islanding detection technique for DG grid-connected PV systems is presented. The proposed technique is based on monitoring the time domain spectral content of the ripple in the PCC voltage that can be easily implemented in the inverter circuitry. Islanding is detected whenever the ripple spectral content exceeds a preset threshold level for a certain period of time. This technique does not have NDZ limitations and is able to detect islanding even in zero power mismatch where other passive techniques fail to detect. Moreover, the proposed technique detects islanding within 300 ms and is independent of the DG system size and parameters.

The rest of the paper is organized as follows. Section II presents the inverter-based distributed generation model.

Section III discusses the proposed islanding detection technique. Section IV presents the model parameter optimization process. Section V discusses the results of the proposed islanding detection technique. Finally, the conclusions are presented in Section VI.

II. INVERTER-BASED DISTRIBUTED GENERATION MODEL

In a typical grid-connected PV system, the energy collected by the solar array is directed to the utility side through a series of electrical devices that condition and convert the DC signal into an AC signal. A single-line diagram consisting of PV panels, DC-DC boost converter, and a 3-phase inverter connected to the utility grid through a matching transformer is illustrated in Fig. 1.
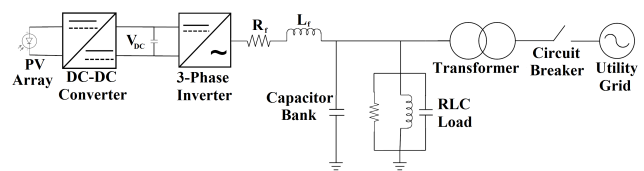

FIGURE 1. Single-line diagram of a grid-connected PV system.

In this model, the PV array is designed to generate a rated power of $100kW$ under standard operating conditions ($1000W/m^2$ irradiance at $25°C$ temperature). The array is connected to the DC-DC boost converter operating with a duty cycle controlled by a Maximum Power Point Tracker (MPPT). The MPPT algorithm used in this system is based on the "Incremental Conductance and Integral Regulator" technique that sets the output voltage for optimal operation. The boost converter is connected to the 3-phase inverter to convert DC into AC. The inverter's control system consists of two loops: 1) an external loop controlling the DC link voltage and, 2) an internal loop controlling the active (I_d) and reactive (I_q) orthogonal current components. The reference setting for the I_d component is determined by an external voltage controller while the value of the I_q component is set to zero to maintain unity power factor ($PF = 1$). The AC power output of the inverter is synchronized with the grid using a Phase Locked Loop (PLL). In this study, the islanding detection technique is implemented within the PV-based inverter and is designed to de-energize the system whenever islanding is detected. A series R-L filter with a capacitor bank is used to filter out the harmonics produced by the high frequency switching in the inverter. At the PCC, the inverter is connected to both the RLC load and a step-up transformer which is connected to the main utility. The utility grid is modeled as a 25 kV equivalent transmission system fed by a 120-kV infinite bus. To simulate islanding, a circuit breaker on the utility side is turned to the open position. The MATLAB Simulink model of this grid-connected PV system is depicted in Fig. 2 with the simulation specifications and initial settings listed in Table 1.
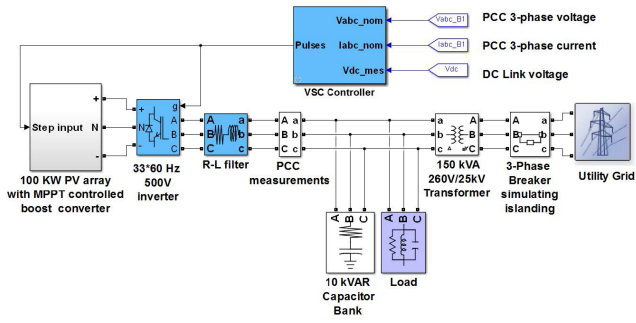
FIGURE 2. Simulink model of a grid-connected PV system.

TABLE 1. Simulation model specifications.

Parameter	Value
PV array maximum power output	100 kW
Load active power (P)	100 kW
Load quality factor (Q_F)	1
Load resonant frequency	60 Hz
DC Link Voltage (V_{DC})	500 V
Inverter switching frequency	1980 Hz
Filter resistance (R_f)	2 mΩ
Filter inductance (L_f)	0.2 mH
Transformer nominal power	150 kVA
Grid short-circuit power	2500 MVA
Grid X/R ratio	7

III. PROPOSED ISLANDING DETECTION TECHNIQUE

A novel passive islanding detection technique based on monitoring the ripple content in the instantaneous output voltage of the inverter at the PCC using time-domain spectral analysis is developed. Under steady state conditions, the output power of the PV inverter has small variations due to high switching frequencies, dead time, and DC link voltage ripple [29], [30] as shown in Fig. 3. These variations are normally absorbed
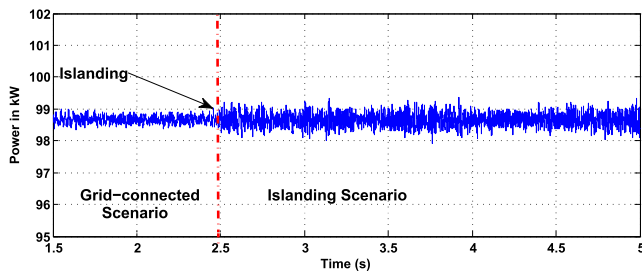

FIGURE 3. Output power of DG inverter in grid-connected and islanding scenarios.

by the grid due to its low impedance and their effect is not observed at the PCC voltage level.

The single-phase voltage V_{island} at the PCC level after islanding is mathematically expressed as [31]

$$V_{island} = V_{grid}\sqrt{\frac{P_{inv}}{3P_{Load}}} \qquad (1)$$

where V_{grid} is the root mean square (RMS) phase voltage on the utility side of the grid, P_{inv} is the 3-phase inverter

output power, and P_{Load} is the power consumed by the load.

Since V_{grid} and P_{Load} are considered constants, any power variation in P_{inv} is directly reflected in V_{island}. As shown in Fig. 4(b), sustained oscillations in V_{island} is observed when islanding occurs and is uniquely different from other disturbances under normal and fault conditions, as illustrated in Fig. 4(a) and 4(c), respectively. In case of zero power
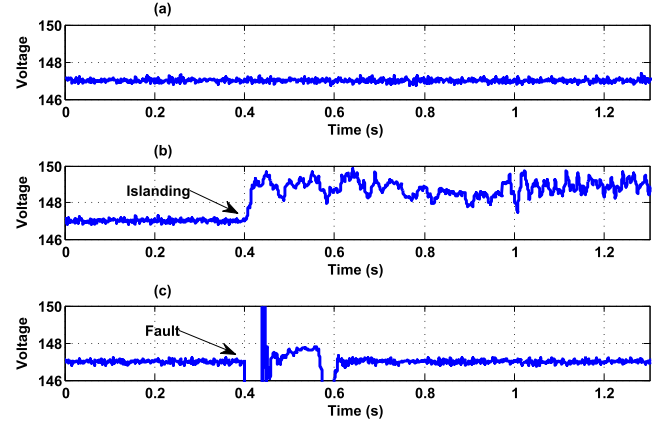

FIGURE 4. Root mean square (RMS) of single-phase voltage waveforms at PCC. (a) Grid-connected condition. (b) Islanding condition. (c) 3-phase short-circuit fault condition.

mismatch, the DG source is fully capable of delivering the load demand ($P_{inv} = P_{Load}$). In this case, conventional passive techniques will fail to detect islanding, therefore this is considered the worst case scenario in this study. For the 3-phase short-circuit case in Fig. 4(c), the fault was shown to clear within two cycles while for the islanding case, the voltage fluctuations did not diminish but persisted as shown in Fig. 4(b).

Based on these observations, the proposed technique is effectively used to detect islanding by monitoring the ripple content in the V_{island} waveform. A block diagram of this technique using Simulink is presented in Fig. 5. As shown,
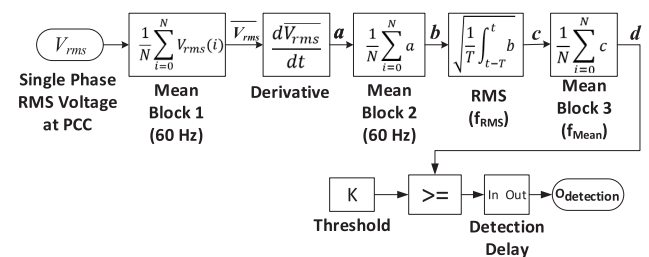

FIGURE 5. Block diagram of the proposed islanding detection technique.

the ripples in the RMS voltage waveform is first amplified by taking its derivative. The derivative signal is then passed through an RMS block to determine the ripple content of the amplified waveform and eliminate the DC component.

Three moving average lowpass filters ('Mean') blocks are used after each output stage. The first mean block eliminates

any high frequency noise above 60 Hz in the input RMS voltage, while the second eliminates any points of discontinuity in the output of the derivative block. Finally, the third mean block is used to smooth out the output of the RMS block. Fig. 6 shows the islanding detection waveform output for the three cases depicted in Fig. 4.
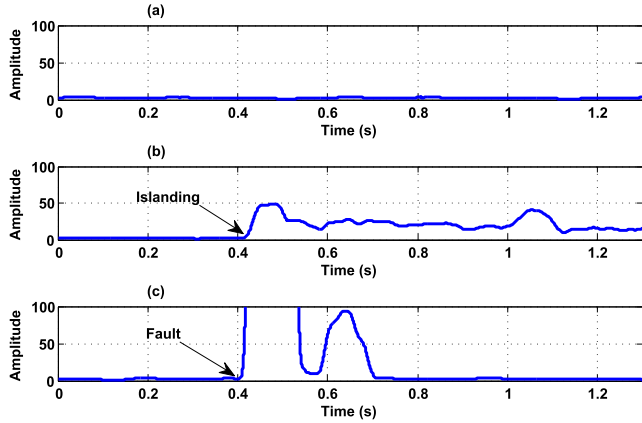

FIGURE 6. Islanding detection waveform. a) Grid-connected condition. b) Islanding condition. c) 3-phase short-circuit fault condition.

From Fig. 6, it is clear that there is a sustained difference in the islanding detection waveform before and after islanding. In the fault scenario, although there is a transient spike in the waveform, it settles down relatively fast. Therefore, a threshold was used to differentiate between the grid-connected and islanded waveforms. In addition, a time delay was introduced in the final detection stage to avoid false tripping due to transients caused by non-islanding scenarios such as faults, load-switching, capacitance switching, loss of parallel feeder, and motor starting.

Fig. 7 illustrates the waveforms at each output of the seven stages using this technique. Stage 1 shows the input waveform, which is the single phase voltage (V) at the PCC. Stage 2 shows the RMS value of V (V_{RMS}). The RMS is calculated over a moving average window of one cycle for a nominal system frequency of 60 Hz as

$$V_{RMS} = \sqrt{\frac{1}{T} \int_{t-T}^{t} V^2} \tag{2}$$

where $T = \frac{1}{60}$ s. All frequency components above 60 Hz in the V_{RMS} represent noise and are eliminated using the Mean Block 1. This has the same effect as a lowpass filter which eliminates any frequency component above 60 Hz as shown in Fig. 7 (Stage 3). The output of the filter $\overline{V_{RMS}}$ is modeled as

$$\overline{V_{RMS}} = \frac{1}{T} \int_{t-T}^{t} V_{RMS} . dt \tag{3}$$

The variations in $\overline{V_{RMS}}$ are small and need to be amplified for this technique to work. This is achieved by taking the derivative of $\overline{V_{RMS}}$ to obtain the a waveform as illustrated in Fig. 7 (Stage 4). The derivative is evaluated after for
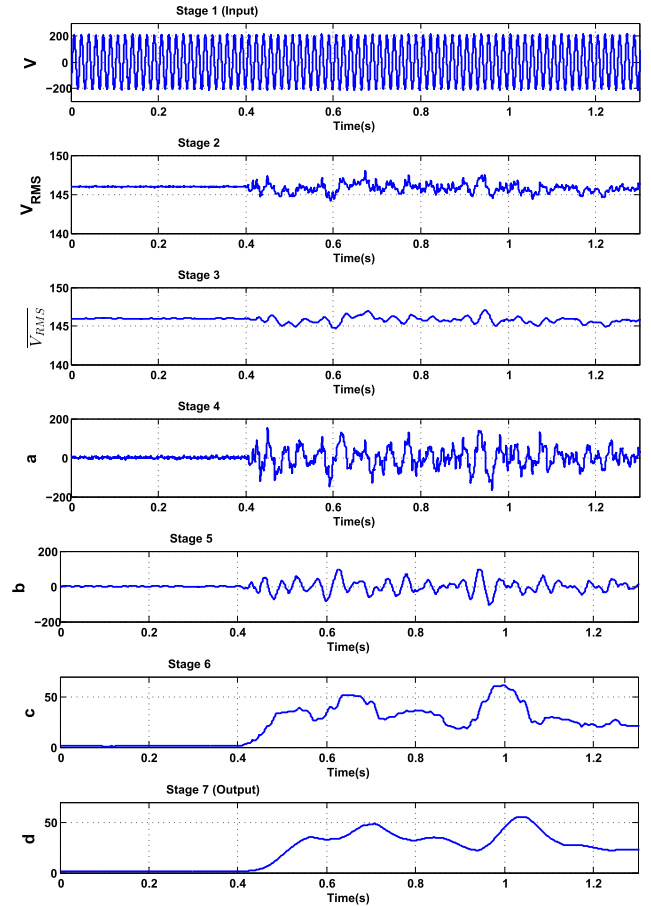

FIGURE 7. Waveforms of all the stages of the islanding detection technique.

each sample with a sampling period of 10 μs. To further improve the performance of the technique, frequency components above 60 Hz in the a waveform are eliminated using a separate lowpass filter to obtain the b waveform as shown in Fig. 7 (Stage 5). The a and b waveforms are modeled as

$$a = \frac{d(\overline{V_{RMS}})}{dt} \tag{4}$$

$$b = \frac{1}{T} \int_{t-T}^{t} a. \tag{5}$$

The RMS value of b was evaluated over a frequency cycle of f_{RMS} to obtain the c waveform. This is used to quantify the ripple content and to eliminate any DC component present within b as illustrated in Fig. 7 (Stage 6). Finally, any frequency component over f_{Mean} in waveform c is eliminated to obtain the islanding detection waveform (d) as illustrated in Fig. 7 (Stage 7). The waveforms c and d are modeled as

$$c = \sqrt{\frac{1}{T_{RMS}} \int_{t-T_{RMS}}^{t} b} \tag{6}$$

$$d = \frac{1}{T_{Mean}} \int_{t-T_{Mean}}^{t} c \tag{7}$$

where $T_{RMS} = \frac{1}{f_{RMS}}$ s and $T_{Mean} = \frac{1}{f_{Mean}}$ s.

The selection of f_{RMS} and f_{Mean} constitutes an important part of the technique design and is further discussed in Section IV. The detection waveform (d) is then compared to a predefined threshold. If d exceeds the threshold for a predefined time, then islanding is detected. Let α be the detection threshold, t_d be the predefined decision time delay, and Δt be the time interval in which d exceeds α. The islanding detection decision signal $O_{detection}$ is modeled as

$$O_{detection} = \begin{cases} 1, & \text{if } d \geq \alpha, \ \Delta t \geq t_d \\ 0, & \text{if otherwise} \end{cases} \quad (8)$$

where $O_{detection} = 1$ means islanding is detected while $O_{detection} = 0$ indicates that there is no islanding. Fig. 8 depicts the complete algorithm for the proposed technique.
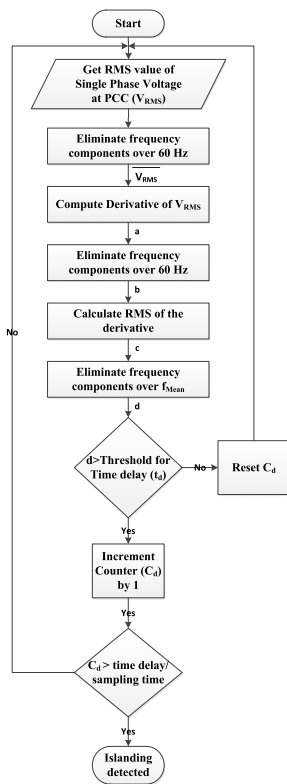

FIGURE 8. Algorithm for the proposed detection technique.

IV. MODEL PARAMETER OPTIMIZATION
The threshold and time delay for islanding detection were optimized based on thorough experimental analysis of possible islanding and non-islanding events. The factors affecting the selection procedure and the final selected values are discussed next.

A. EFFECT OF MEAN 3 AND RMS BLOCK OPERATION FREQUENCIES
The selection of the operation frequencies of the Mean 3 (f_{Mean}) and RMS blocks (f_{RMS}) constitutes an important part of the design process. The operation frequencies represent the time interval over which the RMS or Mean is calculated.

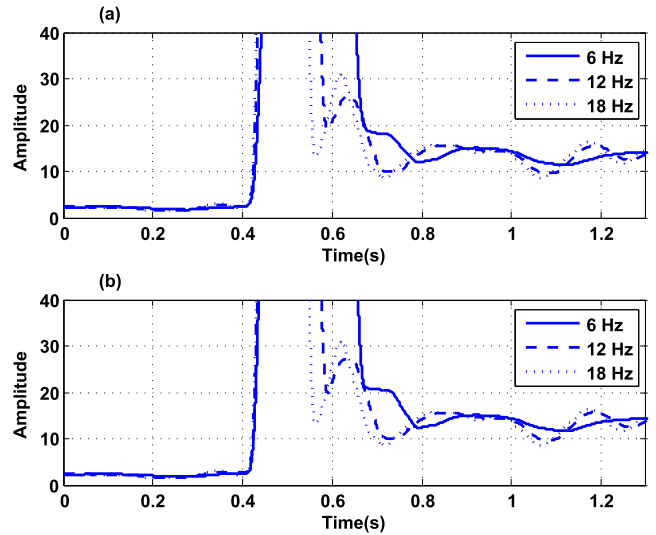Fig. 9 illustrates the effects of changing the frequency of the Mean 3 and the RMS blocks. As shown, decreasing the

FIGURE 9. Effect on islanding detection waveform when changing the fundamental frequency of (a) the Mean 3 block at f_{RMS} = 18 Hz and (b) the RMS block at f_{Mean} = 18 Hz.

frequency increases the moving average window size. This would smooth out the islanding detection waveform which increases the detection waveform level difference between islanding and grid-connected scenarios. Fig. 10 represents the changes in the detection waveform when the frequencies of both blocks are varied. As shown, there is very minimal dif-
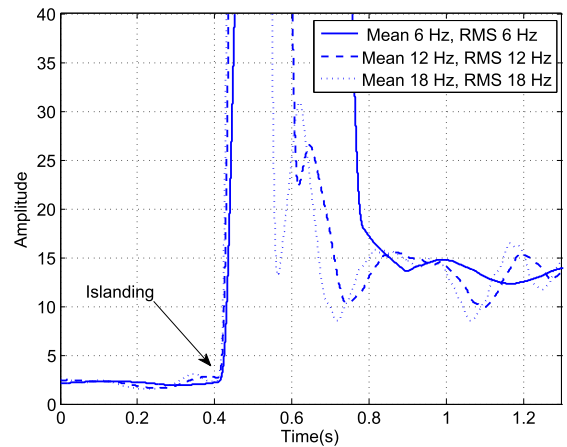

FIGURE 10. Effect of changing the fundamental frequencies of both the Mean 3 and RMS block on islanding detection waveform output.

ference in the grid-connected waveform, however the difference in the islanded waveform is significant. Although a low frequency would generate considerable difference between the grid-connected and islanded levels, it also has the effect of increasing the waveform settling time to a stable value for non-islanding events as depicted in Fig. 11. Therefore, an

optimum frequency for both blocks must be chosen to allow for an adequate difference between the islanded and grid-connected levels while maintaining a delay greater than the highest settling time recorded for non-islanding events.
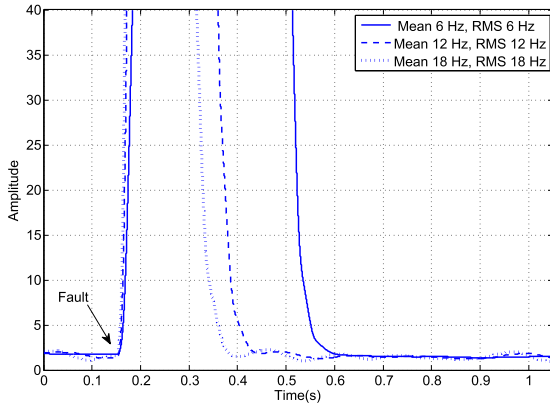

FIGURE 11. Effect of combined changing the fundamental frequencies of the Mean 3 and RMS block on settling time delay after the 3-phase fault scenario.

B. EFFECT OF QUALITY FACTOR

The effect of changing the load quality factor (Q_f) on the detection waveform was also investigated. Q_f is defined as the ratio of the reactive power consumption to the rated power output of the DG inverter. IEEE standards require the islanding detection technique to be operational with loads having $1 \leq Q_f \leq 2.5$ at resonant frequency [25]. Fig. 12 shows the general effect of changing the Q_f on the output waveform of an island with zero mismatch and with both the Mean 3 and RMS fundamental frequencies set to 12 Hz. As depicted, a higher
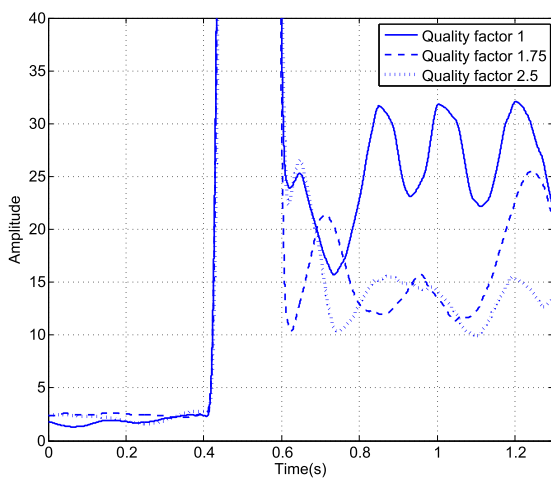

FIGURE 12. Effect of changing Q_f on islanding detection waveform.

quality factor reduces the margin between the islanding and non-islanding levels. This is because a higher Q_f means there is an increased reactance in the load which would decrease

the amount of frequency oscillations in voltage and current waveforms after islanding. A similar effect is observed in the output waveform for all other islanding scenarios. Therefore, the threshold was set based on the worst Q_f case of 2.5.

After thorough experimentation with islanding and non-islanding events using fundamental frequencies ranging from 6 Hz to 30 Hz with Q_f set to 2.5, the fundamental frequency of 12 Hz for both the Mean and RMS blocks was selected as an optimal value. The optimum threshold and time delay at this frequency were 4.5 V/s and 0.3s, respectively.

V. RESULTS AND DISCUSSION

A large number of possible islanding and non-islanding events were investigated to verify the performance of the proposed detection technique. Table 2 lists all the different types of simulated events and the number of cases simulated for each event. The results are summarized as follows.

TABLE 2. Simulated Islanding and non-islanding scenarios.

Event	Parameter	# of Events
Islanding Events		
Real Power Mismatch	-50% to +50%	29
Reactive Power Mismatch	-4% to +4%	8
Non-Islanding Events		
Three-Phase Faults	1-75Ω Fault Resistance	25
Line-to-Line Faults	1-75Ω Fault Resistance	25
Single-Phase Faults	1-75Ω Fault Resistance	25
Load Switching (260 V)	10-100 kVA	10
Load Switching (25 kV)	1-30 MVA	10
Capacitor Switching (260 V)	3-30 kVAR	10
Capacitor Switching (25 kV)	300-3000 kVAR	10
Loss of Parallel Feeder	100-2000 MVA_{sc}	20
Motor Starting	100-300 kVA	20

A. RESULTS OF ISLANDING EVENTS

Fig. 13(a) and 13(b) show the islanding detection output waveform and the islanding trigger signal, respectively, for an island with zero power mismatch. Before
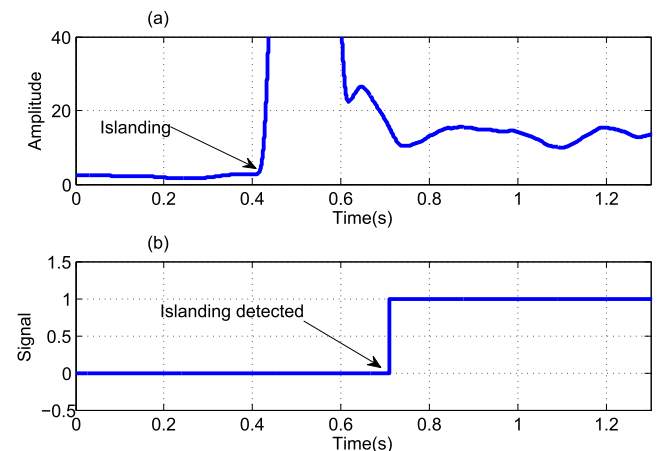

FIGURE 13. Zero mismatch scenario. (a) Islanding detection waveform. (b) Islanding trigger signal.

islanding, the waveform stayed well below the predefined threshold. However, after islanding, the waveform

consistently was above the threshold and islanding was detected within 0.3s.

Both positive and negative real power mismatch scenarios were simulated for $Q_f = 2.5$ with 1% increments from 1% to 10% followed by 10% increments from 20% to 50%. Positive real power mismatch indicates that the generator supplies more power than what the load consumes while negative real power mismatch indicates that the load requires more power than what the generator is able to supply. The percentage is with respect to the load nominal real power. Fig. 14 shows the detection waveform and the islanding trigger signal for ±10% and ±20% real power mismatches. P_L represents
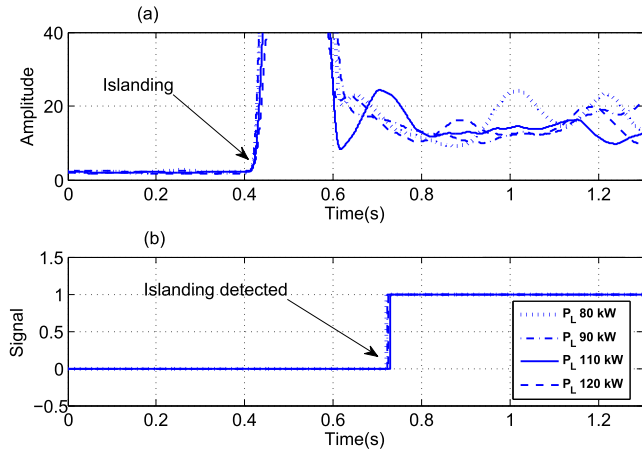

FIGURE 14. Real power mismatch scenarios. (a) Islanding detection waveform. (b) Islanding trigger signal.

the real power consumed by the load. As shown, the detection waveforms did not go below the predefined threshold after islanding and this resulted in accurate detection every time islanding occurred.

Reactive mismatch scenarios between ±4% were simulated with $Q_f = 2.5$. In these scenarios, positive reactive mismatch indicates that the load inductive power requirement is greater than its capacitive requirement while negative reactive mismatch means the opposite. Fig. 15 shows the detection waveform and the islanding trigger signal for ±1% and ±4% reactive power mismatches (ΔQ_L), the detection waveforms remained well above the threshold, resulting in an accurate detection of islanding. It is also observed that the minimum level of the islanding detection waveform is higher for increased levels of reactive mismatch. As a result, simulations of higher levels of reactive mismatch were not presented.

B. RESULTS OF NON-ISLANDING EVENTS

The various possible non-islanding events that can falsely trigger islanding detection are short-circuit faults, loss of a parallel feeder (LOPF), load switching, capacitor switching, non-linear loads, and starting of large motors. Each of these non-islanding scenarios have been simulated to verify the accuracy of the proposed technique.
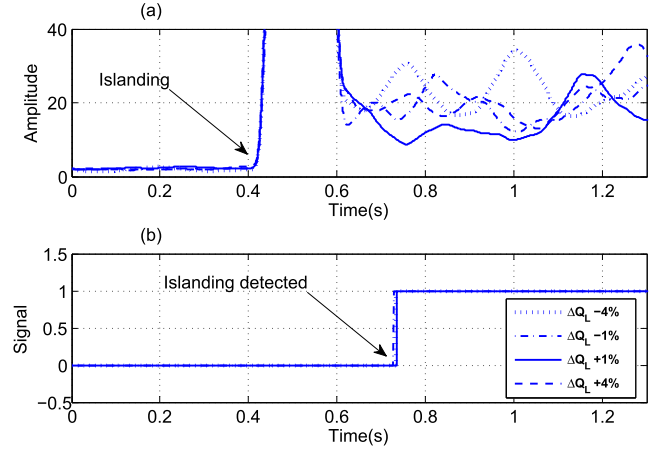

FIGURE 15. Reactive power mismatch scenarios. (a) Islanding detection waveform. (b) Islanding trigger signal.

Figs. 16 and 17 show the detection waveforms for several simulated non-islanding events such as short-circuit faults, LOPF, load switching, and capacitor switching. The fault
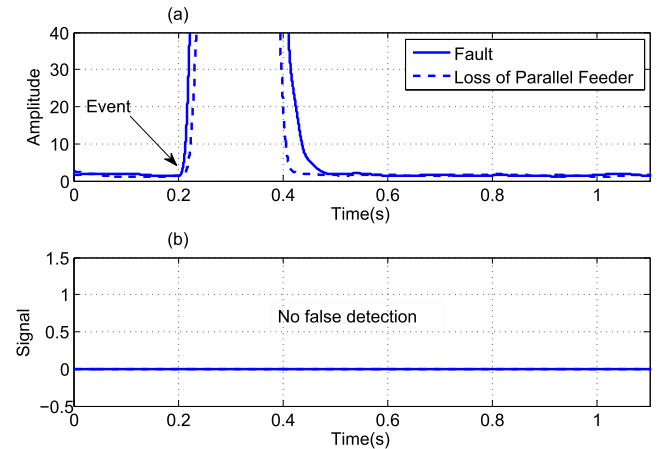

FIGURE 16. Fault and loss of parallel feeder scenarios. (a) Islanding detection waveform. (b) Islanding trigger signal.

scenarios were simulated by initializing a short-circuit fault on a parallel feeder. The circuit breaker on the parallel feeder tripped within 0.02s, thereby clearing the fault. The type of short-circuit faults simulated were 3-phase faults, line-to-line faults and single-line to ground faults. For each case, the total fault resistance was varied from 1Ω to 75Ω, with 3Ω increments. For LOPF scenarios, the utility supply was represented by two parallel feeders of equal short-circuit strength. The total short-circuit MVA of the feeders was varied from 100 MVA_{sc} to 2000 MVA_{sc} with 100 MVA_{sc} increments. Fig. 16 illustrates the islanding detection waveforms and the islanding trigger signals for a 3-phase fault and a LOPF scenario. The fault scenario represents a 1Ω 3-phase fault occurring at 0.2s, while the LOPF scenario represents a weak grid of 100 MVA_{sc} consisting of two parallel feeders of 50 MVA_{sc} each. At 0.2s, one of the feeders is disconnected to simulate LOPF. In both cases, the settling time for the
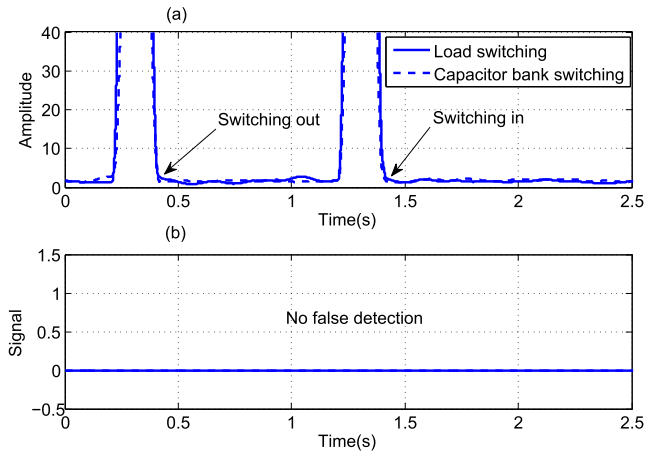
FIGURE 17. **Load and capacitor bank switching scenarios. (a) Islanding detection waveform. (b) Islanding trigger signal.**

detection waveform was lower than the predefined detection delay and therefore no false detection was triggered.

The load switching scenarios involved in/out switching on both the 260 V and 25 kV sides. On the 260 V side, the load kVA was varied between 10-100 kVA with 10 kVA increments while on the 25 kV side, the load kVA was varied between 1-30 MVA with 3 MVA increments. In/out switching of a capacitor bank was also investigated. In these experiments, the load was replaced by a capacitor bank. On the 260 V side, the capacitor bank rating was varied between 3-30 kVAR, with 3 kVAR increments while on the 25 kV side, the capacitor bank rating was varied between 300-3000 kVAR with 300 kVAR increments. Fig. 17 illustrates the islanding detection waveforms and the islanding trigger signals for load and capacitor bank switching scenarios. The load switching scenario represents in/out switching of a 30 MVA load on the 25 kV side. The capacitor bank switching scenario represents the in/out switching of a 3000 kVAR capacitor bank on the 25 kV side. False islanding detection did not occur for any of these events because the detection waveforms settled down to normal levels before the detection delay expired.

Table 3 summarizes the efficacy of the proposed islanding detection technique for islanding and non-islanding events.

TABLE 3. **Efficacy of proposed islanding detection method (threshold: 4.5 V/s, delay: 300 ms).**

Islanding Events	
Type of Islanding	**Minimum $O_{islanding}$ after Islanding**
Real Power Mismatch (-50% to $+50\%$)	$7\ V/s$
Reactive Power Mismatch (-4% to 4%)	$9\ V/s$
Non-Islanding Events	
Type of Non-Islanding	**Maximum Delay** (ms)
Faults	261.4
Capacitor Switching	207.5
Load Switching	203.7
Loss of Parallel Feeder	199.5

C. SPECIAL NON-ISLANDING EVENT: MOTOR STARTING

Starting a large motor can cause voltage fluctuations in the system which may falsely trigger islanding detection. Therefore, the effect of motor starting was also investigated. The motor loading was varied and the effect on the detection waveform was observed. Fig. 18 illustrates the PCC RMS voltage and the islanding detection waveforms for a 223 kVA (300 HP) induction motor. As shown, the variation in the
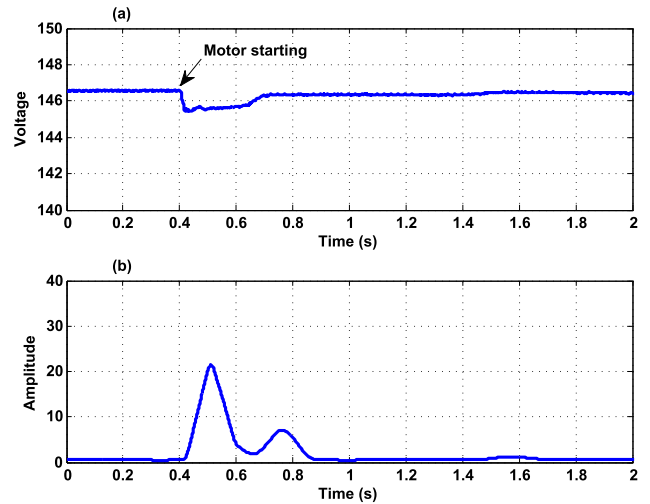

FIGURE 18. **Effect of 100 kVA motor starting on (a) RMS voltage waveform at PCC and (b) islanding detection waveform.**

PCC RMS voltage waveform is due to the high starting currents drawn by the motor. This causes two subsequent peaks in the detection waveform as illustrated in Fig. 18(b). As the motor power requirement increases, the time needed for the peaks to settle will also increase. As a result, the technique will trigger false islanding for motors larger than 245 kVA (328 HP) with a settling time exceeding 0.3s. If the delay is extended beyond 0.3s, the technique will also apply for higher motor ratings. However, motors with ratings above 300 HP are rarely used, so the delay threshold was not increased in order to maintain fast islanding detection.

D. EFFECT OF POWER SYSTEM PARAMETERS

Several additional experiments were conducted to investigate the effect of the power system topology and its parameters on the robustness of the proposed technique as discussed next.

1) EFFECT OF THE PRESENCE OF NON-LINEAR LOAD

Nowadays, consumers use many electronic devices such as computers, printers, and fax machines. These devices require DC power and thus have built-in rectifiers to convert the AC power to DC [32]. Rectifiers are considered non-linear loads because the current they draw is not linear. The presence of non-linear loads have been known to cause problems especially for passive techniques [13]. The increased presence of non-linear loads generates harmonics which can lead to false detection of islanding in the grid-connected mode. Thus, the impact of non-linear load on this technique was

investigated. A 2 kW DG system was modeled, which represents a typical rooftop PV system. In this simulation, the non-linear load was represented by a 3-phase rectifier. The load power consumption was varied by changing its resistance. Table 4 shows the DG power (P_{DG}), linear load power (P_{LL}), non-linear load power (P_{NL}), and the maximum value of the islanding detection waveform in grid-connected mode (d_{max}).

TABLE 4. Effect of presence of non-linear load.

P_{DG} (kW)	P_{LL} (kW)	P_{NL} (kW)	d_{max} (V/s)
2	2	0	2.58
2	1.8	0.2	2.72
2	0.2	1.8	2.74

As shown, the presence of non-linear load has no significant effect on the grid-connected levels of the detection waveform. Thus, it was verified that the technique does not trigger false islanding detection due to the presence of a non-linear load.

2) EFFECT OF TRANSFORMER NOMINAL POWER

The nominal power of the distribution transformer was varied to observe its effect on the average detection waveform levels for the grid-connected and islanded scenarios. An islanded scenario of zero real power mismatch with a load $Q_f = 2.5$ was simulated. Fig. 19 illustrates the effect of varying the transformer nominal kVA compared to the rated load. As observed, increasing the ratio between the transformer nominal kVA and the rated load has the effect of widening the gap between the grid-connected and islanded detection waveform levels. When the nominal power of the trans-
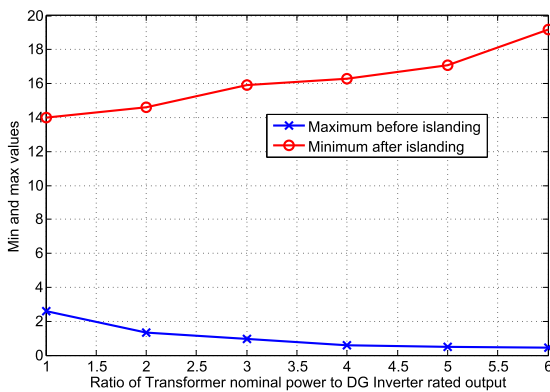

FIGURE 19. Effect of changing the distribution transformer kVA.

former increases, the grid-connected detection waveform level decreases due to the stabilization effect of the grid. In islanded mode, the impedance of the transformer is added to the islanded load [25]. The change in the transformer's impedance causes variation in the islanded voltage signal which increases the level of the detection waveform. Similar effect is observed for all other islanded scenarios. Varying the transformer kVA does not have any effect on the settling

time delay for non-islanding events. Distribution transformers always have higher nominal power than their maximum load, i.e., the ratio between the transformer nominal kVA and the rated islanded load is always greater than 1. So, it is verified that changing the nominal power of the transformer has no detrimental effect on the performance of the proposed technique.

3) EFFECT OF CHANGING THE DG NOMINAL POWER

The rated output of the DG inverter and the peak power of the PV array were varied between 25 to 200 kW with 25 kW increments. Table 5 shows the average values of the detection waveform (d_{avg}) during grid-connected and islanded scenarios for the different levels of DG nominal power. An island

TABLE 5. Effect of changing the DG nominal power.

DG nominal power (kW)	d_{avg} before islanding (V/s)	d_{avg} after islanding (V/s)
25	3.995	24.702
50	2.344	17.163
75	2.506	14.407
100	1.95	15.67
125	1.778	13.782
150	1.826	18.961
175	2.738	15.145
200	3.834	42.560

scenario of zero real power mismatch with a load $Q_f = 2.5$ was simulated. The grid-connected detection waveform levels were found to be consistently below the threshold and the islanded detection waveform levels were always above it. This verifies that the performance of the technique is not limited to any nominal power range of DG systems.

4) EFFECT OF MULTIPLE DGs

The effect of the presence of multiple DG sources on the detection of islanding was investigated. To test this scenario, two PV inverter-based DGs with power rating of 100 kW were connected to the grid. Each DG has its electronic devices for operation and control as illustrated in Fig. 20.

Three different islanding scenarios, including the worst case scenario, were simulated with load at $Q_f = 2.5$. Table 6

TABLE 6. Comparison of the proposed detection performance in the presence of a single and multiple DG systems.

Event	One DG		Two DGs	
	d_{min} (V/s)	d_{max} (V/s)	d_{min} (V/s)	d_{max} (V/s)
Zero mismatch	1.94	11.50	1.90	11.22
Real power deficit of 10%	1.76	13.21	2.51	10.13
Real power excess of 10%	2.20	9.92	1.92	9.94

TABLE 7. Comparison between the proposed and classical islanding detection techniques.

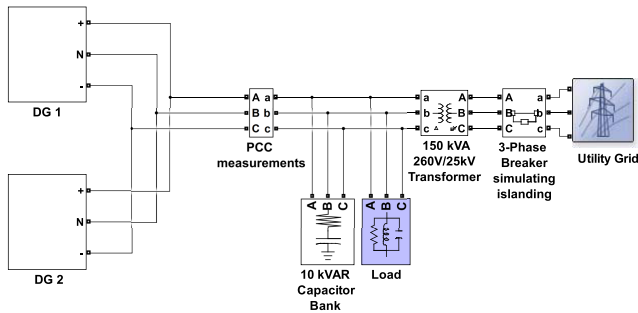| Technique	Categories				
	Non-detection Zone	Detection Time	Power Quality	Reliability	Multiple DGs Effect
Passive (OVP/UVP, ROCOF, PJD)	Large NDZ	Short	No Effect	Low	No Effect
Active (IM, AFD, SVS, SFS)	Small NDZ	Long	High Degradation	High	Synchronization Issues
Proposed Passive Approach	No NDZ	Medium	No Effect	High	No Effect

FIGURE 20. Grid-connected model containing two DGs in parallel.

lists the minimum (d_{min}) and maximum (d_{max}) levels of the detection waveform for single and multiple DG events. It was observed that the minimum and maximum values for all cases were relatively close to each other. This indicates that the performance of the proposed technique is not affected by the presence of another DG source within the island zone.

E. COMPARISON WITH PREVALENT ISLANDING DETECTION TECHNIQUES

A wide variety of islanding techniques have been designed and implemented in real application. Some of the most commonly implemented passive techniques are over/under voltage protection (OVP/UVP) and over/under frequency protection (OFP/UFP), phase jump detection, and rate of change of frequency. These techniques have the advantage of simple operation and relatively easy implementation. However, they suffer from performance issues such as non-detection when the load mismatch is relatively small and false detection due to non-islanding events [33]–[35].

Active techniques such as Impedance Measurement (IM), Active Frequency Drift (AFD), Sandia Frequency Shift (SFS), Sandia Voltage Shift (SVS), have smaller NDZ than the passive techniques and do not suffer from false detection issues. However, they constantly inject harmonics into the system, thereby reducing power quality. Furthermore, active techniques are generally implemented in the DG inverter. If there are multiple DG sources in the

islands, the disturbance injection needs to be synchronized, otherwise the resultant effect gets diluted. Such synchronization becomes complicated for multiple DG systems [13], [36], [37].

The proposed passive technique has the advantage of not having any NDZ and also not suffering from any false detection as demonstrated in all tested scenarios. Therefore, using this technique eliminates the drawbacks of the contemporary passive techniques while retaining operational simplicity. In addition, it does not affect the power quality of the system, and doesn't have to be synchronized for multiple DG sources. Table 7 provides a brief performance comparison between the proposed and several other islanding detection techniques.

VI. CONCLUSION

A novel passive islanding detection technique for grid-connected PV inverters was presented in this paper. The proposed technique monitors, in time domain, the ripple content of the RMS value of the PCC voltage and detects islanding when the ripple content is higher than a predefined threshold for a certain period of time. The proposed technique was thoroughly tested under a variety of possible islanding scenarios, including active and reactive power mismatches over a wide range of RLC loads of varying Q_f. The tested non-islanding scenarios included faults, loss of parallel feeder, load switching, capacitor bank switching and motor starting. The proposed technique successfully detected islanding for all cases including the worst case scenario of zero percent power mismatch. Furthermore, it was able to accurately distinguish islanding from the tested non-islanding events. The presence of dynamic and non-linear loads such as rectifiers had no impact on the performance. However, the technique did exhibit false islanding detection during the starting of induction motors rated above 300 HP. The technique is independent of the nominal settings of the DG and is not affected by the presence of multiple DGs in the system. The technique was able to detect islanding within 300ms, which is well below the 2s imposed by the IEEE 1547 standards. Moreover, the technique is computationally inexpensive and can be easily implemented into a PV inverter.

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