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A 15 kW Wide-Input Reconfigurable Three-Level DAB Converter for On-Board Charging of 1.25 kV Electric Vehicle Powertrains

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***Abstract*—The demand to reduce charging times and run-time losses in electric vehicles has created a push to increase battery pack's voltage level. 800 V class vehicles in production are approaching the 1 kV voltage limit of the Combined Charging System (CCS) connector. New fast charging standards such as ChaoJi (CHAdeMO 3.0) and Megawatt Charging System (MCS) have voltages defined up to 1.5 kV and 1.25 kV, respectively. The SAE J3068 standard, focused on 3-Φ AC charging, recommends compatibility from 208/120Y to 600/347Y, resulting in a wide voltage variation of the power factor correction (PFC) stage's DC link. This paper proposes a reconfiguration method of a neutral-point clamped (NPC) converter in a three-level dual active bridge (DAB) converter to accommodate the wide voltage swing. The reconfigurable three-level DAB converter (R3L-DAB) topology is introduced, and its modes of operation are presented. The steady-state analysis and its soft-switching criterion are discussed. A power loss model and design methodology are established to choose the switching frequency (f_{sw}), turns ratio (n), and leakage inductance (L_k). Finally, the experimental results of a 15 kW R3L-DAB converter, with a power density of 3.25 kW/L and peak efficiency of 97.32% are presented.**

***Index Terms*—Dual active bridge, electric vehicle (EV) charging, megawatt charging system (MCS), medium- and heavy-duty vehicle (MHDV), on-board charger (OBC), multilevel dc/dc converter, neutral-point clamped converter, silicon carbide (SiC).**

Nomenclature

A_c	Transformer core cross section area.
d	dc/dc converter conversion ratio.
D_1	Zero-level duration on the 5-level bridge.
D_2	Half-level duration on the 5-level bridge.
f_{sw}	dc/dc converter switching frequency.
i_p	Transformer primary current.
i_b	Transformer secondary current.
k_{cfg}	Configuration factor of the RNPC.
k_{fe}, α, β	Transformer core Steinmetz coefficients.
L_k	Total system leakage inductance.
n	Secondary to primary transformer turns ratio.
n_l	Number of layers per winding.
N_p	Number of primary turns.
$P_{hb(NPC)}$	NPC reconfiguration power loss.
$P_{hb(ANPC)}$	ANPC reconfiguration power loss.
$P_{hb(RNPC)}$	RNPC reconfiguration power loss.
P_{out}	R3L-DAB converter output power.
$R_{ds(on)}$	MOSFET on-state resistance.
t_{cu}	Transformer winding copper thickness.
T_s	Switching period.
T_{hs}	Half-cycle switching period.
V_{LL}	Line to line voltage.
V_{ph}	Phase voltage.
V_{PFC}	Power factor correction stage DC link voltage.
V_{batt}	Battery pack voltage.
V_P	Input DC link voltage.
V_B	Output DC link voltage.
w_{pri}	Transformer primary winding trace width.
w_{sec}	Transformer secondary winding trace width.
Z_{norm}	Normalized high-frequency link impedance.
η	dc/dc converter efficiency.
φ	Primary to secondary phase shift.
ρ	Resistivity of copper.
ρ_V	Volumetric power density of the dc/dc stage.
OBC	On-board charger.
MCS	Megawatt charging system.
MHDV	Medium- and heavy-duty vehicle.
MLT	Mean length per turn.
NPC	Neutral-point clamped.
RNPC	Reconfigurable neutral-point clamped.
R3L-DAB	Reconfigurable three-level dual active bridge.

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I. Introduction

WITH the exception of neighboring islands, North America has a land-connected region of 21.792 million km^2 covering Mexico, United States of America (U.S.), and Canada. As of 2022, transborder truck freight between the U.S., Canada, and Mexico accounted for \$ 827.8 billion worth of economic activity [1]. A U.S. Environmental Protection Agency (EPA) study shows that medium- and heavy-duty vehicles (MHDV) contributed to 26% of the total greenhouse gas (GHG) emissions from transportation in 2020 [2]. Depending on the adoption rate of battery electric vehicles (BEVs), the projected greenhouse gas (GHG) emissions from MHDVs are expected to decrease to as low as 80 Megatonnes of carbon dioxide equivalent (CO2e) by 2050, compared to the current emissions of 625 Megatonnes (CO_2e) [3]. DC fast charging of MHDVs will draw megawatt scale charging power to replenish the battery in a short time, causing a violation of the grid's fluctuation limits without proper coordination of requested power levels [4]. As of 2023, BEV charging in

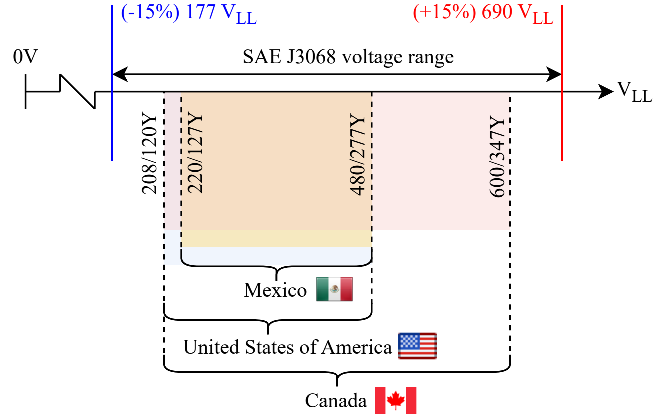


Fig. 1. Three-phase (3-Φ) grid voltage range in North America.

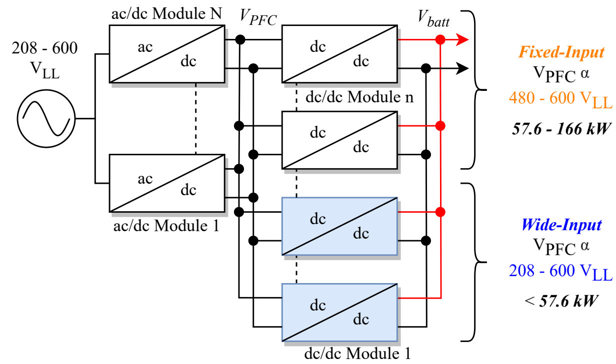


Fig. 2. Multi-module IPOP two-stage on-board charger structure.

North America is governed by SAE J1772 with the potential for moving completely to NACS (North American Charging Standard), which are both single-phase (1-Φ) charging compatible. For Level 3 AC charging ($>$ 43 kW), the SAE J3068 standard has been recommended for adoption and is three-phase (3-Φ) charging compatible [5]. As shown in Fig. 1, the 3-Φ voltage varies from 208-600 V_{LL} (line-line) across Canada, Mexico, and the U.S. With the introduction of DC fast charging standards such as Megawatt Charging System (MCS) and ChaoJi/CHAdeMO 3.0, the powertrain voltages of MHDVs are anticipated to be raised as high as 1.25 kV to 1.5 kV [6]. Fig. 2 shows the structure of a multi-module, input parallel output parallel (IPOP) two-stage on-board charger, where the ac/dc power factor correction stage generates a DC link, and a dc/dc converter interfaces the generated DC link with the traction battery. The control loop for output voltage or current regulation can incorporate variation either on the ac/dc or dc/dc stage, or both, depending upon the region of operation. An approach for current-fed PFC rectifiers is to buck/boost the PFC DC link voltage while maintaining a unity conversion ratio of the dc/dc stage to maintain high-efficiency operation [7]. In the case of conventional PFC rectifiers, their efficiency reduces as the voltage gain increases due to elevated hard-switching losses [8]. Thus, lowering the gain of a conventional PFC rectifier enables operation in its high-efficiency region. To manage a large voltage swing as a result of a grid voltage variation from 208-600 V_{LL} across North America, the dc/dc converter in an SAE J3068 compliant on-board charger using a conventional PFC rectifier must support a wide-input and wide-output voltage operation. In the context of electric vehicle charging, multiple topologies have been reported for the support for 400 V and 800 V DC fast charging [9]–[12], however the input voltage variation is not a challenge in this application due to a fixed DC link of the PFC stage. The authors in [13] report the use of a semi-DAB in a battery energy storage system (BESS) supported DC fast charger; however, this has been applied to 400 V traction battery systems. Recent work in dc/dc converters for on-board chargers has reported peak efficiencies from 96 - 98.8% and power densities up to 8.66 kW/L for the dc/dc conversion stage [14]–[17]; the effect of variation in the PFC DC link voltage is not examined due to standardization of 1-Φ charging in light-duty electric vehicles. With electric vehicle powertrain voltages increasing beyond the 1 kV limit from the Combined Charging System (CCS) connector and the introduction of new DC fast charging standards like MCS and ChaoJi/CHAdeMO 3.0, it is important to address on-board charging requirements of future electric vehicles with high-voltage ($>$ 1 kV) powertrains. The key contributions of this paper are as follows:

1) A novel reconfiguration method is proposed for the neutral-point clamped converter to switch between half- and full-bridge modes, which aids in the reduction of the conversion effort on the converter. This method eliminates the need for additional relays or contactors, which are limited by a fatigue life and consume a higher volume compared to solid-state devices.
2) The steady-state analysis to derive the instantaneous and RMS currents, voltages, and zero voltage switching (ZVS) conditions under the defined modulation scheme is verified.
3) The power loss model utilizing the steady-state analytical equations is proposed, to estimate the efficiency of the R3L-DAB converter under varying operating conditions, and a design optimization procedure to select the turns ratio (n), leakage inductance (L_k), and switching frequency (f_{sw}) has been proposed. The achieved power density is 3.25 kW/L.
4) The experimental verification of a 15 kW R3L-DAB converter in the half- and full-bridge modes under varying input voltage, output voltage, and power levels has been performed.

This paper is arranged as follows: Section II discusses the projections of 3-Φ on-board charging in North America, and it is contextualized for medium- and heavy-duty vehicles with $>$ 1 kV powertrains. Section III discusses the novel reconfigurable three-level dual active bridge converter, its operating principle, steady-state analysis, and its soft-switching criterion. Section IV discusses the application of the analytical solutions to the power loss model, and the design optimization procedure followed for the selection of key converter parameters. The construction of the R3L-DAB converter and its experimental

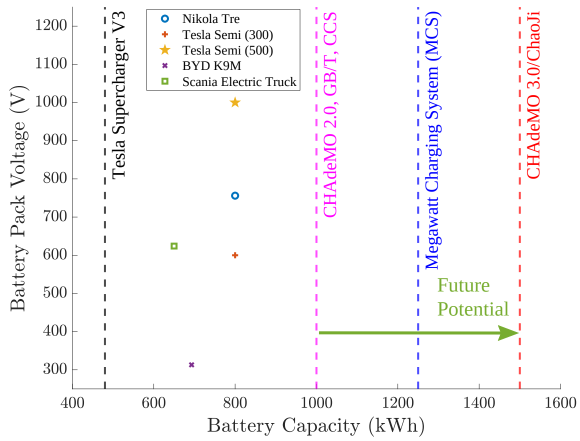


Fig. 3. Current status of electrified medium- and heavy-duty vehicles.

verification is presented in Section V.

II. On-Board Charging of Medium- & Heavy-Duty Vehicles (MHDV) in North America

A. Wide Three-Phase (3-Φ) AC Voltage Range

Battery electric vehicles in North America are equipped with on-board chargers compliant with the SAE J1772 or the NACS connector, which only support 1-Φ charging with power levels up to 22 kW. The 3-Φ compatible SAE J3068 charging standard has been recommended for AC Level 3 charging of medium- and heavy-duty vehicles for power levels up to 166 kW. In North America, Mexico, the U.S., and Canada differently handle the transmission and distribution of 3-Φ power. As shown in Fig. 1, 220/127Y and 480/277Y are common in Mexico, 208/120Y and 480/277Y are common in the U.S., while 208/120Y, 480/277Y and 600/347Y are common in Canada. The voltage ranges of Mexico and the U.S. are inter-compatible. However, Canada is an exception due to a higher voltage limit of 600/347Y. To support the on-board charging feature across North America, a vehicle manufacturer must cater to the voltage level from 208/120Y to 600/347Y to remain competitive in the market. Beyond this, the SAE J3068 standard requires a charger to adhere to a ±15% margin on the communicated voltage range to the electric vehicle supply equipment (EVSE) to account for any voltage sag or swell on the 3-Φ AC inlet [18]. This requires a further extension to the input voltage, ranging from 177 - 690 V_{LL}, while accounting for fluctuations.

B. On-Board Charging of Medium- and Heavy-Duty Vehicles

Increasing the powertrain voltage provides benefits such as reduced conduction losses in the powertrain cabling, lower consumption of copper in the vehicle and traction motors, and lower DC fast charging time due to higher DC fast charging power without increasing the cable dimension [19]. DC fast charging standards such as Megawatt Charging System (MCS) and ChaoJi/CHAdeMO 3.0 can support battery voltages up to 1.25 kV and 1.5 kV and have been targeted for adoption in medium- and heavy-duty vehicles [6]. Fig. 3 shows the current status of electrified MHDVs against the voltage limits of the DC fast charging standards. It can be noted that the battery voltages of existing electrified MHDVs are below the connector voltage of 1 kV, limited by the Combined Charging System connector. To support megawatt scale charging of MHDVs, the authors in [4, 20] have proposed methods to interact with the grid and dynamically modify the charging power level based on the grid loading scenario since the demand of megawatt-scale charging power can risk instability of the grid. Additionally, supporting the battery charging of MHDVs exclusively via DC fast charging requires significant capital expenditure in charging infrastructure to reduce the consumer's range anxiety. Having a secondary source of charging the MHDV until DC fast charging infrastructure is established can be addressed by housing an on-board charger (OBC) in the vehicle.

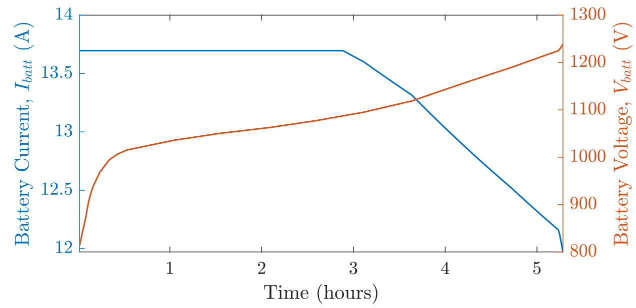


Fig. 4. Charging profile of a 1.25 kV, 500 Ah Li-ion battery.

TABLE I
Charging Power (kW) as a function of varying AC input voltage and SAE J3068 contacts

Contact Current			63 A	100 A	120 A	160 A
V_{ph} (V)	V_{LL} (V)	$V_{PFC(min)}$ (V)	Power (kW)			
120	208	294	22.7	36	43.2	57.6
127	220	311	24	38.1	45.7	61
277	480	679	52.4	83.1	99.7	133
347	602	851	65.6	104.1	124.9	166.6

C. On-Board Charger DC/DC Converter Requirements

As established in Section II-A, the 3-Φ voltages in North America are 208/120Y, 220/127Y, 480/277Y, and 600/347Y. The SAE J3068 standard has variation in the amperage of the current carrying contacts, which determines the power delivery limit of a charging connector. The standard contacts are rated at 63 A, while advanced contacts (AC_6) are rated at 100 A, 120 A, 160 A [18]. Table I shows the values of the charging power P_{charge} for varying values of grid phase voltage V_{ph}, charging contact current I_{ph}, and displacement power factor $\cos\phi$, as seen in (1).

$$P_{charge}(\text{kW}) = \eta 3 V_{ph} I_{ph} \cos\phi \tag{1}$$

A conventional PFC converter stage can be classified as buck, boost, or buck-boost types. Since the battery voltage is higher than the AC input voltage, an example of a boost PFC converter, such as the six-switch PFC rectifier or the Vienna rectifier is assumed. The minimum DC link voltage of the PFC $V_{PFC(min)}$ below which regulation is not possible is given by (2).

$$V_{PFC(min)} = \sqrt{6} V_{ph} \tag{2}$$

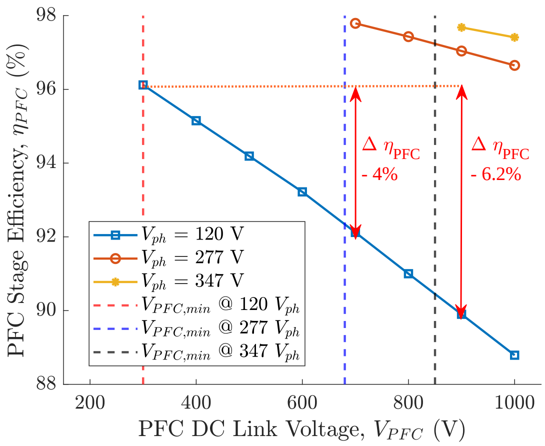


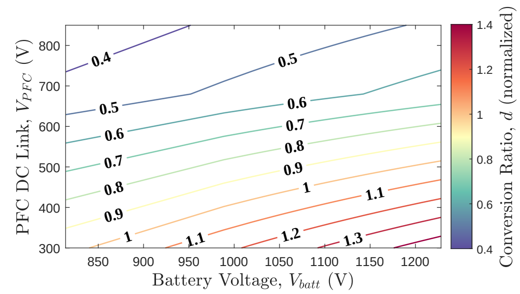
Fig. 5. Simulated efficiency of a 3-Φ boost PFC converter operating at 15 kW, with varying V_{PFC} and V_{ph}.

TABLE II
DESIGN TARGETS OF THE R3L-DUAL ACTIVE BRIDGE CONVERTER

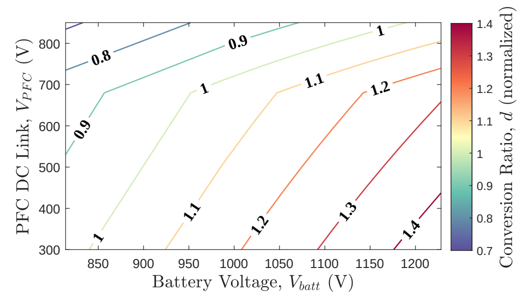
Design Variable	**Description**	**Specification**
V_{PFC}	PFC DC link range	300 - 850 V
V_{batt}	Battery voltage range	890 - 1250 V
P_{out}	Power rating	15 kW

A 3-Φ PFC converter is preferred to be operated in the continuous conduction mode (CCM) due to high power-handling requirements [8]. This causes hard-switching in the PFC converter, resulting in higher switching losses and, thus, a lower efficiency [21]. In a conventional two-level boost PFC converter, the switch's voltage stress is the DC link voltage, while the current stress is a sinusoidal input current. As the PFC's DC link voltage is raised beyond $V_{PFC(min)}$, the converter's efficiency diminishes based on the trajectory of rise in switching energy. That being said, the lowest losses will be experienced on the PFC converter when V_{PFC} = $V_{PFC(min)}$. As explained in Section II-A, the on-board charger must operate from 208/120Y to 600/347Y to fully cater across North America's varying grid voltage, referring to a voltage swing between $300 < V_{PFC} < 850$ V, to enable a minimal reduction in the efficiency of the PFC converter. Fig. 5 shows the simulated efficiency map of a 3-Φ boost PFC converter in the PLECS environment, operating at a load of 15 kW, f_{sw} = 100 kHz, and utilizing Wolfspeed's C3M0016120D (1.2 kV/ 16 mΩ) SiC MOSFETs. The simulation confirms that the efficiency drop is detrimental as the DC link voltage of the PFC stage increases, especially at lower input phase voltages.

A Li-ion NMC cell varies from 3 - 4.2 V, representing 0 - 100% state of charge. A 1.25 kV battery pack would require serialization of 296 cells, resulting in a total battery voltage swing from 890 - 1250 V. The maximum power defined in SAE J3068 is 166 kW, and the R3L-DAB converter is expected to operate in a multi-module IPOP architecture, as shown in Fig. 2. The power level of the R3L-DAB is approximately 1/10$^{\text{th}}$ of the maximum power, and is set to 15 kW. The design requirements are summarized in Table II.



(a)



(b)

Fig. 6. (a) Conversion gain without topology morphing control; (b) Conversion gain with topology morphing control.

III. PROPOSED RECONFIGURABLE THREE-LEVEL DUAL-ACTIVE BRIDGE CONVERTER (R3L-DAB)

A. Reconfigurable Neutral-Point Clamped Converter

As the conversion ratio of a dual active bridge converter deviates from unity, the circulating current in the converter increases, resulting in an increase in transformer and switch RMS and peak current, increased conversion effort (bucking or boosting operation), and a detrimental impact on efficiency [22]. Various modulation techniques have been proposed in the literature to improve the ZVS range and peak current stress of the dual active bridge converter, resulting in improved efficiency [23]. Topology morphing control (TMC) is a method where the bridge of a dc/dc converter is switched between half- or full-bridge mode, depending upon the DC link voltage, in order to reduce the extent of the voltage swing observed by the high-frequency link [24]. At lower DC link voltages, the bridge is configured in the full-bridge mode, while at higher DC link voltages, it is configured in the half-bridge mode, thus ensuring reduced voltage swing across the bridge output.

$$d = \frac{V_B}{nV_P k_{\text{cfg}}} \tag{3}$$

The conversion ratio d is defined by (3), and is a function of the output voltage V_B, input voltage V_P, secondary to primary turns ratio n, and the configuration factor k_{cfg}, which is set to 1 while operating in full-bridge mode and is set to 0.5 while operating in half-bridge mode. Fig. 6(a) shows the contour map of d, when the converter's primary is operated in full-bridge mode, without any topology morphing control, and the range of d is 0.34 - 1.46. Fig. 6(b) shows the contour map of d, when the converter's primary is operated in full-bridge

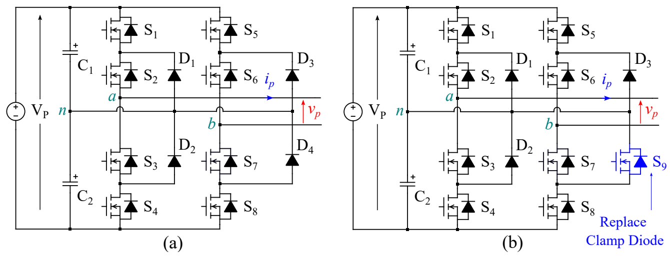


Fig. 7. (a) Conventional neutral-point clamped converter; (b) Reconfigurable neutral-point clamped (RNPC) converter.

TABLE III
VECTOR MATRIX OF THE NPC AND RNPC CONVERTERS

S_5	S_6	S_7	S_8	S_9	**Vector**	**Output referred to 'n'**	**Converter**
1	1	0	0	X	P	$+V_P/2$	NPC/ RNPC
0	1	1	0	X	O	0	NPC/ RNPC
0	0	1	1	X	N	$-V_P/2$	NPC/ RNPC
0	0	1	0	1	R	0	RNPC only

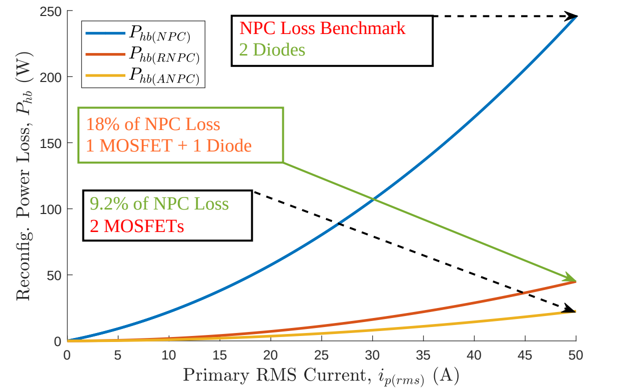
mode when V_{PFC} = 300 V, and in half-bridge mode when V_{PFC} = 680/850 V, and the range of d reduces to 0.68 - 1.46.

Fig. 7(a) shows a conventional three-level neutral point clamped (NPC) converter. C_1 and C_2 are the DC link capacitors, S_1-S_8 are the MOSFETs, and D_1-D_4 are the clamped diodes. Considering leg b of the converter, $S_5 = \overline{S_7}$ and $S_6 = \overline{S_8}$, and are modulated with separation of dead-time. Fig. 7(b) shows the proposed three-level reconfigurable neutral-pointed clamped (RNPC) converter which is created when D_4 in a conventional NPC converter is replaced with a MOSFET S_9. Table III shows the vector table of the conventional NPC converter and RNPC converter. It can be seen that the 'O' and 'R' vectors develop 0 V referenced to the 'n' potential. However, the 'R' vector can only be developed in the RNPC converter, and their differences are highlighted further.

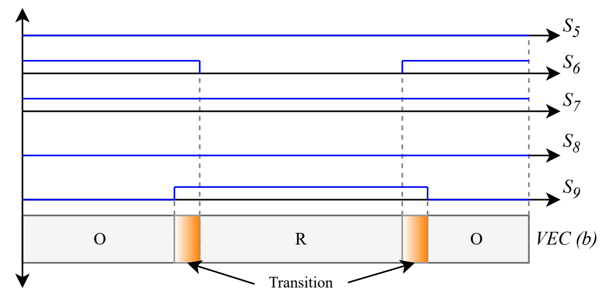
To operate either of the converters in the full-bridge mode, the modulation scheme representing the P/O/N vectors can be individually applied to either of the legs, and the output voltage swing $v(t) = \pm V_P$. To operate a NPC converter in the half-bridge mode, S_6 and S_7 are turned on, resulting in a 'O' vector on leg b and limiting the output voltage swing $v_p(t) = \pm V_P/2$. The reconfiguration power loss is defined as the additional conduction loss experienced in the dc/dc converter stage when switched to the half-bridge mode. This is achieved by permanently routing the AC node's potential of one half-bridge to neutral. The reconfiguration power loss in a NPC, $P_{hb(NPC)}$ is given by (4), where $i_{p(rms)}$ is the RMS current handled by the bridge, $R_{ds(on)}$ and R_d are the on-state resistances of the MOSFETs and clamp diodes, V_{T0} is the clamp diode threshold voltage.

$$P_{hb(NPC)} = i_{p(rms)}^2 \left(R_{ds(on)} + R_d + \frac{\sqrt{2}V_{T0}}{i_{p(rms)}} \right) \tag{4}$$

To operate the RNPC converter in the half-bridge mode, S_7 and S_9 are turned on, resulting in an 'R' vector on leg b. The



(a)



(b)

Fig. 8. (a) Reconfiguration power loss based on the type of method; (b) Proposed gate pulse sequence to perform reconfiguration from 'O' to 'R' vectors, and vice versa.

reconfiguration power loss in a RNPC, $P_{hb(RNPC)}$ is seen in (5).

$$P_{hb(RNPC)} = 2i_{p(rms)}^2 R_{ds(on)} \tag{5}$$

The reconfiguration power losses in an active neutral-point clamped (ANPC) converter, $P_{hb(ANPC)}$ is seen in (6).

$$P_{hb(ANPC)} = i_{p(rms)}^2 R_{ds(on)} \tag{6}$$

Fig. 8(a) shows the comparison in the reconfiguration power loss of the NPC, RNPC, and ANPC converters when $R_{ds(on)}$ = 9 mΩ, R_d = 59 mΩ, and V_{T0} = 1.07 V. Comparing the losses when $i_{p(rms)}$ = 50 A, the losses are 245 W, 44 W, and 22 W, for the NPC, RNPC, ANPC converters, respectively. The losses of a conventional NPC converter are incomparable to the RNPC or the ANPC and make it unsuitable for topology morphing control at high RMS current levels. Multiple strategies have been proposed in the literature to increase the voltage range of resonant power converters; however, they utilize additional relays or contactors for reconfiguration [11, 25, 26]. The proposed reconfiguration method does not require any additional relays or contactors and is solid-state in nature. Reconfiguration on the high-frequency AC link via contactors create large loops that aggravate electromagnetic interference (EMI), and is avoided with the proposed solid-state method. This also improves the reliability of the application, since utilization of electromechanical devices with a fatigue life affected by vehicle vibrations is a cause of concern in an on-board charger application. Additionally, the RNPC converter saves the cost of one gate driver and MOSFET compared

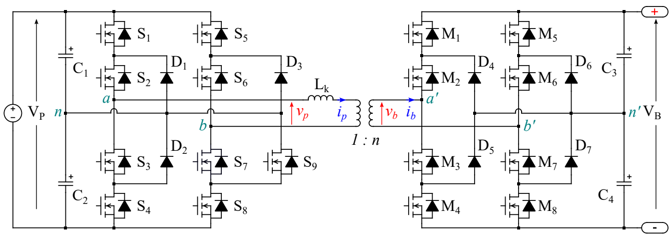


Fig. 9. Reconfigurable three-level dual active bridge converter (R3L-DAB) converter topology.

to using an ANPC converter, and provides a reconfiguration option with a lower switch-count in its comparison, thus providing a trade-off for cost-sensitive applications.

To switch the R3L-DAB between half-bridge and full-bridge modes, the modulation of the converter is ceased, and the RNPC's leg b is switched to the 'O' vector. Fig. 8(b) shows the recommended pulse sequence to switch from the 'O' vector to the 'R' vector (half-bridge mode) and vice versa. This sequence ensures that there are no transient over-voltages on the RNPC's leg b while the transition is performed.

B. Reconfigurable Three-Level Dual Active Bridge (R3L-DAB) Converter

Fig. 9 shows the construction of a reconfigurable three-level dual active bridge (R3L-DAB) converter topology. The stage fed by the input voltage, V_P, referred to as the primary side, is interfaced with a reconfigurable neutral-point clamped converter. The high-frequency link is generated using the system's total leakage inductance, L_k, and isolation transformer with a secondary to primary turns ratio, n. The secondary winding of the transformer is interfaced with a full-bridge neutral-point clamped converter that generates the output DC link, V_B and is referred to as the secondary side. $C_1 - C_4$ are the DC link capacitors, $S_1 - S_9$ are the MOSFETs of the primary RNPC converter, $M_1 - M_8$ are the MOSFETs of the secondary NPC converter, $D_1 - D_7$ are the clamp diodes. The DC link with the larger voltage swing is intended to interface with the primary side with the RNPC converter stage, which is connected to V_P.

Fig. 10 shows the operating modes of the R3L-DAB converter. The modulation scheme is defined as the following: the primary side can operate either in the full-bridge or the half-bridge mode, depending upon the state of the reconfiguration MOSFETs, S_7 and S_9. Fig 11(a) shows the R3L-DAB in the full-bridge mode. The gate command of switch S_9 is maintained at logic 0 to disable the MOSFET channel and only let its body diode be conducted to serve as a clamp diode. The voltage swing observed by the transformer primary, v_p is $\pm V_P$. Fig. 11(b) shows the R3L-DAB in the half-bridge mode, which is done by permanently turning on S_7 and S_9. This creates a permanent connection between nodes *'b'* and *'n'*; resulting in a maximum transformer voltage swing, v_p of $\pm V_P/2$. The primary excitation is limited to a two-level operation; however it can be further extended to a three-level (half-bridge) or five-level (full-bridge) operation to optimize the switching currents based on the available degrees of freedom [27]. The secondary excitation is controlled by two

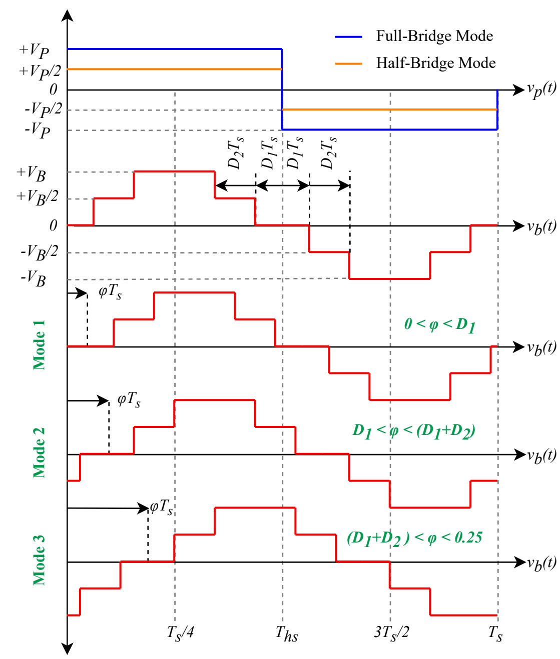


Fig. 10. Operating modes of the R3L-DAB converter.

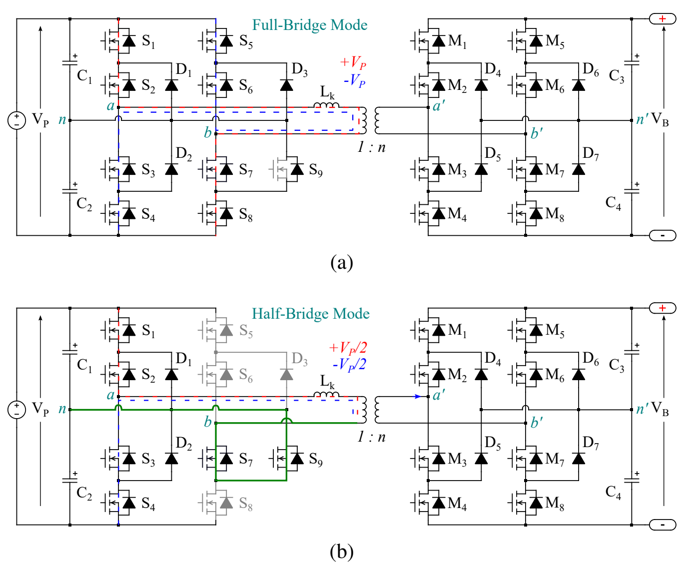


Fig. 11. (a) Reconfigurable three-level DAB in full-bridge mode; (b) Reconfigurable three-level DAB in half-bridge mode.

phase shifts, D_1 and D_2, and generates a five-level waveform $(+V_P, +V_P/2, 0, -V_P/2, -V_P)$. The power transfer between the two ports is controlled by the phase shift, φ between the primary and secondary bridge voltages, referenced to the primary's zero position.

The normalized values of all control variables, 0 - 1, translate as 0 - T_s seconds, or 0 - 2π radians. These control variables are bound by the following conditions: $-0.25 < \varphi < 0.25$ ($\varphi > 0$ to transfer power from V_P to V_B and $\varphi < 0$ to transfer power from V_B to V_P). $D_1 + D_2 \leq 0.25$. In order to facilitate power transfer from V_P to V_B, $\varphi > 0$ has been assumed for the analysis. Mode 1 refers to a condition when $0 < \varphi < D_1$. Mode 2 refers to a condition when

$D_1 < \varphi < (D_1 + D_2)$. Mode 3 refers to a condition when $(D_1 + D_2) < \varphi < 0.25$. Each of these modes is applicable when the R3L-DAB is operated either in the full-bridge or the half-bridge configuration.

C. Operating Principle

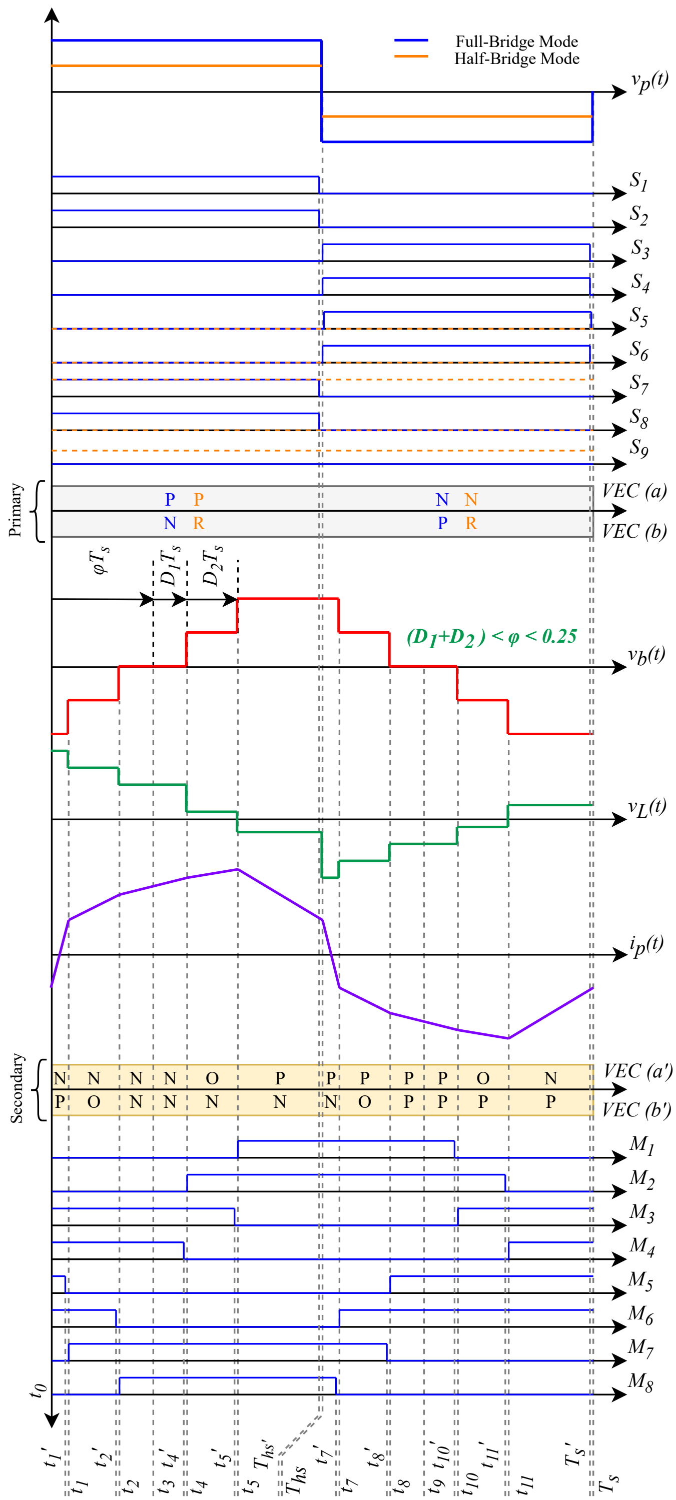


Fig. 12. Modulation scheme of the R3L-DAB converter in mode 3.

The modulation scheme of the R3L-DAB converter in operating mode 3, with the primary gating signals $S_1 - S_9$, secondary gating signals $M_1 - M_8$, transformer primary voltage v_p, inductor voltage v_L, secondary voltage v_b, and inductor current i_p are shown in Fig. 12. In the full-bridge mode, the relationship between the gating signals is as $S_1 = \overline{S_3}$, $S_2 = \overline{S_4}$, $S_5 = \overline{S_7}$, $S_6 = \overline{S_8}$, and is applicable for $M_1 - M_8$ in the same order. The complementary signals are separated by the dead time t_{dead} at the turn-off interval and are depicted in the intervals $t_x' - t_x$, where $x \in \{0..12\}$. t_6 is represented by the half-cycle period T_{hs}, and t_{12} is represented by the switching period T_s. The primary side, connected to the RNPC converter, can be operated either in full-bridge or half-bridge mode and is used to generate a two-level waveform. The secondary side, connected to the NPC converter, is operated in the full-bridge mode and generates a five-level waveform based on the symmetric modulation scheme defined in [28].

TABLE IV
SWITCHING CRITERION OF THE R3L-DAB CONVERTER IN MODE 3

Switch	Turn-on instance t_{on}	Turn-off instance t_{off}
$S_{1,2}$	0	T_{hs}
$S_{5,6}$	T_{hs}	T_s
$S_{5,6,8}$	Always off (half-bridge)	
$S_{7,9}$	Always on (half-bridge)	
M_1	$(\varphi + D_1 + D_2)T_s$	$(2\{\varphi + D_1\} + 1)T_{hs}$
M_2	$(\varphi + D_1)T_s$	$(2\{\varphi + D_1 + D_2\} + 1)T_{hs}$
M_5	$(2\{\varphi - D_1\} + 1)T_{hs}$	$(\varphi - D_1 - D_2)T_s$
M_6	$(2\{\varphi - D_1 - D_2\} + 1)T_{hs}$	$(\varphi - D_1)T_s$

The turn-on and turn-off criterion for the switches of the R3L-DAB converter in operating mode 3 for both full-bridge and half-bridge operation is summarized in Table IV. The relationship to the complementary switches in the bridge has been summarized in Section III-A. The specified modulation criterion is valid for mode 3 in the forward power mode $(0 < \varphi < 0.25)$, however, it can be mapped for realization on a digital signal processor (DSP) or field programmable gate array (FPGA) for modes 1, 2, and reverse power mode $(-0.25 < \varphi < 0)$ provided the necessary overflow conditions of the PWM modules are managed according to the implementation platform.

The current paths of the R3L-DAB in a full-bridge mode 3 operation are shown in Fig. 13(a)-(j) and Fig. 14(a)-(j). The direction of currents and the switches undergoing ZVS have been shown in the figures. The secondary side current paths and their intervals during the half-bridge mode 3 operation remain the same as Fig. 13(a)-(j) and Fig. 14(a)-(j), however the primary bridge current paths are shown in Fig A.1(a)-(d).

D. Steady-State Analysis

The closed-form solution of the steady-state instantaneous currents in the leakage inductance $i_p(t)$, the leakage inductance RMS current $i_{p(rms)}$, and the RMS currents in the various switches of the R3L-DAB based on the above mentioned modulation scheme are derived in this section. Due to the modulation of the R3L-DAB converter, there are discontinuities observed in the voltages seen by the primary and secondary bridges. The time instance t_x, where $x \in \{1..12\}$ is unique in all modes of operation. In all modes of operation, the time instances are defined as a function of D_1, D_2, φ and T_s. The instantaneous value of the current through an inductor can be

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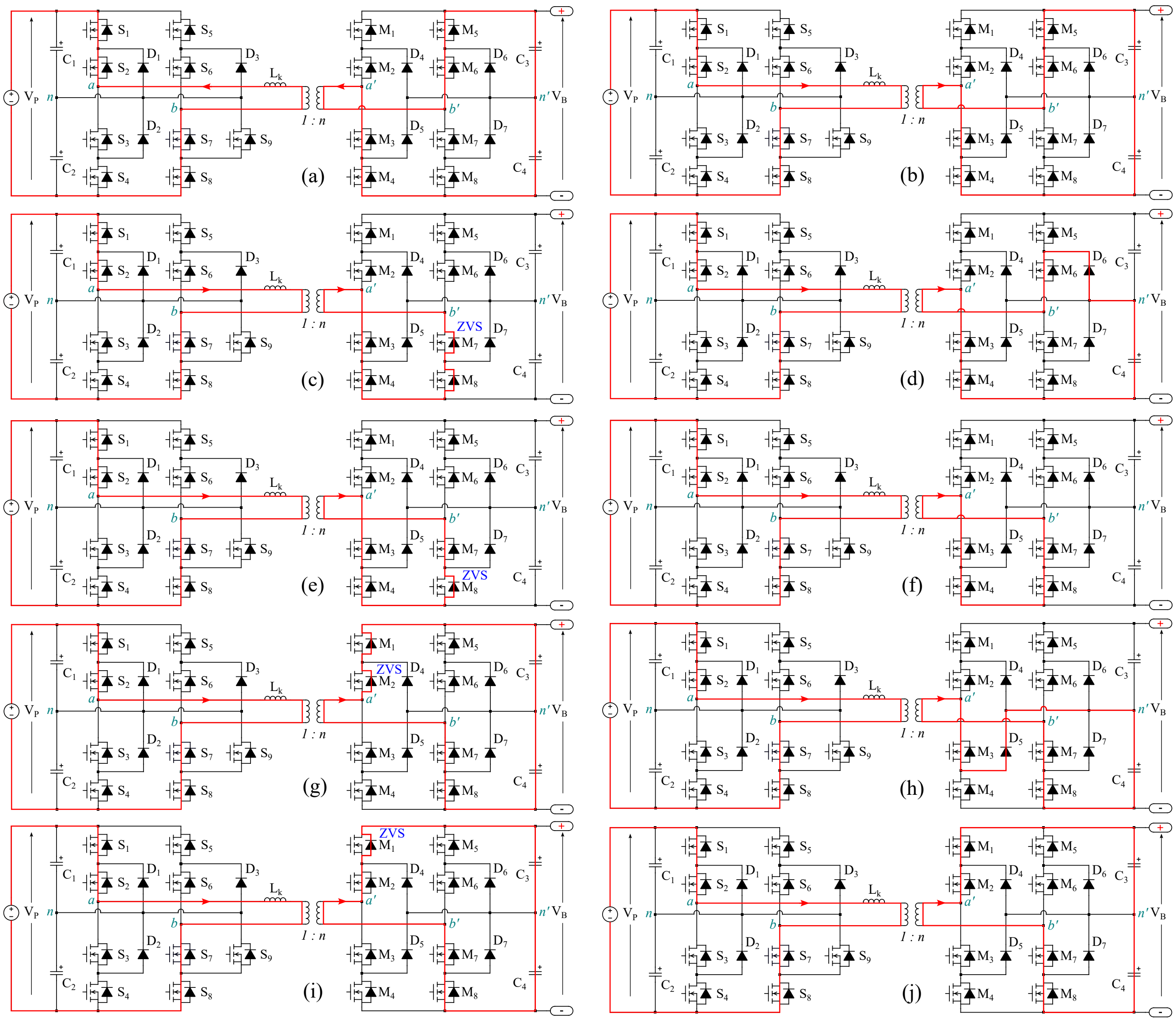


Fig. 13. Operation of the R3L-DAB in full-bridge Mode 3 $(D_1 + D_2) < \varphi < 0.25$, k_{cfg} = 1; (a) and (b) Current path from $t_0 - t_1'$, (c) Current path from $t_1' - t_1$, (d) Current path from $t_1 - t_2'$, (e) Current path from $t_2' - t_2$, (f) Current path from $t_2 - t_4'$, (g) Current path from $t_4' - t_4$ (h) Current path from $t_4 - t_5'$, (i) Current path from $t_5' - t_5$, (j) Current path from $t_5 - T_{hs}'$.

expressed by solving (7), (8), (9).

$$\frac{V_L(t)}{L_k} = \frac{\mathrm{d}i_p(t)}{\mathrm{d}t} \tag{7}$$

$$\frac{V_L}{L_k} = \frac{i_p(t_{x+1}) - i_p(t_x)}{t_{x+1} - t_x} \tag{8}$$

$$i_p(t_{x+1}) = i_p(t_x) + \frac{V_L}{L_k}(t_{x+1} - t_x) \tag{9}$$

Under the steady-state condition of the R3L-DAB converter, the average value of current through the leakage inductance is zero and is given by (10). Since the current through the inductor is half-wave symmetric, the condition shown in (11) is satisfied.

$$\left\langle i_p \right\rangle_{t=t_0}^{T_s} = 0 \tag{10}$$

$$i_p(t_0) = -i_p(T_{hs}) \tag{11}$$

Since the operation of the RNPC converter can be reconfigured between half-bridge and full-bridge mode, this can be reflected by choosing k_{cfg} = 0.5 for the half-bridge and k_{cfg} = 1 for the full-bridge mode.

The value of the inductor currents at various instances ($t_1 - t_6$) can be calculated by solving the simultaneous equations at $x = 0..6$ in (9), using the equality shown in (11). The solution of $i_p(t)$ in mode 3 of operation is shown in (12).

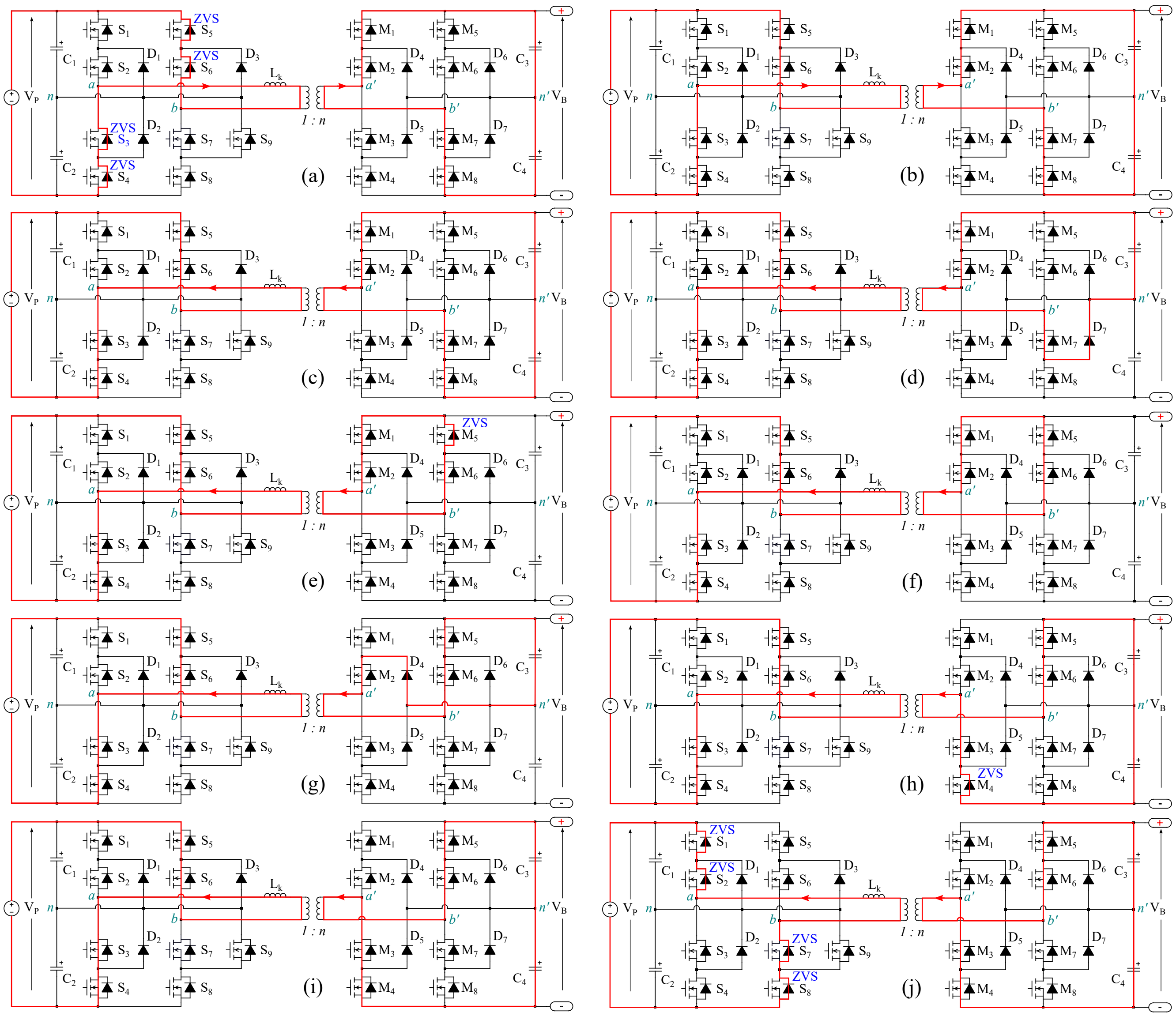


Fig. 14. Operation of the R3L-DAB in full-bridge Mode 3 $(D_1 + D_2) < \varphi < 0.25$, k_{cfg} = 1; (a) Current path from $T'_{hs} - T_{hs}$, (b) and (c) Current path from $T_{hs} - t'_7$, (d) Current path from $t'_7 - t'_8$, (e) Current path from $t'_8 - t_8$, (f) Current path from $t_8 - t'_{10}$, (g) Current path from $t'_{10} - t'_{11}$, (h) Current path from $t'_{11} - t_{11}$, (i) Current path from $t_{11} - T'_s$, (j) Current path from $T'_s - T_s$.

$$i_p(t) = \begin{cases} \frac{(1+D_2-2nD_2-4\varphi)V_B+(-1+2D_2)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \\ \frac{(-1+4D_1+3D_2+2nD_2)V_B+(1+4D_1+2D_2-4\varphi)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \\ \frac{(-1+4D_1+D_2+2nD_2)V_B+(1+4D_1-2D_2-4\varphi)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \\ \frac{(-1+4D_1+D_2+2nD_2)V_B+(1-2D_2-4\varphi)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \\ \frac{-(-1+4D_1+D_2+2nD_2)V_B+(-1+4D_1+2D_2+4\varphi)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \\ \frac{-(-1+4D_1+3D_2+2nD_2)V_B+(-1+4D_1+6D_2+4\varphi)nV_P k_{\text{cfg}}}{4nf_{sw}L_k} \end{cases} \quad \text{for } t = t_0 ... t_5 \tag{12}$$

The average power transferred between the DC links is given by (13). By solving $i_p(t)$ in modes 1, 2, and 3, the power transfer equations in their respective modes are given by (14), (15), and (16).

$$P_{out} = \frac{1}{T_{hs}} \int_{t_0}^{T_{hs}} v_p(t) i_p(t) \mathrm{d}t \tag{13}$$

$$P_{out,1} = \frac{V_P k_{\text{cfg}} V_B}{n f_{sw} L_k} (\varphi - 4D_1\varphi - 2D_2\varphi) \tag{14}$$

$$P_{out,2} = \frac{V_P k_{\text{cfg}} V_B}{n f_{sw} L_k} (\varphi - \varphi^2 - 2D_2\varphi - 2D_1\varphi - D_1^2) \tag{15}$$

$$P_{out,3} = \frac{V_P k_{\text{cfg}} V_B}{n f_{sw} L_k} (\varphi - 2\varphi^2 - 2D_1^2 - 2D_1 D_2 - D_2^2) \tag{16}$$

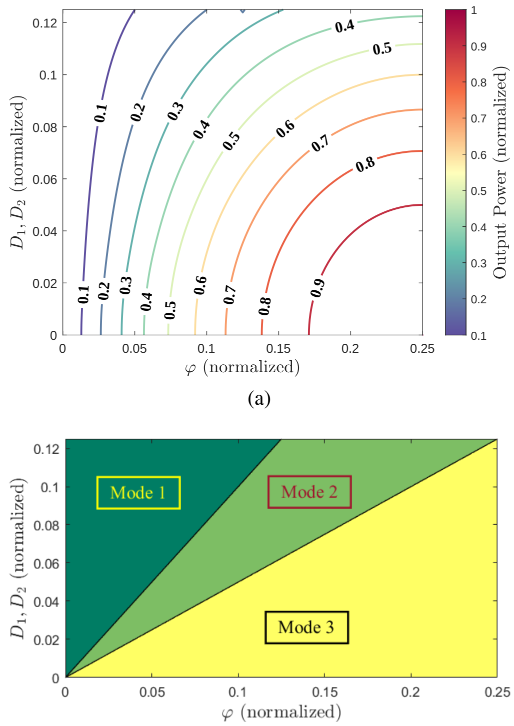


Fig. 15. (a) Output power variation of the R3L-DAB as a function of D_1, D_2, φ; (b) Mode variation of the R3L-DAB as a function of D_1, D_2, φ.

Fig. 15(a) shows the normalized output power variation when $0 < \varphi < 0.25$, $0 < D_1 < 0.125$, and $D_1 = D_2$, while Fig. 15(b) shows the mode variation under the same criterion.

The leakage inductance RMS current $i_{p(rms)}$ through the R3L-DAB converter is calculated using its general form as seen in (18). Solving for mode 3, the closed-form solution of $i_{p(rms)}$ is seen in (17).

$$i_{p(rms)} = \sqrt{\frac{1}{T_s}\int_{t_0}^{T_s} i_p^2(t)\mathrm{d}t} \tag{18}$$

The values of RMS current stress of various switches in the R3L-DAB converter can be calculated using the general form seen in (19), t_{start} and t_{stop} are the conduction intervals of the switch, dependent upon the mode of operation.

$$i_{S/M/D(rms)} = \sqrt{\frac{1}{T_s}\int_{t_{start}}^{t_{stop}} i_{S/M/D}^2(t)\mathrm{d}t} \tag{19}$$

Since the RNPC is operating in the two-level modulation scheme, and the switches $S_1 - S_8$ operate at a fixed duty cycle of 50%, the RMS current for these switches in the full-bridge mode is given by (19). In the half-bridge mode, (20) is applicable for $S_1 - S_4$, and $i_{S_7,S_9(rms)} = i_{p(rms)}$.

$$i_{S_1-S_8(rms)} = i_{p(rms)}\frac{1}{\sqrt{2}} \tag{20}$$

The closed-form solutions of the various RMS currents in the R3L-DAB converter are evaluated using the general form shown in (19), and the intervals shown in Table V. Equations (A.1), (A.2), (A.3) are used to calculate the RMS current stress on M_1, M_2, D_4, i.e. the NPC's leg a. Equations (A.4), (A.5), (A.6) are used to calculate the RMS current stress on M_5, M_6, D_6, i.e. the NPC's leg b. Fig. 16 and Table V show the comparison of the analytically modeled and simulated values of the RMS current stress in the R3L-DAB converter at the operating point where $D_1 = 0.028$, $D_2 = 0.028$, $\varphi = 0.12$, P_{out} = 15 kW, V_{PFC} = 300 V, V_{batt} = 1.25 kV. The mean value of the modeling error $\bar{\epsilon}$ = -0.26%, while the standard deviation of the modeling error σ_ϵ = 2.9%.

TABLE V
COMPARISON OF THE ANALYTICALLY MODELED AND SIMULATED RMS CURRENTS OF THE R3L-DAB CONVERTER IN OPERATING MODE 3

Section	t_{start}	t_{stop}	**Analytical** i_{rms}	**Simulation** i_{rms}	**Error** ϵ **(%)**
L_k	t_0	T_s	55.41	55.24	+0.31
$S_{1..8}$	t_0	T_{hs}	39.17	36.79	+6.47
M_1, M_4	t_5	t_{10}	12.60	13.14	-4.07
M_2, M_3	t_5	t_{11}	13.92	13.99	-0.50
D_4, D_5	t_{10}	t_{11}	4.63	4.82	+0.22
M_5, M_8	t_0 & t_8	t_1 & t_{12}	13.36	13.67	-2.27
M_6, M_7	t_0 & t_7	t_2 & t_{12}	13.96	13.99	-0.21
D_6, D_7	t_7	t_8	2.90	2.96	-2.03

E. Soft-Switching Criterion

The dual active bridge converter, due to the nature of its power decoupling impedance, does not contain a resonant tank, and hence deprives the ability to perform zero current switching (ZCS) naturally without using advanced modulation techniques. However, ZVS can be achieved by having a lagging current prior to the turn-on instant of the switch under consideration. The action of forward-biasing the body-diode of a MOSFET prior to turn-on enables a zero voltage turn-on. The ZVS criterion of the R3L-DAB converter while operating as a full-bridge in all modes of operation is shown in Table VI. Should the R3L-DAB converter be reconfigured as a half-bridge, the soft-switching criterion of $S_{3,4,5,6}$ is not applicable due to the permanent connection of leg b to neutral and the inactivity of these switches in the switching operation. The mentioned inequalities are required to be satisfied based on the mode of operation as the first step for achieving ZVS.

The action of ZVS, caused by the forward-biased body diode of the MOSFET, is due to the resonance between the leakage inductance and the MOSFET's output capacitance (C_{oss}). Depending upon the state of the bridge and whether inner-phase shifts are present based on the modulation scheme, the equivalent capacitance changes (21) [29].

$$0.5L_k I_{on}^2 > 0.5C_{eq}V_{eq}^2 \tag{21}$$

IV. Design of the R3L-DAB Converter

A. Optimization Procedure

The priority operating regions of a R3L-DAB operating in the Grid to Vehicle (G2V) operating modes can be determined based on the battery charging profile. The assumed charging

$$
\begin{aligned}
i_{p(rms)} = \frac{1}{4\sqrt{3}} \Bigg[\frac{V_P^2 k_{\text{cfg}}^2}{f_{sw}^2 L_k^2} \Bigg\{ & 1 - 4D_2(4D_1^2 + D_1(3+6D_2-8\varphi) + 2(D_2-2\varphi)(D_2-\varphi) - 3\varphi) + 2d(-1 + D_2^2(21-32D_2 \\
& -6n) + 4D_1^2(6-15D_2+2D_2 n-24\varphi) - D_2(-21+52D_2+6n+8D_2 n)\varphi + 4(6-9D_2+2D_2 n)\varphi^2 - 32\varphi^3 + D_1 D_2 \\
& (27-68D_2+6n+8D_2 n-16(6+n)\varphi)) + d^2 \Big[(1+128D_1^3+8D_1^2(-6+D_2(17+14n)) + 2D_1 D_2(-21-6n+ \\
& D_2(41+4n(15+n)) - 4\varphi + 8n\varphi) + D_2 \Big(2D_2^2(9+4n(7+n)) + 2(-1+2n)\varphi(-9+16\varphi) - D_2(-5+2n) \\
& (-3-6n-2\varphi+4n\varphi)\Big)\Big] \Bigg\} \Bigg]^{1/2}
\end{aligned}
\tag{17}
$$

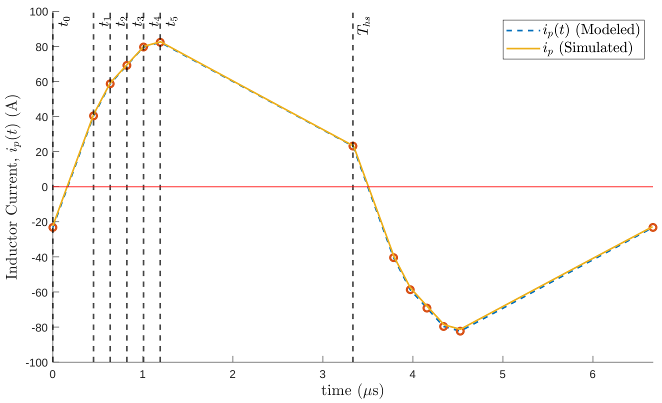


Fig. 16. Comparison of analytically modeled and simulated steady-state inductor current $i_p(t)$, (D_1 = 0.028, D_2 = 0.028, φ = 0.12, P_{out} = 15 kW, V_{PFC} = 300 V, V_{batt} = 1.25 kV.

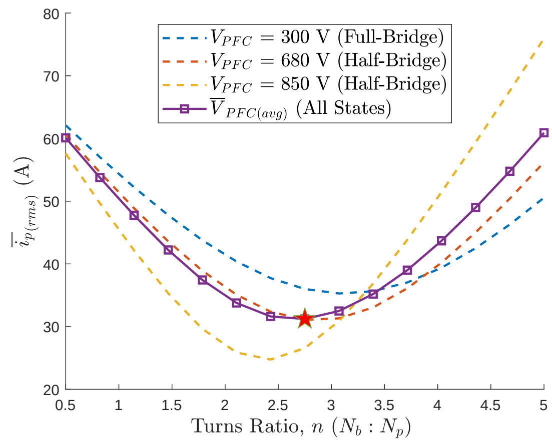


Fig. 17. Mean leakage inductance RMS current $\bar{i}_{p(rms)}$ as a function of turns ratio and variations in V_{PFC}.

TABLE VI
ZERO VOLTAGE SWITCHING (ZVS) CRITERION OF THE R3L-DAB IN ALL FULL-BRIDGE MODES OF OPERATION

Switch	**Mode 1**	**Mode 2**	**Mode 3**
	Soft-Switching Criterion		
$S_{1,2,7,8}$	$i_p(t_0) < 0$		
$S_{3,4,5,6}$	$i_p(T_{hs}) > 0$		
$M_{1,4}$	$i_p(t_3) > 0$	$i_p(t_4) > 0$	$i_p(t_5) > 0$
M_2	$i_p(t_2) > 0$	$i_p(t_3) > 0$	$i_p(t_4) > 0$
M_3	$i_p(t_8) < 0$	$i_p(t_9) < 0$	$i_p(t_{10}) < 0$
$M_{5,8}$	$i_p(t_5) < 0$	$i_p(t_7) < 0$	$i_p(t_8) < 0$
M_6	$i_p(t_4) < 0$	$i_p(t_5) < 0$	$i_p(t_7) < 0$
M_7	$i_p(t_{10}) > 0$	$i_p(t_{11}) > 0$	$i_p(t_1) > 0$

profile for a 1.25 kV/ 500 Ah battery pack is shown in Fig. 4. The operating point vector $\vec{OP} = f(V_{PFC}, V_{batt}, P_{batt})$ is discretized based on finite time intervals in the charging profile.

Selection of the turns ratio n, switching frequency f_{sw}, and leakage inductance L_k affects the average efficiency of the R3L-DAB converter. The normalized high-frequency link impedance Z_{norm} is calculated using (16), where the equation is evaluated at $\varphi = 0.5, D_1 = 0, D_2 = 0$. The value of the leakage inductance RMS current shall thus remain consistent while scaling the switching frequency.

$$
Z_{norm}\Big|_{\varphi=0.25}^{D_1,D_2=0} = \frac{V_{P(min)} V_{B(min)}}{8P_{out(max)}} \tag{22}
$$

The mean RMS current through the leakage inductance $\bar{i}_{p(rms)}$ is evaluated at Z_{norm} for every $\vec{OP}$ using (17). Since $D_1, D_2 = 0$, the modulation scheme is limited to two-level modulation on the secondary bridge. Lower RMS current is an indicator of higher utilization of the high-frequency link. The mean value of the RMS current $\bar{i}_{p(rms)}$ for $\vec{V_{PFC}}$ = [300, 680, 850] V and $\vec{k_{\text{cfg}}}$ = [1, 0.5, 0.5] is shown in Fig. 17, and its minima is observed at $n = 2.8$, which is the selected turns ratio of the converter.

Fig. 19 shows the algorithm used for the selection of the switching frequency and leakage inductance. To maintain the same $\bar{i}_{p(rms)}$ while scaling the switching frequency, the maximum leakage inductance $L_{k(max)}$ is given by (23).

$$
L_{k(max)}|_{f_{sw}} = \frac{V_{P(min)} V_{B(min)}}{8n f_{sw} P_{out(max)}} \tag{23}
$$

After the turns ratio is selected and the high-frequency link impedance is normalized, the RMS and peak current stress of the R3L-DAB will not change with variation in f_{sw}. The worst case analysis (WCA) results of the transformer primary RMS

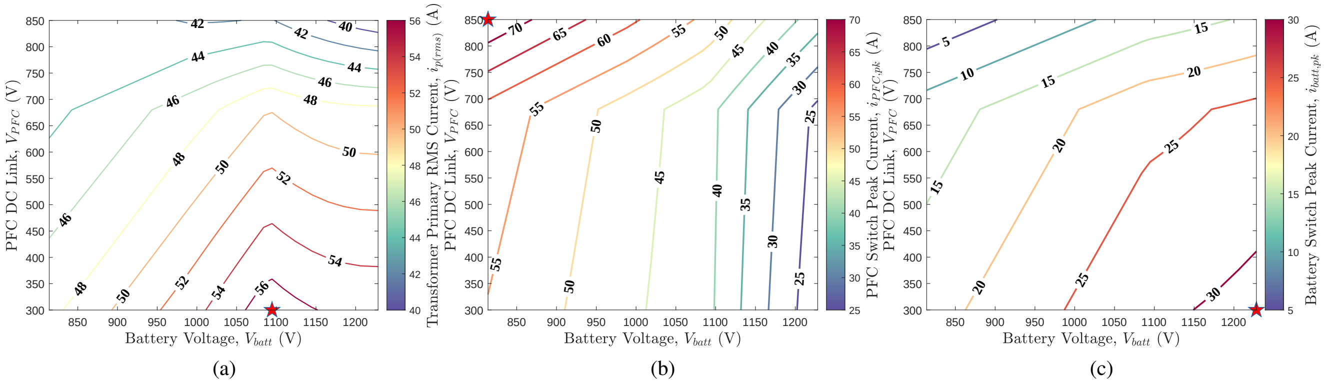


Fig. 18. Contour plots showing the current stress pattern for variations in V_{PFC} and V_{batt}, evaluated at P_{out} = 15 kW (a) $i_{p(rms)}$ (b) $i_{PFC,pk}$ (c) $i_{batt,pk}$.

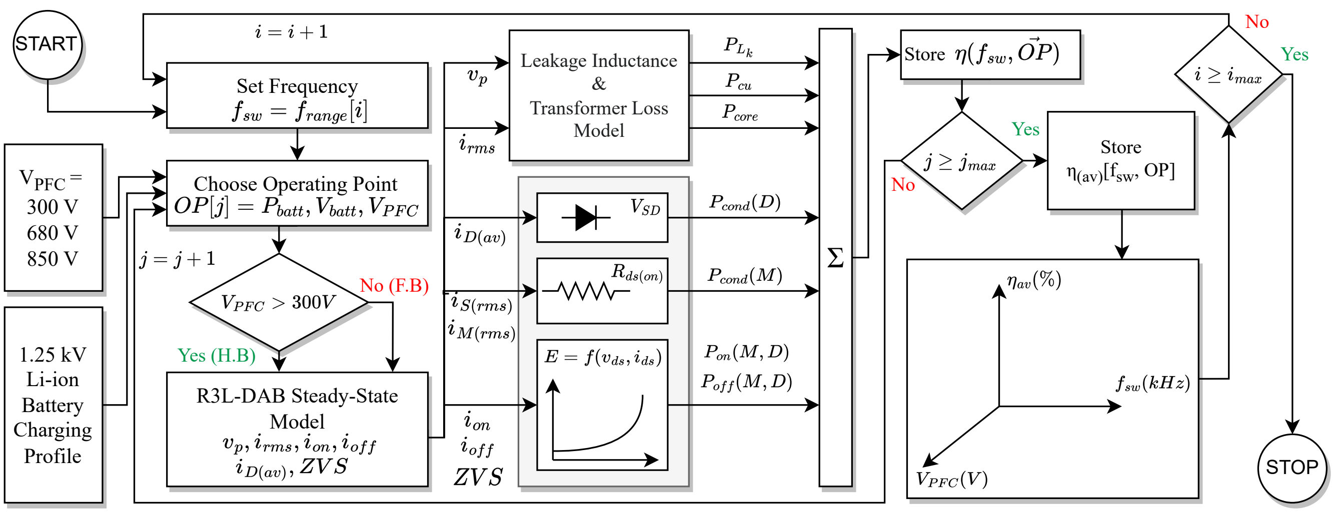


Fig. 19. Design framework for key parameter selection of the R3L-DAB converter.

current $i_{p(rms)}$, PFC switch peak current $i_{PFC,pk}$, and the battery switch peak current $i_{batt,pk}$ are shown in Fig. 18(a-c). The switching devices selected based on the worst-case stress analysis are UJ4SC075009K4S for the primary bridge and G3R20MT12K for the secondary bridge. The switching energy tables, $E_{on/off} = f(V_{ds}, I_{ds})$ are used in the design framework of the R3L-DAB converter.

B. Planar Transformer

The transformer core size and material is selected to be ELP 102/20/38 and N97 (TDK) based on the required power handling requirement of the R3L-DAB converter. The high-frequency link between the primary and secondary bridges is isolated using the transformer, with a secondary-to-primary turns ratio n. The turns ratio has been selected as n = 2.8. The number of primary winding turns N_p and its optimal value $N_{p,opt}$ can be evaluated at every frequency using (24), for which the symbol definitions are as follows: copper resistivity ρ, mean length per turn (MLT), number of layers per winding n_l, copper thickness t_{cu}, primary winding printed circuit board (PCB) trace width w_{pri}, secondary winding PCB trace width w_{sec}, core cross section area A_c, core effective volume V_e, and the Steinmetz coefficients of the core k_{fe}, α, and β.

$$N_{p,opt}(f_{sw}) = \min \Bigg(\underbrace{\mathrm{ceil}\left(\frac{N_p}{n}\right)^3 \frac{i^2_{p(rms)}}{n_l}\left(\frac{\rho \mathrm{MLT}}{t_{cu} w_{sec}}\right)}_{\text{Secondary Copper Loss}} \underbrace{N_p \frac{i^2_{p(rms)}}{n_l}\left(\frac{\rho \mathrm{MLT}}{t_{cu} w_{pri}}\right)}_{\text{Primary Copper Loss}} + \underbrace{k_{fe} f^{\alpha}_{sw}\left(\frac{V_{batt(max)}}{\mathrm{ceil}(nN_p) f_{sw} A_c}\right)^{\beta} V_e}_{\text{Core Loss}} \Bigg)$$
$$f_{sw} \in \{f_{sw(min)} \ldots f_{sw(max)}\}$$
$$N_p \in \{N_{p(min)} \ldots N_{p(max)}\} \tag{24}$$

Fig. 20 shows the variation of the optimal primary turns N_{opt} as a function of f_{sw}. The transformer is constructed using a set of two EE cores; B66297G0000X197 by TDK. The number of layers n_l = 10. The primary and secondary windings are separated by an FR-4 insulator, and the transformer is constructed using the methodology shown in [30]. The mag-

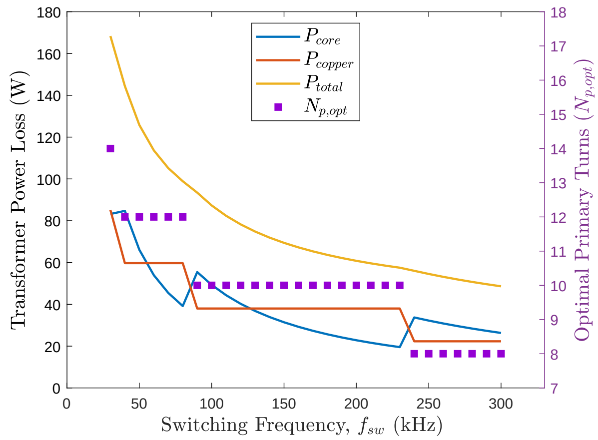


Fig. 20. Optimal primary turns $N_{p,opt}$ over variation in f_{sw}.

netostatic simulations to evaluate the parasitic capacitance of the transformer have been done using Ansys Maxwell. The detailed specifications of the transformer are mentioned in Table VIII.

C. Power Loss Model

This section describes the set of equations used to estimate the losses within various components of the R3L-DAB converter. The chosen operating point is evaluated using the steady-state analytical model to evaluate the instantaneous and RMS current values. The power loss equations of various components in the R3L-DAB are defined in Table VII. The symbols encountered for the first time are as follows: ZVS is a boolean and is 0 when ZVS the above-mentioned conditions for the operating point are true and is 1 when ZVS condition is false. E_{on} and E_{off} are the switching energy look-up tables, and are defined as a function of switched voltage and current. t_{dead} is the dead time between the transition of the complementary switches. V_{SD} is the forward voltage of the MOSFET's body-diode. V_F is the forward voltage of the clamp diodes, $I_{D(av)}$ is the average forward current through the clamp diode. R_p and R_s are the AC resistances of the transformer winding. V_e is the total core volume. $i_{c(rms)}$ is the capacitor RMS current. ESR_C and ESR_L are the equivalent series resistances of the capacitor and inductor, respectively.

D. Optimization Results

As shown in Fig. 19, the algorithm generates a three-dimensional space of the average efficiency η_{av}, as a function of the input voltage V_{PFC} and the switching frequency f_{sw}. The algorithm operates as follows; The switching frequency sweep is defined between $f_{sw(min)}$ = 25 kHz to $f_{sw(max)}$ = 300 kHz. At first, the operating point $\vec{OP}$ is selected based on the discrete point on the charging profile and the selected V_{PFC}. The operating point is passed through the R3L-DAB's steady-state model to calculate the steady-state instantaneous and RMS currents in the power converter. The steady-state current equations discussed in Section III-D and Appendix A are used to evaluate the various power losses in the R3L-DAB converter for estimating the efficiency at an operating point. The average efficiency of the R3L-DAB at a single

TABLE VII
POWER LOSS EQUATIONS OF THE R3L-DAB CONVERTER

Component	Loss Symbol	Equation (W)
S_x/M_y	$P_{cond(M)}$	$i^2_{rms}R_{ds(on)}$
	P_{on}	ZVS.$f_{sw}E_{on}(V_{ds}, I_{on})$
$x \in 1..9$	P_{off}	$f_{sw}E_{off}(V_{ds}, I_{off})$
$y \in 1..8$	$P_{cond(D)}$	$f_{sw}t_{dead}V_{SD}I_{on}$
D_x	P_d	$V_F I_{D(av)}$
$x \in 1..7$	P_{rr}	Neglected
Transformer	P_{cu}	$i^2_{p(rms)}R_p + (i_{p(rms)}/n)^2 R_s$
	P_{core}	$k_{fe}f^{\alpha}_{sw}\Delta B^{\beta}V_e$
Passives	P_L	$i^2_{p(rms)}ESR_L$
	P_C	$i^2_{c(rms)}ESR_C$

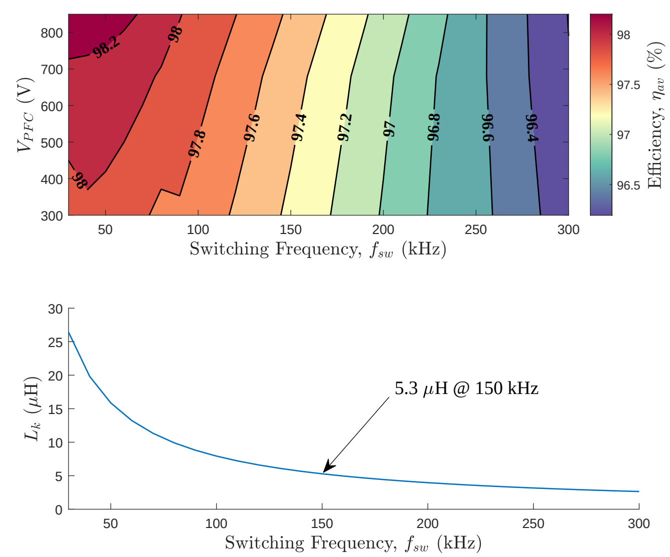


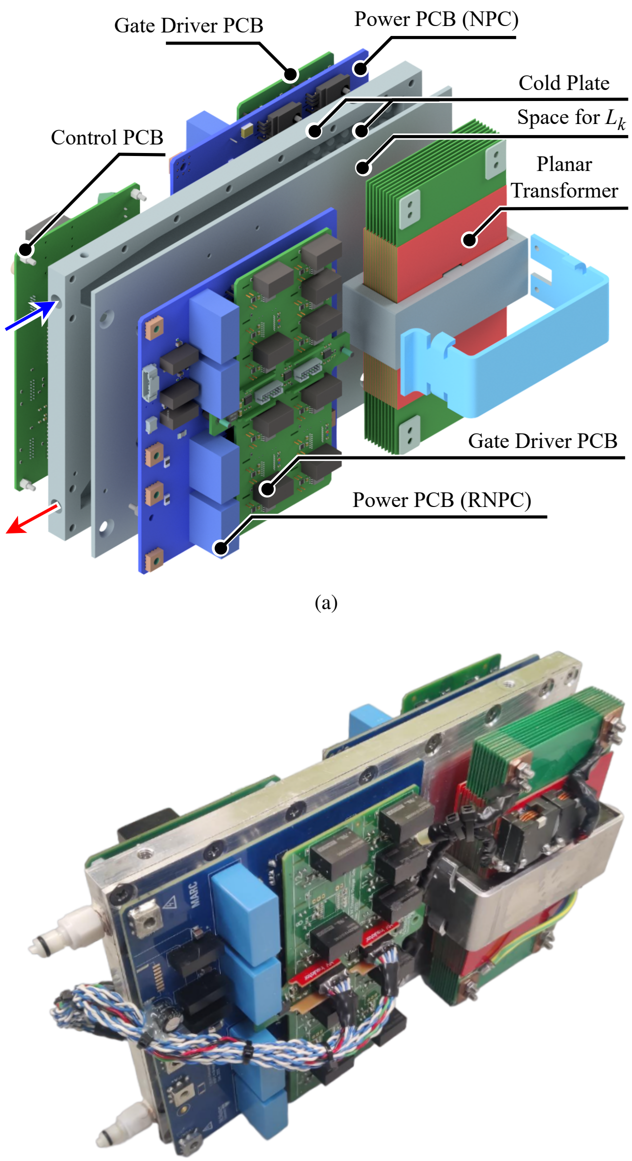
Fig. 21. Results of the average efficiency η_{av} evaluation.

input voltage, for varying V_{batt} and P_{out} is computed, while consequently calculating the efficiency for all values of V_{PFC} and f_{sw} to develop the trajectory map of the efficiency.

Fig. 21 shows the efficiency map of the R3L-DAB as a function of variation in the switching frequency and the PFC DC link voltage. It can be observed that the mean efficiency of this dataset is approximately 97%, and the increase in switching frequency of the R3L-DAB is not very detrimental to the average efficiency. However, the variation in required leakage inductance is minimal beyond an inflection point. To reduce the challenges in management of the system's leakage inductance, and not affect the power converter's control sensitivity, the leakage inductance is chosen at the inflection point of $\mathrm{d}L_k/\mathrm{d}f_{sw} < 0.5\mu$H/10 kHz, while also verifying the ability to fit the external leakage inductance into the power electronics package.

V. EXPERIMENTAL VERIFICATION

This section discusses the experimental results of the R3L-DAB converter, and focuses primarily on its efficiency



(a)

(b)

Fig. 22. (a) Exploded view of the hardware demonstrator of a 15 kW liquid-cooled R3L-DAB converter. (b) Prototype of the R3L-DAB converter.

TABLE VIII
REALIZATION DETAILS OF THE R3L-DAB CONVERTER

	Parameter	Specification
Key Specifications	V_{PFC}	300 - 850 V
	V_{batt}	890 - 1250 V
	$P_{out(max)}$	15 kW
	f_{sw}	150 kHz
	L_k	5.3 μH
	η_{peak}	97.32 %
Primary (RNPC)	SiC MOSET	UJ4SC075009K4S (Qorvo)
	$R_{ds(on)}/V_{ds(max)}$	9 mΩ/ 750 V
	$V_{gs(on)}/V_{gs(off)}$	+15 V/ -5 V
	$R_{g(on)}/R_{g(off)}$	3.3 Ω/ 5.6 Ω
	R_s/C_s	5 Ω/ 560 pF
	SiC Diode	MSC030SDA070K (Microchip)
	SiC Diode's V_F/I_D	700 V/ 30 A
Secondary (NPC)	SiC MOSET	G3R20MT12K (GeneSiC)
	$R_{ds(on)}/V_{ds(max)}$	20 mΩ/ 1200 V
	$V_{gs(on)}/V_{gs(off)}$	+15 V/ -5 V
	$R_{g(on)}/R_{g(off)}$	12 Ω/ 2 Ω
	SiC Diode	GD20MPS12A (GeneSiC)
	SiC Diode's V_F/I_D	1200 V/ 20 A
Power Board Components	DC link capacitor	5 μF/ 800 V
		B32774D8505K000 (EPCOS)
	Bypass capacitor	0.1 μF/ 1500 V
		C2225C104KFRAC (KEMET)
	Gate driver	1ED3322MC12N (Infineon)
	Iso. power supply	MGJ2D151505SC (muRata)
Transformer	Turns ratio (n)	28:10 (2.8)
	Core & material	ELP 102/20/38 & N97
		B66297G0000X197 (TDK)
	L_{mag}	768.08 μH at 1 kHz
	$L_{k,xfmr}$	1.17 μH at 1 kHz
	Copper thickness	6 oz/ft^2 (210 μm)
	PCB prepreg	FR-4 (0.35 mm)
	n_l per winding	10
	Insulator thickness	0.35 mm
	Insulator breakdown	4130 V_{peak}
Cold Plate	Dimensions	176 $\times$ 274 $\times$ 14 mm
	Flow rate	8 LPM
	Coolant	50% DI water/ ethylene glycol
Mechanical Dimensions	Dimensions	176 $\times$ 274 $\times$ 96 mm
	Power density (ρ_V)	3.25 kW/L or 53.25 W/in^3

evaluation. Fig. 22(a) shows the 3D exploded view of the hardware demonstrator of the 15 kW R3L-DAB converter, and Fig. 22(b) shows the realized prototype hardware. The power and gate driver PCBs are developed using Altium Designer. The layout of the power board has been optimized for minimum commutation loop inductance based on the study in [34]. The CAD modelling of the cold plate is done using Autodesk Inventor. The hardware demonstrator of the R3L-DAB converter measures 176 $\times$ 274 $\times$ 96 mm and achieves a volumetric power density (ρ_V) of 3.25 kW/L, or 53.25 W/in^3. This power converter is liquid-cooled and is designed at a flow-rate of 8 L/minute (LPM). The modulation scheme is developed on the Texas Instruments' TMS320F28379D digital signal processor (DSP) platform. Table VIII consolidates the information regarding the realization of the R3L-DAB converter.

The reconfiguration pulse sequence from full-bridge to half-bridge mode proposed in Section III-A is verified experimentally. Fig. 23(a), (b) show the experimental results of the dynamic reconfiguration test of a RNPC converter. The state of gate-source voltage V_{gs} of S_5, S_7, and S_8 remains unchanged during this test, and hence has not been measured during this test. Fig. 23(a) shows the observations of $V_{ds5,6}$ (upper switches), while Fig. 23(b) shows the observations of $V_{ds7,8}$ (lower switches) when V_P = 300 V. There is no unnatural transient voltage stress observed across any of the switches during both the transitions, thus verifying the efficacy of the proposed pulse sequence.

The Zimmer LMG671 Power Analyzer is used to measure the electrical efficiency of the R3L-DAB converter. The DC currents of the PFC and battery side are measured using the LEM IT 700-S and LEM IT 60-S ULTRASTAB current sensors, respectively. The efficiency measurements are performed for the following variation of the PFC voltage; $\vec{V}_{PFC}$ = [300, 400, 680, 850] V. The battery side voltage variation is done based on the minimum, nominal and maximum voltages of the battery pack; $\vec{V}_{batt}$ = [890, 1095, 1250] V. The efficiency is evaluated by connecting a resistive load across the V_B

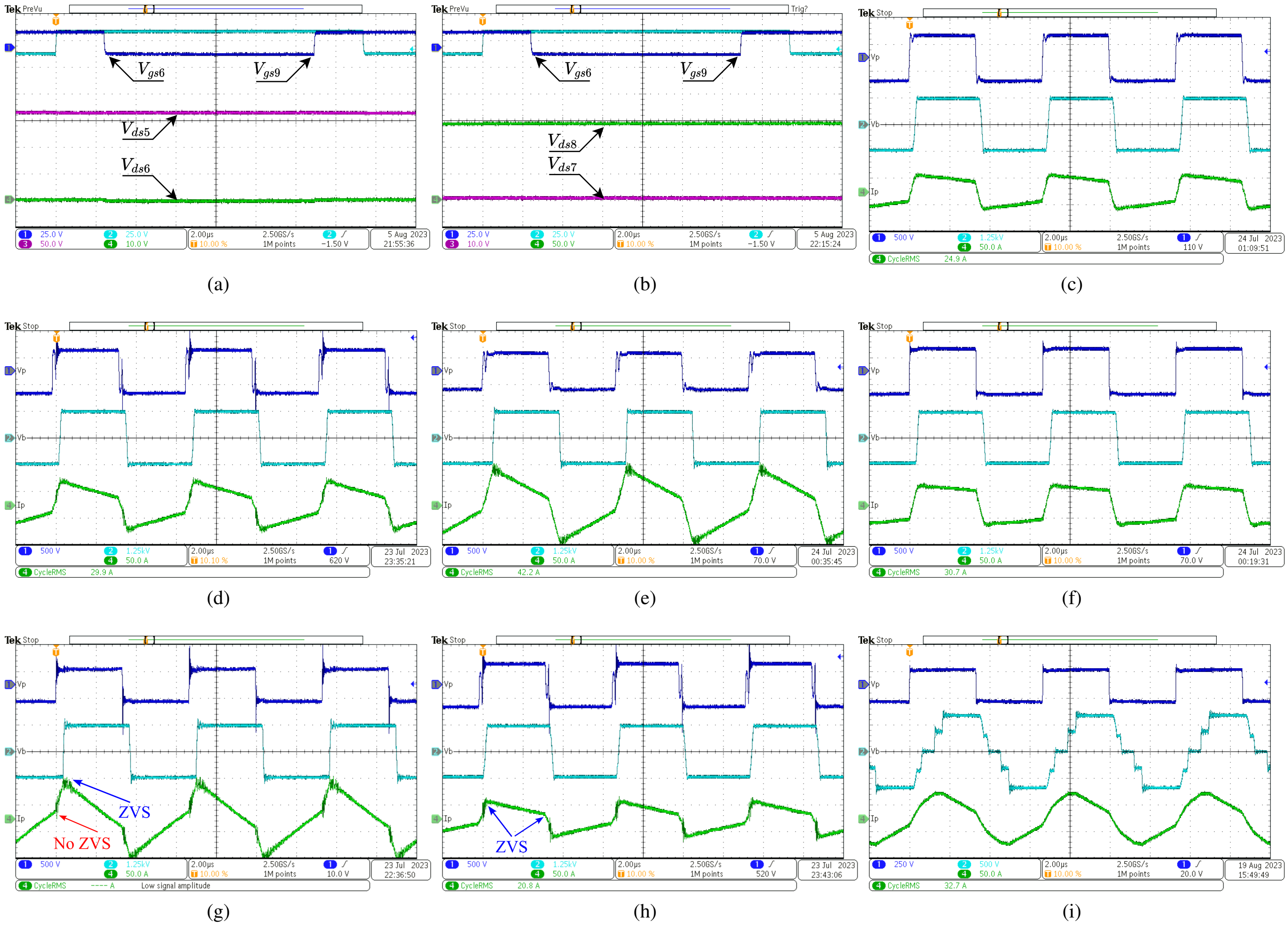


Fig. 23. Experimental waveforms of the reconfiguration test (vectors 'O' to 'R' to 'O') when V_P = 300 V on the RNPC's leg b; (a) S_5 and S_6; (b) S_7 and S_8. Experimental waveforms of the R3L-DAB converter (c) η_{peak} = 97.32%, V_{PFC} = 850 V, V_{batt} = 1.25 kV, P_{out} = 10.38 kW (half-bridge); (d) V_{PFC} = 400 V, V_{batt} = 1.25 kV, P_{out} = 10.38 kW (full-bridge); (e) V_{PFC} = 680 V, V_{batt} = 1.25 kV, P_{out} = 13 kW (half-bridge); (f) V_{PFC} = 850 V, V_{batt} = 1.25 kV, P_{out} = 13 kW (half-bridge); (g) and (h) V_{out} = 1.25 kV, P_{out} = 7.8 kW, V_{PFC} = 300 V (loss of ZVS) V_{PFC} = 400 V (full ZVS); (i) Five-level modulation on battery-bridge V_{PFC} = 150 V, V_{batt} = 690 V, P_{out} = 4 kW, D_1 = 0.05, D_2 = 0.06, φ = 0.14.

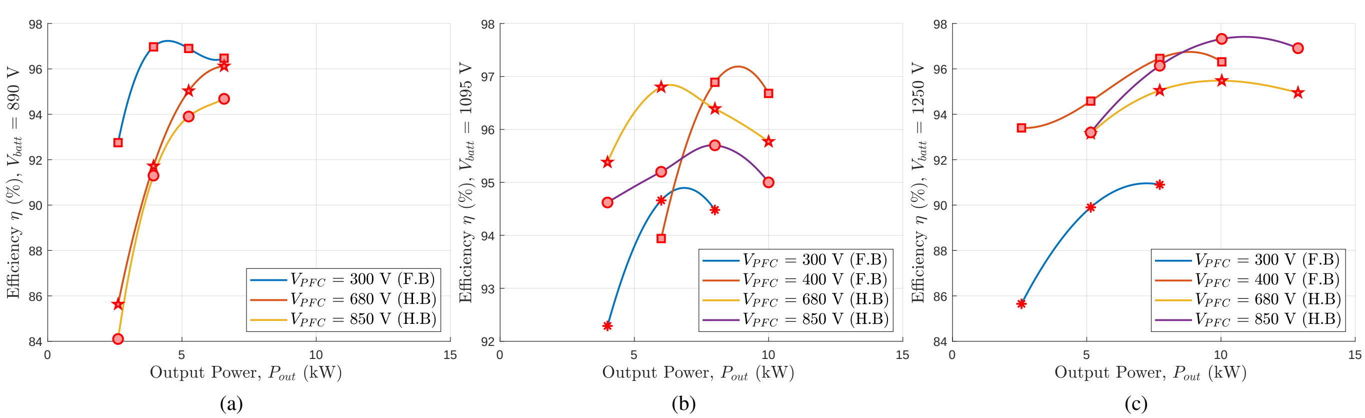


Fig. 24. Experimental efficiency map of the R3L-DAB converter under varying input voltage, output voltage, and power conditions; (a) V_{batt} = 890 V (b) V_{batt} = 1095 V (c) V_{batt} = 1250 V.

TABLE IX
COMPARISON OF THE PROPOSED WORK TO THE RECENT CONTRIBUTIONS IN EV CHARGING (ON-BOARD AND OFF-BOARD)

Ref.	Application	Topology	f_{sw} (kHz)	Switch	Power Density (kW/L)	Input Voltage (V)	Output Voltage (V)	η_{peak} (%)
[31]	On-board	PSFB	20	Si	-	760	420 - 760	98.3
[32]	On-board	LLC	47.2 - 100	Si	-	400	250 - 430	97.5
[33]	On-board	LCCL	88 - 120	SiC	-	400	250 - 450	97.4
[11]	Off-board	LCL-T	500	GaN	7.3	800	150 - 950	98.2
[14]	On-board	DAB	500	GaN	5.44	380	250 - 380	98
This work	**On-board**	**R3L-DAB**	**150**	**SiC**	**3.25**	**300 - 850**	**890 - 1250**	**97.3**

potential. The load resistance range varies from 1.2 kΩ to 120 Ω. Considering that the minimum achievable load resistance is 120 Ω, the efficiency maps are capped to 6.6 kW when V_{batt} = 890 V, 9.9 kW when V_{batt} = 1095 V, and 13 kW when V_{batt} = 1250 V.

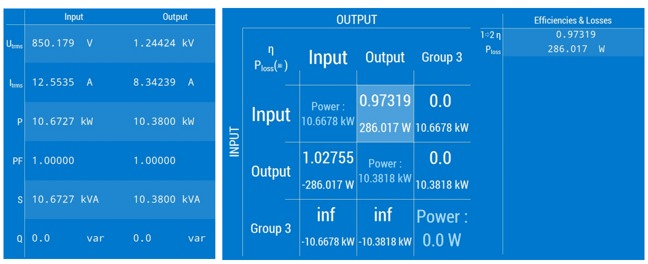


Fig. 25. Power analyzer measurements (Zimmer LMG671) at the peak efficiency point of η_{peak} = 97.32%.

Fig. 23(c) shows the waveforms at the peak efficiency point of V_{PFC} = 850 V, V_{batt} = 1.25 kV, P_{out} = 10.38 kW in the full-bridge mode, with an efficiency of 97.32%. Fig. 23(d)-(f) shows the operating waveforms when V_{batt} = 1.25 kV, while V_{PFC} = 400 V (full-bridge), 680 V (half-bridge), and 850 V (half-bridge). Fig. 23(g) and (h) show a comparative difference in operation when V_{batt} = 1.25 kV, P_{out} = 7.72 kW. It can be noted that the primary bridge loses ZVS when V_{PFC} = 300 V, while it is in full ZVS when V_{PFC} = 400 V. Based on the efficiency plot in Fig. 24(c), it can be observed that raising V_{PFC} by 100 V results in an efficiency improvement of +5.56 %. This is an opportunity to perform system-level coordination between the PFC stage and the dc/dc converter for maximizing the total efficiency as shown in [35]. Based on the efficiency simulations of the PFC stage, as shown in Fig. 5, and experimental result comparison at 300 V, 400 V, the projected efficiency at 300 V is 87.37%, while at 400 V is 91.78%, leading to an efficiency improvement of 4.4%.

The efficiency plots of the R3L-DAB converter across the input voltage, output voltage, and output power variations are shown in Fig. 24(a)-(c). It can be noted that the average efficiency of the R3L-DAB converter is approximately 95%, with varying input and output voltage. Due to the reconfiguration between half-bridge and full-bridge modes, the wide voltage variation of 300 - 850 V at the input does not cause a detrimental impact on the converter's efficiency. The peak efficiency η_{peak} = 97.32% is measured when V_{batt} = 1.25 kV, P_{out} = 10.38 kW. The efficiency of the R3L-DAB converter when P_{out} = 12.98 kW is 96.91%.

The results presented so far are shown while the R3L-DAB converter is operating under two-level, single-phase shift modulation ($D_1, D_2 = 0$) on both bridges for brevity in the development of the efficiency map. Fig. 23(i) shows the five-level, mode 3 operation of the R3L-DAB converter while operating in the full-bridge mode. To clearly identify the distinction in voltage levels, the control point is D_1 = 0.05, D_2 = 0.06, φ = 0.14. V_{PFC} = 150 V, V_{batt} = 690 V, P_{out} = 4 kW. At this operating point, the conversion ratio d = 1.64, yet the R3L-DAB exhibits an efficiency of 93%. The control variables can be further optimized for minimized conduction and switching losses using numerical optimization methods [27].

Table IX shows the comparison of recent contributions of dc/dc converters supporting EV charging, both on-board and off-board. The key difference is that the PFC stage voltage is fixed, and no variation is accounted for due to a fixed grid voltage: single-phase (on-board charging in North America), and three-phase for off-board charging. Additionally, the voltage range is limited to either 400 or 800 V EV powertrains. This work extends to accounting for a wide input voltage variation on the PFC stage's output (300 - 850 V), while catering to the voltage levels needed for the next generation of medium- and heavy-duty vehicles with 1.25 kV powertrains.

VI. CONCLUSION

This paper addresses an upcoming electrification challenge in North America pertaining to on-board charging of electric vehicles with 1.25 kV powertrains. The target application is medium- and heavy-duty vehicles that require on-board charging compliant with the SAE J3068 standard, and expect a wide variation in the available AC input voltage and a high-voltage battery charging capability. The key contributions are summarized below:

1) A novel reconfiguration method is proposed for the neutral-point clamped converter to switch between half- and full-bridge modes. The reconfigurable neutral-point clamped (RNPC) converter aids in the reduction of the conversion effort of the R3L-DAB converter. This method eliminates the need for additional relays or contactors, which are limited by a fatigue life and are a cause of concern in high-vibration automotive applications.
2) The steady-state analysis to derive the instantaneous and RMS currents, voltages, and zero voltage switching (ZVS) conditions under the defined modulation scheme is verified in the simulation.

3) A design procedure to select the turns ratio (n), leakage inductance (L_k), and switching frequency (f_{sw}) has been proposed. The achieved power density is 3.25 kW/L.
4) The experimental verification of a 15 kW R3L-DAB converter under varying input voltage, output voltage, and output power with test results across the entire voltage and power spectrum is presented. The peak efficiency at 10.38 kW is 97.32%, and the full-load efficiency is 96.91%.

Appendix A

Appendix A contains Fig. A.1(a)-(d) which discusses the current paths of the R3L-DAB in Mode 3, while the RNPC is configured as a half-bridge, as discussed in Section III-C. It also contains the closed-form solutions to the RMS current stress of the primary and secondary side switches and clamp-diodes of the R3L-DAB converter as seen in (A.1)-(A.6), which is discussed in Section III-D.

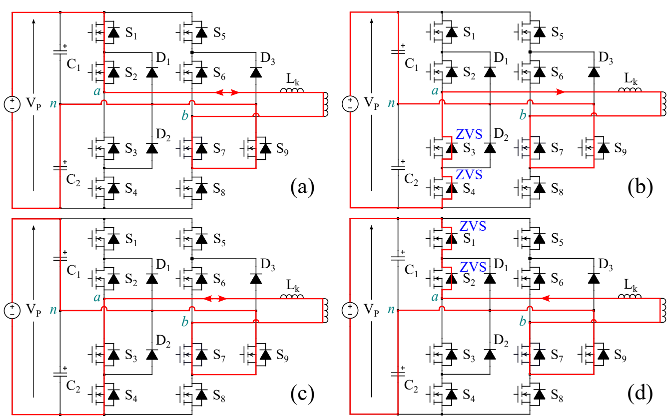


Fig. A.1. Operating of the R3L-DAB in half-bridge Mode 3 $(D_1 + D_2) < \varphi < 0.25$, k_{cfg} = 0.5; (a) Current path from $t_0' - T_{hs}'$, (b) Current path from $T_{hs}' - T_{hs}$, (c) Current path from $T_{hs} - T_s'$, (d) Current path from $T_s' - T_s$.

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$$
\begin{aligned}
i_{M1(rms)} = \frac{1}{4\sqrt{6}}\Bigg[\frac{V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&1 - 2D_2(3 + 64D_1^2 + 6D_2(-3 + 10D_2) - 36\varphi + 72D_2\varphi + 64\varphi^2 + 4D_1(-3 + 30D_2 + 16\varphi))\\
&+2d\Big[-1 + 6D_2(1 + 2D_2(-1 + D_2 - n + 4D_2 n)) + 8D_1^2(3 + D_2(3 + 2n) - 12\varphi) + 2D_2(-3 - 6n + 4D_2(-1 + 4n))\varphi\\
&+8(3 + D_2(-3 + 2n))\varphi^2 - 32\varphi^3 + 2D_1D_2(-9 + 6n + 4D_2(7 + 8n) - 16n\varphi)\Big] + d^2\Big[1 + 128D_1^3 + 16D_1^2(-3 + D_2(2 + 8n))\\
&+4D_1D_2(-1 + 2n)(-3 + D_2(7 + 2n) + 4\varphi) + D_2(-6 - 2D_2^2(7 + 4(-2 + n)n) + 3D_2(5 + 4(-1 + n)n)\\
&-4D_2(5 + 4(-3 + n)n)\varphi + 4(-1 + 2n)\varphi(-3 + 4\varphi))\Big]\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.1}
$$

$$
\begin{aligned}
i_{M2(rms)} = \frac{1}{4\sqrt{6}}\Bigg[\frac{V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&1 - 4D_2(3 + 4D_1 + 4D_2 - 4\varphi)(2D_1 + D_2 - 2\varphi) + 2d\Big[-1 - 40D_2^3 + 8D_1^2(3 + D_2(-9 + 2n)\\
&-12\varphi) + 8(3 - 4\varphi)\varphi^2 + 2D_2(-3 + 2n)\varphi(-3 + 4\varphi) - 8D_2^2(-3 + 7\varphi + 2n\varphi) + 2D_1D_2(15 + 6n + D_2(-44 + 8n)\\
&-16(3 + n)\varphi)\Big] + d^2\Big[1 + 128D_1^3 + 16D_1^2(-3 + 8D_2(1 + n)) + 4D_2^3(3 + 4n(4 + n)) + 4D_2(-1 + 2n)\varphi(-3 + 4\varphi) + 4D_1D_2\\
&(-9 - 6n + D_2(1 + 2n)(17 + 2n) - 4\varphi + 8n\varphi) - D_2^2(9 + 20\varphi + 4(-3 + n)n(-3 + 4\varphi))\Big]\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.2}
$$

$$
\begin{aligned}
i_{D4(rms)} = \frac{1}{4\sqrt{3}}\Bigg[\frac{D_1^2 V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&16D_1^2 + 3d^2(-1 + 4D_1 + D_1 + 2D_2 n)^2 + 12D_1(-1 + 2D_2 + 4\varphi) + 3(-1 + 2D_2 + 4\varphi)^2\\
&-6d(-1 + 4D_1 + D_2 + 2D_2 n)(-1 + 2D_1 + 2D_2 + 4\varphi)\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.3}
$$

$$
\begin{aligned}
i_{M5(rms)} = \frac{1}{4\sqrt{6}}\Bigg[\frac{V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&1 + 12D_2^2 - 8D_2^3 - 6D_2(1 + 4D_1 - 4\varphi)^2 - 2d\Big[1 + 28D_2^3 + 24D_1D_2(-1 + 2D_2(2 + n)) +\\
&8\varphi^2(-3 + 4\varphi) + 24D_1^2(-1 + 6D_2 + 4\varphi) - 6D_2^2(1 - 4n + 8n\varphi) + 6D_2(-1 + 8\varphi^2)\Big] + d^2\Big[1 + 128D_1^3 + 48D_1^2\\
&(-1 + D_2 + 2D_2 n) + 3(D_2 + 2D_2 n)^2 - 2D_2^3(1 + 12n^2) + 6D_2(-1 + 4(-1 + 2n)\varphi(-1 + 2\varphi))\Big]\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.4}
$$

$$
\begin{aligned}
i_{M6(rms)} = \frac{1}{4\sqrt{6}}\Bigg[\frac{V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&1 + 12D_2^2 - 2d\Big[1 + 24D_2^3 + 24D_2\varphi(-1 + 2\varphi) + 8\varphi^2(-3 + 4\varphi) + 24D_1^2(-1 + 2D_2 + 4\varphi)\\
&+24D_1D_2(-1 + 2D_2 + 4\varphi) + 6D_2^2(-3 + 2n + 8\varphi)\Big] + d^2\Big[1 + 128D_1^3 + 48D_1D_2(-1 + 2D_2(1 + n))\\
&+48D_1^2(-1 + D_2(3 + 2n)) + 3D_2(8D_2^2(1 + 2n) + D_2(-7 + 4(-1 + n)n) + 8(-1 + 2n)\varphi(-1 + 2\varphi))\Big]\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.5}
$$

$$
\begin{aligned}
i_{D6(rms)} = \frac{1}{4\sqrt{3}}\Bigg[\frac{D_2^2 V_P^2 k_{\mathrm{cfg}}^2}{n^2 f_{sw}^2 L_k^2}\Bigg\{&d^2(3 + 48D_1^2 - 12D_2(1 + n) + 24D_1(-1 + 2D_2(1 + n)) + D_2^2(13 + 12n(2 + n))) + 4(D_2^2\\
&+12(D_1 - \varphi)^2) + 3(1 + 8D_1 - 8\varphi) + 2d\Big[-3 + 48D_1^2 + 24D_1(D_2 + D_2 n - 2\varphi)\\
&+12\varphi + 2D_2(D_2 + 3(1 + n - 4(1 + n)\varphi))\Big]\Bigg\}\Bigg]^{1/2}
\end{aligned}
\tag{A.6}
$$

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