A Holistic Design Optimization Method for LLC Converters in Light Electric Vehicle Chargers

Abdulsamed Lordoglu, *Member, IEEE*, Mehmet Onur Gulbahce, *Member, IEEE*, Derya Ahmet Kocabas, *Member, IEEE*, Serkan Dusmez, *Senior Member, IEEE*

Abstract—The passive components of LLC resonance converters are traditionally designed based on a resonance frequency and switching frequency range considering required voltage conversion rate while ensuring zero-voltage-switching of the primary side power devices. Afterwards, the sub-elements such as transformer, power stage, and heat-sink are locally designed. However, this may only lead to locally optimized designs. In this paper, a systematic design framework is proposed that attempts to determine the resonance frequency by considering non-linear battery load profile, power loss, volume and cost of all main components. To achieve smaller sized transformer, a series connected primary and parallel connected secondary windings with a multi-core configuration is also considered. The proposed algorithm aids designers to optimally size the LLC, and provides a step-by-step design methodology. An LLC stage of a light electric vehicle battery charger converting 370 V- 430 V to an output voltage range of 36 V- 54 V rated at 3700 W with a peak efficiency of 98.2% has been designed validating the proposed design procedure.

Index Terms—Battery charger, electric vehicle, LLC resonance converter, magnetics, optimization, power converter.

I. INTRODUCTION

LC converter is a commonly used DC/DC resonance converter topology in converting high voltage to isolated low voltage in variety of applications. It has been demonstrated extensively that the design with LLC converter can achieve both high-efficiency and high-power-density [1]-[3]. LLC converters can switch under zero-voltage-switching (ZVS) for zero to rated load with a low turn-off current for the primary switches, while achieving zero current switching (ZCS) for the synchronous rectifiers (SRs) below resonance frequency. In addition to low power losses, soft turning-on allows minimizing the generated electromagnetic noise [3], [4]. In comparison to soft-switching PWM-controlled converters, LLC resonance converters can work at a higher switching frequency with higher efficiency particularly at light load, resulting in a higher power density [5]–[7]. However, the selection and design of components remain a difficult task, particularly for varying loads such as batteries in light electric vehicles (LEVs). These vehicles are defined by the industry as electric vehicles with a power range from 1 kW to 10 kW and voltage classes between 24 V and 72 V [8]. Within these voltage classes, the 48V category is commonly utilized, thus, this study has selected a 48 V output for the design in focus.

Serkan Dusmez is with the Power Management Solutions Department, WAT Motor Sanayi, Istanbul, Turkey (e-mail: serkan.dusmez@wat.com.tr) Manuscript received XXX, XX, 2015; revised XXX, XX, 2015. The common approach to design an LLC converter is to determine the switching frequency range and resonance frequency, and then select the magnetics, power switches and heat-sinks, accordingly [9]. The challenge with this approach is that the switching frequency is chosen based on designer's experience or availability of components without conducting a systematic design framework [10]. The downside of this design procedure is clear; the resonances elements such as resonance inductance (L_r) , magnetizing inductance (L_m) , and resonance capacitor (C_r) values, and corresponding core material and size for magnetics are not optimally selected. This approach hinders the power density as the total power losses and power density are determined based on the initially selected switching frequency range, and resonance frequency [11].

1

The optimization of LLC converters is more difficult than conventional PWM controlled converters due to their variety of operating modes and non-linear dynamics [12]. Many designs and optimization methodologies have been proposed for this type of converter in the past decades. Optimal design methods are developed based on the operation mode analysis in [12], [13], but these approaches require utilizing sophisticated calculation tools. A simple and highly accurate design procedure is presented in [14], but the wide output voltage range and load profile has not been discussed. Based on the characteristics of the battery charging profiles, time-weighted average efficiency index is proposed in [15], which represents the average weight of conversion efficiency during battery charging period. However, the presented design methodology only considers the power losses without taking cost and volume into account. The wide adjustable output voltage range for lithium-ion battery charger systems has been analyzed in [16]–[18] considering the charging profiles and corresponding worst-case scenarios for the primary side ZVS operation.

On the other hand, all these research efforts are only towards finding optimum resonance tank design under limited design criteria. To obtain optimal solution across multiple objectives with varying design frequency, the designers still require a multi-objective optimization method considering the design frequency, power losses, system cost and volume. A comprehensive optimization design procedure considering magnetic design, power switches and associated heat-sinks has not been proposed for LLC resonance converter operating under wide load range.

In this paper, a systematic design framework for LLC converter is proposed to find the optimal resonance frequency, minimum and maximum switching frequency limits that satisfy the required voltage gains at corresponding quality factors



Fig. 1. High level block diagram of the optimization of LLC converter.

by minimizing the system level fitness function. The high-level block diagram summarizing the proposed optimization tools is shown in Fig. 1. For each resonance frequency, satisfying L_r , L_m , and C_r values are calculated. For each calculated combination, a transformer and an inductor are designed based on the analytical models for every possible core in the database. Next, the transformer and the inductor are selected among the designed candidates, which minimizes the defined local fitness function. A key strength of this approach lies in its capacity to apply diverse fitness functions to local and system-level designs. In this approach, multi-core transformer configuration with primary windings in series and secondary windings in parallel is also considered instead of a single-core transformer as in the traditional LLC resonance converter. On the power stage side, the primary and secondary power switch losses for the devices in the database and the required heatsink sizes considering thermal resistances of the packages are calculated. After obtaining the design space, a system level fitness function consisting of power loss, system volume and cost is applied to find the most optimal resonance frequency together with the corresponding locally optimized L_r - L_m - C_r combinations and all other non-trivial components.

Different than the previous studies, the algorithm provides; 1) the magnetic design and switch selection has been carried out by considering total energy optimization based on the user charging profile as opposed to the worst-case scenarios or nominal point designs. All losses have been computed for these four operating points and weighted based on the different operating conditions, contributing to 50%, 20%, 20%, and 10% of the overall consideration, respectively [19], [20], 2) inclusion of thermal resistances of power switches and corresponding heat-sink volumes, 3) determination of optimal effective relative permeability for gapped magnetic cores in the database that is found by sweeping the operating flux density, 4) primary-series secondary-parallel connected multi-core transformer structure, 5) new derivations of current equations in relation to switching frequency, 6) a high level system fitness function consisting of power losses, system volume, and cost.

II. PROPOSED OPTIMIZATION ALGORITHM

The resonance tank design, which depends on the resonance frequency, determines the soft switching state. Smaller L_n (L_m/L_r) value provides higher gain for a constant quality factor (Q) value and moves the operation point away from the capacitive region providing ZVS turn-on for the primary switches. As the L_n decreases, the magnetization current increases causing an increase in the circulating current related conduction losses. Smaller Q value makes the gain higher, whereas higher Q may not meet the design requirements, and may transit the operation point to capacitive region. Therefore, a design optimization is required for LLC converters particularly in wide input and output voltage applications with dynamic load profile.

A. Effect of Battery Load on Design Optimization

The design requirements for an LLC resonance converterbased lithium-ion battery charger is significantly different than the regular passive load applications because of the nonlinear I–V characteristics of the battery load [18]. The charge process for a lithium-ion battery usually contains constantcurrent (CC) and constant-voltage (CV) charging stages, which are represented by four key points as shown in Fig. 2. At the beginning point, the input current drawn from the high voltage DC bus is the lowest in CC region; however, the switching frequency is highest due to required low voltage conversation ratio. The turning point marks the transition from CC to CV charging mode, and represents the region in which maximum power is transferred. The charging current in the CV stage is much smaller than that in the CC stage; hence, the lightload efficiency is more important for this stage. Because of these reasons, the designs optimized for a certain operating point may not be able to operate at other operation points. For instance, the circulating conduction losses may overheat



Fig. 2. Typical charging characteristics of a Li-ion battery cell and key operation points [21].

the power switches, or the magnetic core may be overheated due to core losses at high switching frequencies observed at the begining point. Similarly, a design made based on begining point may fail at the turning point due to reasons such as increased conduction loss on the secondary-side power FETs and transformer. Moreover, designs made for a single operation point may not be efficient at the other operating points.

In the presented design framework, all four key operation points are considered in the optimization process. Firstly, for a given resonance frequency, the switching range that covers the voltage conversation ratio of wide input and output voltage ranges is found. The power stage and magnetics are designed and evaluated at other operating points as well. The designs that do not meet the design criteria such as thermal limits and saturation flux density are eliminated. Furthermore, the designs are evaluated at all four operation points with different weights assigned to the fitness function for each operation point as

$$minimize \sum_{i=1}^{4} w_{OP,i} \cdot f\left(V_{bat_{OP,i}}, I_{bat_{OP,i}}\right)$$
(1)

where, $w_{OP,i}$ denotes the weights assigned to each operation point, and $f(V_{bat_{OP,i}}, I_{bat_{OP,i}})$ is the fitness function of each operation point in the local optimization loop. As a result, the proposed algorithm offers optimizing the design for a given operation point as well as across multiple operation points. In this study, the weight distributions have been defined as 50%, 20%, 20%, and 10% respectively. Significantly, our algorithm is inherently adaptable, allowing for the alteration of these weight distributions to accommodate specific user needs or distinct operating conditions.

B. Determination of Switching Frequency Range

The parametric analyzes are conducted by sweeping the L_n , Q, and resonance frequency (f_0) , which inherently determine the switching frequency range. Using the first harmonic approximation (FHA) method, L_r , L_m , and C_r values are expressed as

$$C_r = \frac{1}{2 \cdot \pi \cdot f_0 \cdot R_e \cdot Q_e} \tag{2}$$

$$L_r = \frac{1}{\left(2 \cdot \pi \cdot f_0\right)^2 \cdot C_r} \tag{3}$$

$$L_m = L_n \cdot L_r \tag{4}$$

3

where, R_e is the AC equivalent load resistance. The voltage gain (M) of the converter can be expressed in terms of frequency rate (F), L_n , and Q with the relationship given in (5).

$$M = \frac{1}{\sqrt{\left(1 + \frac{1}{L_n} \cdot \left(1 - \frac{1}{F^2}\right)\right)^2 + \left(\left(F - \frac{1}{F}\right) \cdot Q\right)^2}}$$
(5)

Here, F denotes f_s/f_0 . By rearranging (5) and solving for F, both the minimum and maximum switching frequency that would satisfy the minimum and maximum voltage conversion ratio in can be calculated as given in (6).

$$Q^{2} \cdot F^{6} + \left(\left(1 + \frac{1}{L_{n}} \right)^{2} - 2 \cdot Q^{2} - \frac{1}{M^{2}} \right) \cdot F^{4} + \left(\frac{-2}{L_{n}} \cdot \left(1 + \frac{1}{L_{n}} \right) + Q^{2} \right) \cdot F^{2} + \frac{1}{L_{n}^{2}} = 0$$
(6)

Some L_n and Q pairs may require a large switching frequency range to meet the required M of the application. To avoid inefficient results, the maximum frequency is limited to 1.8 times of the resonance frequency.

C. Transformer and Resonance Inductor Design

The magnetic model developed in this study designs locally optimized transformer and inductor according to the given L_m and L_r values, respectively, and provides these locally optimized magnetic designs to the system level optimization tool. Since high power LEV battery chargers generate high output currents, i.e. 68.5 A at 54 V battery voltage for a charger rated at 3700 W, it is a good practice to parallel transformers to decrease the current density on the secondary windings. On the other hand, the current density on the primary windings is not as high due to being fed from high bus voltage. This allows connecting the primary windings of transformers in series to lower the number of turns. Due to the difficulty in controlling the leakage inductance and the possibility of saturation of the magnetic material, a separate resonance inductor is designed instead of integrating it into the transformer core.

The transformer and inductor are designed for each L_n , Q and f_0 combination using the core database. This database comprises EE type cores associated with four distinct materials N87, 3C94, 3C95, and 3F36. Furthermore, these cores present in a spectrum of 16 different volumes, varying from 1490 mm³ (20/10/06) to 102000 mm³ (65/32/27), amounting to a total of 64 different core variants. The current density is calculated for the cores that are provided in the database as given in (7), where A_p is defined as the product of the core window area and the cross-sectional area, k_a and k_w are the coefficients. ρ_w is the resistivity of copper, and k_u is the window utilization factor. γ is the total losses except the DC copper loss. The typical values of k_a , k_w , k_u are 40, 10, 0.6, respectively [22].

$$J_0 = \sqrt{\frac{h_c \cdot k_a}{\rho_w \cdot k_w}} \cdot \sqrt{\frac{\Delta T}{k_u \cdot (1+\gamma)}} \cdot \frac{1}{\sqrt[8]{A_p}}$$
(7)

JOURNAL OF LATEX CLASS FILES, VOL. 14, NO. 8, AUGUST 2021

The cross-sectional areas of the primary and secondary (A_w) windings are calculated in (8) and (9), respectively. The cross-section areas are used to calculate the conductor dimensions.

$$A_{wp} = \frac{I_{Lr_{rms}}}{J_0} \tag{8}$$

$$A_{ws} = \frac{I_{sec_{rms}}}{J_0} \tag{9}$$

The AWG value closest to the calculated conductor dimensions is selected as the conductor diameter (r_{pri} , r_{sec}), and new current density values are updated for selected cross-section at standard AWGs. As a design constraint, the current density limit is set as 3.5 A/mm².

Since the design is optimized at multiple operation points according to the battery charging profile as detailed in Section II.A, the $I_{Lr_{rms}}$ requires to be expressed in relationship to the f_s . The $I_{Lr_{rms}}$ is the sum of the referred secondary current of the transformer referred to the primary side, and the magnetizing current (I_{Lm}) .

The resultant $I_{Lr_{rms}}$ expression that is valid for both below and above resonance operation is found as

$$I_{Lr_{rms}} = \sqrt{\frac{1}{48} \cdot \left(\frac{n \cdot V_o}{f_s \cdot L_m}\right)^2 + \frac{\pi^2}{8} \cdot \left(\frac{I_o}{n} \cdot \sqrt{\frac{f_0}{f_s}}\right)^2 - \beta}$$
(10)

where,

$$\beta = I_o \cdot \frac{V_o}{L_m} \cdot \frac{1}{2} \cdot \left(\frac{1}{f_s} - \frac{1}{f_0}\right) \tag{11}$$

Similarly, (12) expresses the secondary side rms current that is used to calculate the current density in the windings and Cu losses on the secondary side.

$$I_{sec_{rms}} = \frac{\sqrt{2} \cdot \pi \cdot I_o}{4} \cdot \sqrt{\frac{f_0}{f_s}} \tag{12}$$

The operating flux density is the paramount variable for gapped magnetic design, as various cores result in different loss coefficients for frequency and flux density. Therefore, it is taken as the main design variable in this study. The optimization algorithm sweeps the operating flux density, and calculates the optimal relative permeability (μ_{opt}), which allows utilizing the core optimally based on its power dissipation capability and saturation flux density (B_{sat}) limits.

$$\mu_{opt} = \frac{B_0 \cdot l_c}{\mu_0 \cdot \sqrt{\frac{P_d \cdot k_{up} \cdot W_a}{\rho_W \cdot \text{MLT}}}} \cdot \frac{I_{Lr_{rms}}}{I_{Lm_{max}}}$$
(13)

where,

$$I_{Lm_{\max}} = \frac{n \cdot V_o}{4 \cdot L_m \cdot f_s} \tag{14}$$

Since the air-gap (g) directly affects the operating flux density and the number of turns (N), the required N for the given L_m are calculated using the inductance-per-square (A_L) turn corresponding to the calculated optimal air-gap as given in (15)-(16).

$$g = \frac{l_c}{\mu_{opt}} \tag{15}$$

$$N = \sqrt{\frac{L_m}{A_L}} \tag{16}$$

4

The accurate estimation of leakage inductance in transformers is critical for LLC resonance converters because a wellmatched resonance frequency is required [23]. The leakage inductance referred to the primary, can be found from the energy stored in the magnetic field as in (17), where a is the winding length, b is the winding build, c is the insulation thickness.

$$L_k = \frac{\pi \cdot \text{MLT} \cdot N_p^2}{a} \cdot \left(\sum c + \frac{\sum b}{3}\right) \cdot \left(10^{-6}\right)$$
(17)

By using the calculated number of winding and conductor diameters, the DC resistance can be calculated by (18), where MLT is the mean-length-turn of the winding.

$$R_{dc} = \frac{N \cdot \rho_w \cdot \text{MLT}}{A_w} \tag{18}$$

The skin effect, which causes an increase in the resistivity of the copper as the effective conductive area is reduced at higher frequencies, is determined by (19). The skin depth is used in finding the AC resistance of round windings as given in (20), where σ is the conductivity of the conductor material, and r is radius of the winding. For foil windings, the AC resistance can be calculated as described in [24].

$$\delta = \frac{1}{\sqrt{\pi \cdot f_s \cdot \mu \cdot \sigma}} \tag{19}$$

$$R_{ac_{round}} = R_{dc} \cdot \left[1 + \frac{(r/\delta)^4}{48 + 0.8 \cdot (r/\delta)^4} \right]$$
(20)

After finding the AC resistances and current values, the copper and core losses are calculated by (21)–(22), where V_e is the volume of core. The Steinmetz equation is used for core loss calculation, and the C_m , α and β coefficients are derived by using the $P(W/mm^3) - B(mT)$ graphs for different frequency values given by the manufacturer data.

$$P_{cu} = R_{ac} \cdot (I_{Lr_{rms}})^2 \tag{21}$$

$$P_{core} = C_m \cdot f_s^{\alpha} \cdot B_{\text{sweep}}^{\beta} \cdot V_e \tag{22}$$

In order to estimate the temperature rise of the magnetic components, the thermal resistances of the cores are calcualted by the empirical formula given in (23) for natural convection cooling, and temperature rise is checked by using (24) [24]. The maximum temperature rise is restricted to 90 $^{\circ}$ C as a design constraint.

$$R_{\theta} = \frac{0.06}{\sqrt{V_c}} \tag{23}$$

$$\Delta T = \frac{P_{cu} + P_{core}}{R_{\theta}} \tag{24}$$

The optimization algorithm sweeps the operating flux density to find the optimal operating flux density across a large design space by minimizing a fitness function, which includes power loss, cost and volume of transformer and inductor. The cost includes core, winding and labor costs given in (25)–(27), where $\sigma_{core,x}$, $\sigma_{wdg,x}$ and $\sigma_{lab,x}$ are the specific costs per weight considering different magnetic core and the winding types. $\Sigma_{core,x}^{fc}$, $\Sigma_{wdg,x}^{fc}$ and Σ_{lab}^{fc} indicate the fixed costs for

JOURNAL OF LATEX CLASS FILES, VOL. 14, NO. 8, AUGUST 2021

the magnetic cores including the coil formers, connectors, and labor, where N_{stack} represents the stacking factor. The power loss includes core loss, temperature dependent copper loss, and AC winding loss due to the skin effect. More information on the magnetic design for gapped cores can be found in [25].

$$\Sigma_{core} = N_{stack} \cdot \Sigma_{core,x}^{fc} + \sigma_{core,x} \cdot W_{core}$$
(25)

$$\Sigma_{wdg} = \Sigma_{wdg,x}^{fc} + \sigma_{wdg,x} \cdot W_{wdg}$$
(26)

$$\Sigma_{lab} = \Sigma_{lab}^{fc} + \sigma_{lab,x} \cdot W_{wdg} \tag{27}$$

D. Power Switch and Heat-sink Selections

The first criteria in choosing a power device for the primary and secondary sides is to satisfy the ZVS operation. For the given design variables of L_m and f_0 , the energy stored in the magnetizing inductance must be sufficient to soft-switch the primary side FETs. Besides, in the dead-time period, the energy from the magnetic field, associated with the I_{Lm} , needs to charge and discharge the equivalent switch node capacitance (C_{eq}) . The minimum energy and dead-time required to ensure ZVS operation is are given in (28) and (29).

$$\frac{1}{2} \left(L_m + L_r \right) \cdot \left(I_{Lm_{\max}} \right)^2 \ge \frac{1}{2} \left(C_{eq} \right) \cdot V_{dc}^2$$
(28)

$$t_{dead} \ge 4 \times C_{eq} \times f_s \times L_m \tag{29}$$

where, C_{eq} is the equivalent capacitance referred to the switch node, which includes the total parasitic output capacitance of the primary side power devices, the total parasitic output capacitance of the secondary side power devices reflected to the primary side, the parasitic capacitance of the switch node traces as well as the transformer and inductor winding capacitances. For simplicity, C_{eq} has been taken equal to 4 x $C_{oss_{nri}}$ in literature [6]. Since the ZVS operation of the primary power switches are guaranteed by choosing appropriate power devices in accordance with (28), there are no power losses during turn-on. However, there are still conduction and turn-off losses occurring in the primary power switches. Since the duty cycle of the diagonal power switches are identical to that of the remaining diagonal power switches with 180° phase shift, the total power dissipation of the full-bridge leg can be found by

$$P_{cond_{pri,FB}} = 2 \cdot R_{dson_{pri}} \cdot I_{Lr_{rms}}^2 \tag{30}$$

Even though the turn-off power losses are not as high as the capacitive losses of a hard-switched converter, they can be considerably high when the switching frequency is low and magnetizing current is high. The total turn-off power losses are expressed as

$$P_{turn_{off,FB}} = 2 \cdot V_{bus} \cdot I_{Lr} \cdot t_{fall} \cdot f_s \tag{31}$$

where,

$$t_{fall} = (R_g + R_{gext}) \cdot C_{iss} \cdot \log\left(\frac{V_{plt}}{V_{th}}\right)$$
(32)

Here, R_g is the internal gate resistance, R_{gext} is the external resistance, C_{iss} is the effective input capacitance, V_{plt} is the gate plateau voltage, V_{th} is the threshold voltage. The other

frequency dependent power loss component is the gate drive loss, which is expressed as

$$P_{gate,FB} = 4 \cdot Q_g \cdot V_{gs} \cdot f_s \tag{33}$$

Another loss component, which may become significant in high frequency designs is the dead-time losses. Depending on the switching period, it is either inserted as a constant time or a percentage of the soft-switching time, and can be expressed as

$$P_{body_{diode,FB}} = 4 \cdot V_{sd} \cdot I_{sd} \cdot t_{bdc} \cdot f_s \tag{34}$$

Here, V_{sd} is the body diode voltage drop, I_{sd} is the average source to drain current during total body-diode conduction time (t_{bdc}) both during turn-on and turn-off. The total conduction losses on the secondary side synchronous switches of center-tapped configuration are expressed as

$$P_{cond,sec} = R_{dson,sec} \cdot I_{sec_{rms}}^2 \tag{35}$$

In the case of using SiC diodes, the total conduction losses per center-tap configuration are expressed as,

$$P_{cond,diode} = V_f \cdot I_o \tag{36}$$

Please note that I_o , and thereby, $I_{sec_{rms}}$ decrease proportionally with parallel number of transformers and power devices per each secondary side output stage. The secondary side synchronous devices are ZCS turned on and off at below resonance operation. In the above resonance operation, the secondary side power devices are turned on under current, where di/dt is limited by the loop and leakage inductances.

To calculate the heat-sink size required for each L_n , Q and f_0 combination, and thereby to choose the best power device and package, it is necessary to estimate the thermal resistance from the junction of the power device to the heat-sink. For this purpose, a MOSFET/SiC diode database from different manufacturers has been created along with package information. It is important to note that this extensive database encompasses 18 different switches for the primary side and another 16 switches for the secondary side. For total thermal resistance calculation, finite element analysis tools can be used; however, this requires heavy computation. For simplification, the theory on iso-flux rectangles and strips on compound flux channels as explained in [26] has been utilized for each layer. The die attached pad (DAP) thicknesses are dependent on the construction of die and the package, and whole thermal pad area is used for cooling and filled with vias that are 8 mils in diameter. This is because the power loop is not as critical in soft-switching converters as in hard-switching converters. It is considered that top and bottom Cu layer is 70 μ m thick, and total PCB thickness is 1.6 mm and vias are plated with 25 μ m Cu, and filled with conducting Epoxy.

For each power device in the database, the required heatsink is calculated based on the product of power losses and thermal resistances. A correlation between the heat-sink surface area and corresponding thermal resistance is obtained. Then, the heat-sink in the database that has closest surface area to this value is selected from the database, which comprises 72 different heat-sinks of varying sizes.

JOURNAL OF LATEX CLASS FILES, VOL. 14, NO. 8, AUGUST 2021

The costs of heat-sinks generally depend on the base material, volume and weight as well as the manufacturing and engineering costs. Heat-sink costs can be calculated in (37), where $\sigma_{sink,x}$ is the specific costs per volume depending on heat-sink type and $\Sigma_{sink,x}^{fc}$ is fixed costs which can result from additional engineering work and processing steps which are independent from heat-sink volume [27].

$$\Sigma_{sink} = \Sigma_{sink}^{fc} + \sigma_{sink,x} W_{sink} \tag{37}$$

E. Optimization Flowchart

After finding the volume, cost, power losses of the local best primary and secondary power devices as well as the transformer and inductor, the values are stored for the corresponding L_n and Q combination. In this way, a design space is created with locally optimized designs. The final selection of the design parameters is achieved by assigning weights to the volume, size and cost of the locally optimized designs and finding a global solution that minimizes the fitness function. The flowchart of the proposed framework is shown in Fig. 3.

III. RESULTS AND DISCUSSIONS

A 3700 W LLC converter with an input-output voltage range of 430V-370V and 54V-48V is designed using the proposed optimization framework under a 97% efficiency constraint. The algorithm sweeps the resonance frequency between 250-500 kHz at the outer loop, while the minimum and maximum frequencies are internally swept through L_n and Q sweeps. Both the weights of the local and system level fitness functions are chosen as 60%, 20%, and 20% for volume, power loss, and cost, respectively. Fig. 4(a) shows the design space considering magnetic designs achieved using every feasible core in the database for each resonance frequency and L_n -Q combinations. As it can be seen in Fig. 4, increase in f_0 decreases the total volume and cost of magnetic component; however, the power losses also increase. By applying a local fitness function to the magnetic model, the design space is further reduced.

The resultant design spaces in the case of using synchronous rectifier and SiC diodes on the secondary side are shown in Fig. 4(b) and Fig. 4(c), respectively. These points show the total volume, cost and efficiency of the converter for the local best designs at each swept resonance frequency. For high power design specifications, use of synchronous rectifier on the secondary side brings an advantage in efficiency and heat-sink volume, even though it increases the cost. The details of the design space with synchronous rectifier is provided in Fig. 5.

By applying the same fitness function applied locally to the whole design space, the optimum design parameters are



Fig. 3. Detailed flow chart of the system-level design procedure for LLC converter.

found as 37.52 μ H, 1.3 μ H, 9.38 μ H and 19.73 nF for L_m , L_k , L_r and C_r , respectively. The algorithm suggests using 40

TABLE I THE OPTIMUM TRANSFORMER AND INDUCTOR DESIGN PARAMETERS FOR L_m =37.52 μ H and L_r =9.38 μ H.

	Transformer	Number	Primary	Secondary	ΔB_{max}	Temperature	Air-gap	Primary	Secondary
Magnetics	Core	of Cores	Turn	Turn	(mT)	Rise (ΔT)	(mm)	$J (A/(mm^2))$	$J (A/(mm^2))$
Transformer	3F36-E422120	2	8	2	96.63	26.1	1.272	2.95	2.83
Inductor	3F36-E422115	1	10		101.06	43	3.942	2.95	



98.2 250kHz 98 Efficiency (%) 97.8 97.6 97 Selected 97.2 Design Point 500kHz 97 20 22 24 26 28 30 Cost (\$) (a) 250 Heatsink and Magnetic Volume (cm²) 250kHz 200 Selected Design Point 150 100 500kHz 50 20 22 24 26 28 30 Cost (\$) (b) 250 Heatsink and Magnetic Volume (cm³) 250kHz 200 Selected Design Point 150 100 500kHz 50 ∟ 97 97.5 98 Efficiency (%) (c)

Fig. 5. 2-D design space with synchronous rectifier on the secondary side; (a) efficiency-cost, (b) volume-cost, (c) volume-efficiency.

Fig. 4. 3-D design space; (a) magnetic model, (b) synchronous rectifier on the secondary side, (c) use of diodes on the secondary side.

m Ω / 650V and 7.2 m Ω / 150 V MOSFETs on the primary and secondary side, respectively. The optimal f_0 , f_s range and efficiency values for this optimized system are found as 370 kHz, 255.6 kHz- 610 kHz and 97.83%, respectively. For higher efficiency and smaller heat-sink size, two MOSFETs are paralleled; therefore, there are a total of eight devices on the secondary side. The core material is 3F36. The design parameters of the transformer and inductor are provided in Table I.

For detailed in-depth analysis, the volume, loss and cost for the primary and secondary FETs, the transformer and the inductor are provided with the radar chart given in Fig. 6(a), (b), (c). In order to observe the distribution of primary and secondary MOSFET power losses in more detail, the conduction and switching losses are shown in Fig. 6(d), (e). The results of the system level optimization tool are summarized with the radar chart given in Fig. 6(f).



Fig. 6. Radar chart for the optimal design point; (a) total volume, (b) total cost, (c) total power losses, (d) power losses on primary FETs, (e) power losses on secondary FETs, (f) system level results.

IV. EXPERIMENTAL RESULTS

A 3700 W/48 V LLC prototype has been designed to verify the theoretical calculations used in the optimization tool. The photo of the designed converter is shown in Fig. 7. Using the proposed optimization algorithm, the L_m , L_k , and L_r values were found as 37.52 μ H, 1.3 μ H, and 7.78 μ H, respectively. However, there is typically an error margin of 5-10% in manufacturing of wounded magnetics. The designed L_m , L_k , and L_r values have been measured as 35.245 μ H, 1.4 μ H and 8.2 μ H, respectively. Here, the loop inductance on the PCB enclosing the impedance network from the half-bridge is calculated approximately as 0.5 μ H [28]. Therefore, the resonance frequency has been experimentally obtained around 350 kHz. Fig. 8 shows the operation of LLC converter under different loads up to 3890 W. Here, V_{DS} is the drain-source voltage of primary device Q_2 , i_{Lr} is the current through resonance inductor L_r . As seen in Fig. 8, the primary side devices operate under ZVS in both full-load and light-load conditions over the entire switching frequency range. The oscillation that starts after $i_{Lr}=i_{Lm}$ is due to the resonance between the leakage inductance and secondary rectifier's junction capacitance in the below resonance region.

The gain curve obtained by the FHA analysis, simulation and experimental data at the nominal operation point are shown in Fig. 9(a). As seen from Fig. 9(a), the gain obtained from the simulations is very similar to that obtained by the experiments. Since the effects of harmonics other than the fundamental harmonics increase in the below resonance region, the gain obtained in this region from FHA is lower



Fig. 7. Prototype of the designed 400 V/48 V LLC resonance converter rated at 3700 W.

than that in simulation and experiment. Moreover, the lumped interwinding and intra-winding parasitic capacitances of the transformer impacts the voltage gain curve slightly.

The expected efficiency at the turning operation point, where the transferred power is maximum, had been provided by the proposed tool as 98%. The designed converter exhibits a peak efficiency of 98.2% at around 60% load and 98% efficiency at 80% load as shown in Fig. 9(b). Fig. 10 provides the thermal test results of the proposed LLC converter under

8



Fig. 8. Experimental waveforms for; (a) f_s =270 kHz, P_{in} =3890 W, (b) f_s =300 kHz, P_{in} =2927 W, (c) f_s =340 kHz, P_{in} =2265 W, (d) f_s =340kHz, P_{in} =1827 W, (e) f_s =400kHz, P_{in} =3430 W, (f) f_s =400kHz, P_{in} =3100 W.



Fig. 9. Converter characteristics; (a) gain curve comparison at nominal operation point, (b) measured efficiency.

natural convection cooling switched at 340 kHz transmitting a power of 2200 W at 25 °C ambient temperature. The highest temperature is 66.1 °C and occurs on the primary devices. As predicted by the optimization tool, 3700 W is achieved by 200 LFM cooling providing a maximum of 60 °C temperature rise on the FETs.

To demonstrate the benefits of the suggested method, the recommended optimization technique has been implemented using volume-weighted design parameters for two benchmark designs presented in [29] and [30] with 3 kW output power and an output voltage range of 48-54V. Efficiency, boxed volume, and cost are compared for each design, and the results are displayed in Fig. 11 as stacked bar charts. As the algorithm aims to minimize design volume, it achieves a slightly lower full load efficiency (98.1%) compared to [30] (98.4%), but significantly higher than [29] (95.3%). Additionally, it suggests a much smaller boxed volume of 343 cm³, in contrast to the



Fig. 10. Thermal test results at 2200 W under natural convection cooling.



Fig. 11. Comparison of the proposed algorithm results with prototypes in [29] and [30] for a 3 kW design; (a) efficiency, (b) volume, and (c) cost.

volumes of [29] and [30], which are 740 $\rm cm^3$ and 452 $\rm cm^3,$ respectively.

The improvement in volume can also be observed separately for each design in the figure, specifically in terms of the magnetic components' volume, which comprises the total volume of the high-frequency transformer and the resonant inductor. Moreover, the proposed algorithm yields highly satisfactory results in terms of cost. The design in [30] is the most expensive due to the utilization of 16 switches in the secondary part and four magnetic components, including two parallel transformers and two series inductors. As a result, the cost of [30] serves as the base value for comparison and is considered as 1 pu. In contrast, [29] has the most cost-effective magnetic design, as the transformer's leakage inductance is used as a resonant inductor. However, due to the use of 8 MOSFETs with very small R_{dson} values on the secondary side, the total cost of the [29] design rises dramatically to 0.83 pu. Finally, the proposed design's cost is determined to be 0.7 pu, making it the most affordable option with 2 parallel transformers, a resonant inductor, and 8 MOSFETs on the secondary side.

V. CONCLUSION

In this study, a systematic design approach has been presented for LLC converter that determines the resonance frequency, minimum and maximum switching frequency limits

that satisfy the quality factors at corresponding voltage gains of a LEV battery charger by minimizing the system level fitness function for optimum design. During the design and optimization process L_r , L_m , and C_r values have been calculated for each resonance frequency. For each L-L-C combinations, a transformer and an inductor considering distributed core structure have been designed based on the developed analytical models for every possible core in the database. Among the designed candidates, the magnetic designs that minimize the local fitness function are recorded. For the operation conditions of each combination, the primary and secondary power device losses have been analytically calculated, and the required heat-sink volumes are estimated by using thermal models of bottom-side cooled devices cooled by mounting heat-sinks on a 4-layer 1.6 mm thick PCB.

After obtaining a design space, a system level fitness function including volume, efficiency and cost has been applied to find the optimal design. The proposed framework is essential to size the LLC converter optimally based on the given weights between cost, size and efficiency considering the load profile of a LEV battery charger. A 3700 W/48 V LLC prototype has been designed based on the outcome of the proposed framework, where minimum peak efficiency was constrained to 97%. The designed prototype achieves a peak efficiency of 98.2% at 60% load.

ACKNOWLEDGMENTS

This work was supported in part by European Union's Horizon 2020 Research and Innovation Programme under the Marie Sklodowska-Curie under Grant 101031029 and in part by the 2232 International Fellowship for Outstanding Researchers Program of TUBITAK under Grant 118C374.

REFERENCES

- D. Shu and H. Wang, "Light-Load Performance Enhancement Technique for LLC-Based PEV Charger Through Circuit Reconfiguration," in IEEE Transactions on Transportation Electrification, vol. 7, no. 4, pp. 2104-2113, Dec. 2021, doi: 10.1109/TTE.2021.3078771.
- [2] C. Shi, H. Wang, S. Dusmez and A. Khaligh, "A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage Range," in IEEE Transactions on Industry Applications, vol. 53, no. 1, pp. 501-511, Jan.-Feb. 2017, doi: 10.1109/TIA.2016.2605063.
- [3] F. C. Lee, Shuo Wang, Pengju Kong, Chuanyun Wang and Dianbo Fu, "Power architecture design with improved system efficiency, EMI and power density," 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008, pp. 4131-4137, doi: 10.1109/PESC.2008.4592602.
- [4] Y. Liu, H. Wu, S. Ni, Y. Song and F. Yang, "Lower-Height-Oriented Magnetic Integration Design for Onboard Power Converter of Electric Vehicles," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2023.3259148.
- [5] A. Khaligh and S. Dusmez, "Comprehensive Topological Analysis of Conductive and Inductive Charging Solutions for Plug-In Electric Vehicles," in IEEE Transactions on Vehicular Technology, vol. 61, no. 8, pp. 3475-3489, Oct. 2012.
- [6] D. Fu, B. Lu and F. C. Lee, "1MHz High Efficiency LLC Resonant Converters with Synchronous Rectifier," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 2007, pp. 2404-2410, doi: 10.1109/PESC.2007.4342388.
- [7] H. Wang, S. Dusmez and A. Khaligh, "Design and Analysis of a Full-Bridge LLC-Based PEV Charger Optimized for Wide Battery Voltage Range," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1603-1613, May 2014.

- [8] N. Jolly, A. Chandwani and A. Mallik, "Sliding Mode Control of a 2-MHz All-GaN based 700W 95.6% Efficient LLC Converter," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2022.3230929.
- [9] R. Beiranvand, B. Rashidian, M. R. Zolghadri and S. M. H. Alavi, "Using LLC Resonant Converter for Designing Wide-Range Voltage Source," in IEEE Transactions on Industrial Electronics, vol. 58, no. 5, pp. 1746-1756, May 2011, doi: 10.1109/TIE.2010.2052537.
- [10] Huang, Hong. "Designing an LLC resonant half-bridge power converter." 2010 Texas Instruments Power Supply Design Seminar, SEM1900, Topic. Vol. 3. 2010.
- [11] C. Sun, R. Wang, X. Xiao, Y. Wang and Q. Sun, "Model-free Bidirectional Synchronous Rectification Control Scheme for LLCbased Energy Storage System in Electric-Vehicle Energy Router," in IEEE Transactions on Transportation Electrification, 2022, doi: 10.1109/TTE.2022.3212686.
- [12] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. -K. Ling and J. Lam, "Computer-Aided Design and Optimization of High-Efficiency LLC Series Resonant Converter," in IEEE Transactions on Power Electronics, vol. 27, no. 7, pp. 3243-3256, July 2012, doi: 10.1109/TPEL.2011.2179562.
- [13] X. Fang, H. Hu, J. Shen and I. Batarseh, "An optimal design of the LLC resonant converter based on peak gain estimation," 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2012, pp. 1286-1291, doi: 10.1109/APEC.2012.6165984.
- [14] C. Adragna, S. De Simone and C. Spini, "A design methodology for LLC resonant converters based on inspection of resonant tank currents.," 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008, pp. 1361-1367, doi: 10.1109/APEC.2008.4522901.
- [15] Z. Fang, T. Cai, S. Duan and C. Chen, "Optimal Design Methodology for LLC Resonant Converter in Battery Charging Applications Based on Time-Weighted Average Efficiency," in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5469-5483, Oct. 2015, doi: 10.1109/TPEL.2014.2379278.
- [16] J. Deng, S. Li, S. Hu, C. C. Mi and R. Ma, "Design Methodology of LLC Resonant Converters for Electric Vehicle Battery Chargers," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1581-1592, May 2014, doi: 10.1109/TVT.2013.2287379.
- [17] H. Xu, Z. Yin, Y. Zhao and Y. Huang, "Accurate Design of High-Efficiency LLC Resonant Converter With Wide Output Voltage," in IEEE Access, vol. 5, pp. 26653-26665, 2017, doi: 10.1109/AC-CESS.2017.2757764.
- [18] H. Wang and Z. Li, "A PWM LLC Type Resonant Converter Adapted to Wide Output Range in PEV Charging Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3791-3801, May 2018, doi: 10.1109/TPEL.2017.2713815.
- [19] S. A. Hohenberger, J. Spöttle and K. Fichter, "The Charging Behavior of Electric Vehicle Users," Energies, vol. 13, no. 7, p. 1632, 2020.
- [20] C. Nelder and M. Tal, "Plugging in: A stakeholder investment guide for public electric-vehicle charging infrastructure," Rocky Mountain Institute, 2017.
- [21] A. Lordoglu, M. O. Gulbahce, D. Ahmet Kocabas and S. Dusmez, "Extended Describing Function Modeling and Closed-Loop Control of LLC Converter in Battery Charging Applications," 2021 International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) & 2021 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM), 2021, pp. 274-279, doi: 10.1109/OPTIM-ACEMP50812.2021.9590032.
- [22] J. Zhang, W. G. Hurley and W. H. Wölfle, "Gapped Transformer Design Methodology and Implementation for LLC Resonant Converters," in IEEE Transactions on Industry Applications, vol. 52, no. 1, pp. 342-350, Jan.-Feb. 2016, doi: 10.1109/TIA.2015.2465932.
- [23] McLyman, C. W. T. (2004). Transformer and inductor design handbook. CRC press.
- [24] Hurley, William G., and Werner H. Wölfle. Transformers and inductors for power electronics: theory, design and applications. John Wiley & Sons, 2013.
- [25] A. Lordoglu, M. O. Gulbahce, D. A. Kocabas and S. Dusmez, "A New Optimization Method for Gapped and Distributed Core Magnetics in LLC Converter," in IEEE Access, vol. 11, pp. 14061-14072, 2023, doi: 10.1109/ACCESS.2023.3242869.
- [26] M.M. Yovanovich, Y.S. Muzychka and J.R. Culham, "Spreading Resistance of Isoflux Rectangles and Strips on Compound Flux Channels," AIAA 98-0873, presented at the AIAA 36th Aerospace Sciences Meeting and Exhibit, Reno, NV, January 12 - 15, 1998.

- [27] Burkart, Ralph M. Advanced modeling and multi-objective optimization of power electronic converter systems. Diss. ETH Zurich, 2016.
- [28] P.R. Shea and M.M. Jovanovic, "Printed-circuit-board layout technique for improved switching regulator performance," IEEE Transactions on Power Electronics, vol. 24, no. 9, pp. 2097-2106, Sept. 2009.
- [29] Steval-DPSLLCK1. STMicroelectronics. (n.d.). Accessed: Dec. 28, 2022. [Online]. Available: https://www.st.com/en/evaluationtools/stevaldpsllck1.html
- [30] AG,IT.(n.d.). Eval3kw2llcc720.Infineon Technologies. Accessed: Dec. 30, 2022. [Online]. Available: https://www.infineon.com/cms/en/product/evaluationboards/eval3kw2llcc720.html



Serkan Dusmez (S'11–M'16- SM'21) received the B.S. (Hons.) and M.S. degrees in electrical engineering from Yildiz Technical University, Istanbul, Turkey, in 2009 and 2011, respectively. He received the M.S. degree from Illinois Institute of Technology, Chicago, IL, USA, in 2013, and the Ph.D. degree from the University of Texas at Dallas, Richardson, TX, USA, in 2016, both in electrical engineering. From 2016-2019, he has worked as a Systems Engineer in the Texas Instruments, Dallas, TX, USA. In between 2019-2022, he was with the

Arcelik Global R&D serving as the Technical Leader. Since 2022, he has been serving a role of Technical Leader at the WAT Motor A.S.

Dr. Dusmez is the coauthor of more than 75 journal and conference papers and 7 US patents. He is the recipient of Marie Skłodowska-Curie Individual Fellowship awarded by the European Commision in 2021, and International Fellowship for Outstanding Researchers by the Scientific and Technological Research Council of Turkey in 2019. Dr. Dusmez received the 2018-2019 IAS Second Prize Paper and 2017-2018 First Prize Paper both from the IEEE Industry Applications Society, the Jimmy Lin Award for Innovation from the University of Maryland at College Park in 2017, the First Prize Paper Award in the IEEE IAS Annual Meeting from the Industry Applications Society in 2016, the 2015 Best Vehicular Electronics Paper Award from the IEEE Vehicular Technology Society, the David Daniel Doctoral Dissertation Award in 2016 and several other awards from the University of Texas at Dallas. His research interests include high power density solutions with GaN power stage and real-time fault diagnosis of power converters.



Abdulsamed Lordoglu Abdulsamed Lordoglu received the B.S. degree in electrical engineering from Yildiz Technical University, Istanbul, Turkey, in 2016. He received the M.Sc. degree in 2019 in Electrical Engineering Programme, Institute of Science and Technology, ITU and since 2019 he has been a Ph.D. student in the same program. He was a research assistant in the Department of Electrical Engineering, Electric and Electronic Faculty, YTU between 2017 and 2021. He is currently lecturer at Energy Institute, Istanbul Technical University. His

main research interests include high power density solutions for DC/DC resonant converters and the design and optimization of resonant converters for electric vehicles, electrical machines and power converters, harmonics and acoustic noise in electrical machines.



Mehmet Onur Gulbahce Mehmet Onur Gulbahce received the B.Sc. degree in electrical and electronics engineering from Istanbul University, Istanbul, Turkey, in 2010, the M.Sc. degree in electrical engineering from Istanbul Technical University (ITU), Istanbul, Turkey, in 2013, and the Ph.D. degree in electrical drives from the Istanbul Technical University (ITU), Istanbul, Turkey, in 2019. During his Ph.D., he was a visiting researcher with Power Electronic Systems Laboratory, ETH Zurich. Between 2019 and 2021, he was an Assistant Professor at

Department of Electrical and Electronics Engineering, Fatih Sultan Mehmet Vakif University (FSMVU). He is currently Assistant Professor at Department of Electrical Engineering, Istanbul Technical University (ITU), Istanbul, Turkey. His research interests include novel high-speed electrical machine topologies, harmonics in electrical machines and wide-bandgap power devices for very efficient and compact electrical drive systems and power converters.



Derya Ahmet Kocabas received the B.S. degree in electrical engineering from ITU, Istanbul, Turkey, in 1994. He received the M.Sc. and Ph.D. degrees from Electrical Engineering Programme, Institute of Science and Technology, ITU, in 1997 and 2004, respectively. His main subjects of concern are design and control of electrical machines, space harmonics, drive systems and power electronics. He joined to Department of Electrical Engineering, Electroics and Electronics Faculty, ITU in 1995 and since January 2009 he has been an Assistant Professor.