Microwave Bytes

Conservatively Speaking

■ **John Wood**

Are there any new ideas under the sun? We are all aware of those ideas that reappear, sometimes after several decades, as new and effective solutions to current problems. A good example of this is the Doherty power amplifier (DPA), which was first invented and reported by W.H. Doherty [1] in 1935 for the efficient amplification of amplitude-modulated (AM) radio-frequency (RF) signals. The original idea used vacuum tubes for the active devices. The DPA was rediscovered in the 1990s as an efficient and effective means of amplifying cellular wireless signals; this new implementation used LDMOS transistors. Nowadays, the DPA is virtually ubiquitous in cellular base stations.

There are also those ideas that are not so good, and one wonders why they keep resurfacing periodically. One of these ideas is to use nonlinear capacitors, controlled by two independent voltages, as the reactive components in large-signal field-effect transistor (FET) models. While this approach does, on the face of it, seem quite reasonable, as it looks like an extension of the small-signal FET model by making the junction capacitances voltage dependent (Figure 1), it is not really such a good idea in practice. We shall pursue why this is the case in this article.

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Digital Object Identifier 10.1109/MMM.2014.2355634
Date of publication: 12 November 2014

A Brief Review of the Historical Development of Large-Signal FET Models

The first compact models for FETs to appear in a circuit simulator were the SPICE junction FET and MOSFET models [2]. These circuit models were based on the physics of the transport of electrons along the channel in long gate-length devices. While these models were adequate for the low-speed silicon technology of the time, with the advent of new transistor technologies, such as the GaAs metal–semiconductor FET (MESFET), which boasted a gate length of the order 1 μm and a transition frequency over 10 GHz, coupled with new microwave measurement techniques such as S-parameters, there was a renewed interest in the development of FET compact models. The well-known examples of compact models of this era are the "Curtice" [3] and "Statz" or "Raytheon" [4] models for GaAs IC FETs, the "Curtice-cubic" [5] model for FETs used in power amplifiers, and more general-purpose models such as the "Parker–Skellern" [6] and "TriQuint's Own Model" [7].

IMAGE LICENSED BY GRAPHIC STOCK

Many of these compact models for GaAs MESFETs were extensions of the small-signal equivalent circuit model, based on the intuitive association of the circuit elements with the physical structure of the transistor. They describe the large-signal behavior by curve fitting the dc $I_d - V_{ds}$ characteristics and the terminal capacitance–voltage relationships of the transistor. And this is, in general, much the same approach as is practiced today for many FET models, including those models that have been developed or adapted from the previously mentioned list for newer technologies, such as the HEMT and PHEMT in III–V semiconductors, and models developed for LDMOS power FETs [8]–[10].

The drain current characteristics are often fitted with a hyperbolic tangent curve. This is essentially a behavioral

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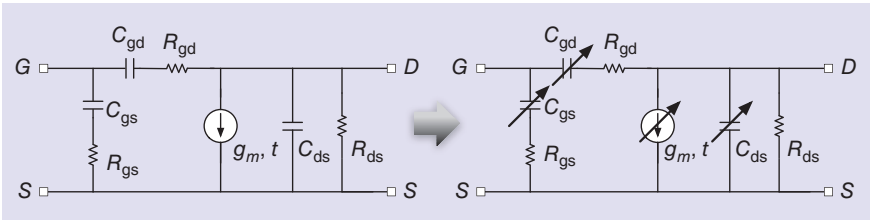

Figure 1. *Extending a small-signal FET model to large signal by the simple act of making the nonlinear components voltage dependent. While the gate-drain capacitance may often be shown as a function of the voltage across it, V_{gd}, the control variables in the model are the gate-source and gate-drain voltages, and, thus, V_{gd} is a derived variable.*

model, using parameters that shape the function to the I–V curves. The input capacitances C_{gs} and C_{gd} can vary with bias and have a significant impact on the FET behavior. Early large-signal MESFET models incorporated a voltage dependence for these capacitances based on the classic p-n junction or Schottky barrier capacitance–voltage relationship

$$C(V_{\text{applied}}) = \frac{C_0}{\sqrt{\phi_{\text{bi}} - V_{\text{applied}}}}, \qquad (1)$$

where C_0 is the zero-bias capacitance and ϕ_{bi} is the built-in voltage of the junction; the applied voltage is the gate-to-source or gate-to-drain voltage across the appropriate capacitor.

An inspection of the capacitance–voltage relationships for the small-signal capacitances C_{gs} and C_{gd} indicates that the form of the relationship is very different from our expectations based on the classical equation predictions given here. Examples of C_{gs} and C_{gd} plotted against V_{ds}, with V_{gs} as parameter, for a GaAs PHEMT power transistor, are shown in Figure 2(a) and (b), respectively, to illustrate this effect.

We can observe from Figure 2 that in the current saturation region, beyond the knee of the curves, the value of the capacitance C_{gd} is larger when the channel is pinched off, that is, when V_{gs} is below the threshold, than when the channel is open. This is exactly counter-intuitive to our expectations from a one-dimensional analysis of the charge in the gate-drain depletion region. It is clear from the curves in Figure 2(a) and (b) that the model capacitances are not simple one-dimensional capacitances but are the functions of both V_{gs} and V_{ds}.

At this point, a simple development of a large-signal model from the small-signal parameters suggests itself

$$C_{gs} = \frac{1}{\omega}\text{Im}(y_{11} + y_{12}) = C_{11} + C_{12}$$
$$C_{gd} = -\frac{1}{\omega}\text{Im}(y_{12}) = -C_{12}. \qquad (2)$$

The capacitances C_{ij} are now dependent on the instantaneous values of the voltages V_{gs} and V_{ds}. We can then write, for the (reactive) current at the gate

$$I_1 = C_{gs}(V_{gs}, V_{ds})\frac{dV_{gs}}{dt} + C_{gd}(V_{gs}, V_{ds})\frac{dV_{gd}}{dt}. \qquad (3)$$

At first glance, this equation looks like a satisfactory description for the reactive port current. But implementing this expression in a compact model leads to several problems.

A circuit capacitor is a two-terminal device that carries a charge whose value is controlled by the voltage across its terminals. Here, the capacitances are controlled by two independent voltages. While this description is quite straightforward for the small-signal case, the behavior of a two-terminal capacitor, whose value depends on the two signal voltages V_{gs} and V_{ds}, requires a more careful definition under large-signal conditions. Even though (3) can be implemented algebraically in some

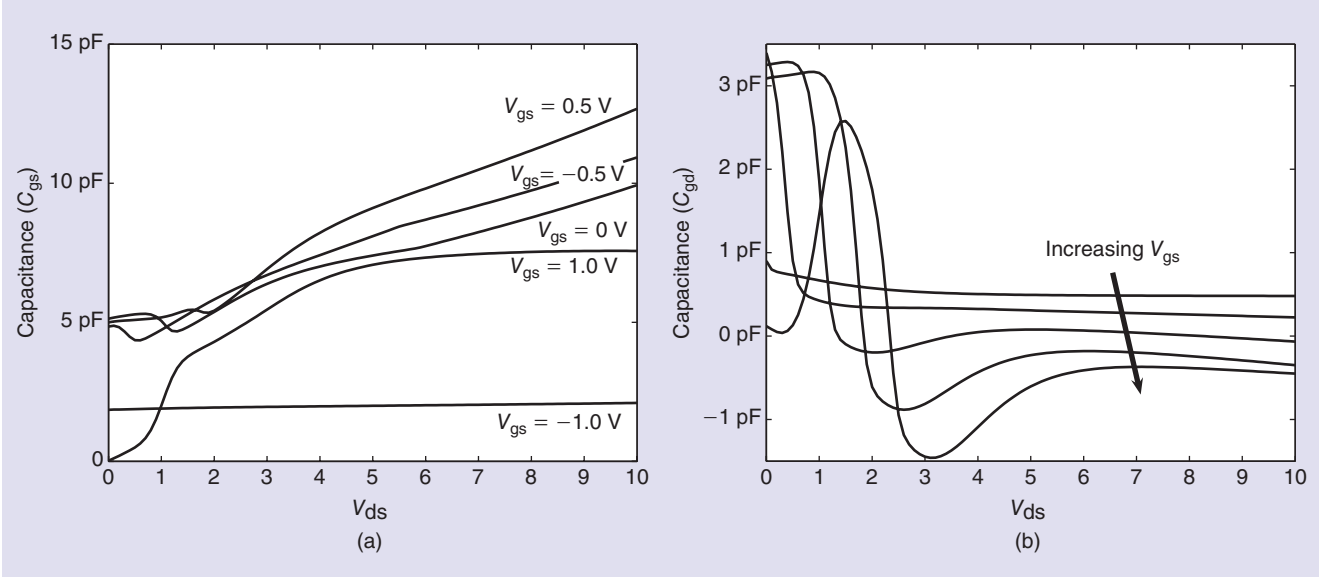

Figure 2. *The gate-source and gate-drain small-signal capacitances for a GaAs power PHEMT shown as functions of the applied bias voltages: (a) C_{gs} of the GaAs PHEMT and (b) C_{gd} of the GaAs PHEMT. From [11], © 2007 Cambridge University Press. Reprinted with permission.*

circuit simulators, Root and Hughes [12] noted that such a component can accumulate a net charge under steady-state periodic signal conditions, even though the voltage across the capacitor's two terminals returns to the same value at the end of the period. This is a violation of the concepts of conservation of charge and conservation of energy.

In a simple "thought experiment," Snider [13] illustrates just how the principles of conservation of charge and energy are violated with such a nonlinear capacitor. In Figure 3, we have a nonlinear two-terminal capacitor, whose value is governed by the remote voltage V_2, placed across the input voltage source V_1. The capacitor's value is (following Snider)

$$C(V_1, V_2) = 3 - V_2. \tag{4}$$

Let us analyze this circuit over a single cycle in which the voltage V_1 steps from 1 to 2 V, then voltage V_2 steps from 1 to 2 V; then, V_1 returns to 1 V, and finally, V_2 returns to 1 V; now, both voltages are back in their original conditions.

Initially, with $V_2 = 1$ V, the capacitance is 2 farads; and $V_1 = 1$ V, hence the charge on the capacitor is $Q = 2$ coulombs. As the voltage V_1 is stepped to 2 V, the capacitor remains fixed at 2 farads, and 2 coulombs of charge is delivered from the source V_1. Integrating the charge through the voltage source shows that 3 joules of energy has been supplied from the source V_1.

Source V_1 is now held at 2 V, while source V_2 is stepped from 1 to 2 V. Since the source V_2 is not connected physically to the capacitor, then, by conventional circuit theory (as is generally used in the better circuit simulators), the charge on the capacitor must remain fixed because V_1 has not changed, but the value of the capacitance drops to 1 F by (4). We begin to feel that something is starting to go wrong here. Nevertheless, we will press on.

The source V_1 now steps back to its initial value of 1 V. The capacitance is fixed at 1 F during this transition, and, hence, the change in charge on the capacitor is −1 coulomb and −1.5 joules of energy is returned to the source V_1. Finally, V_2 steps back from 2 to 1 V, the initial condition. Again, the change in charge and energy are zero by conventional circuit theory—V_1 is unchanged—but the capacitance value returns to 2 farads.

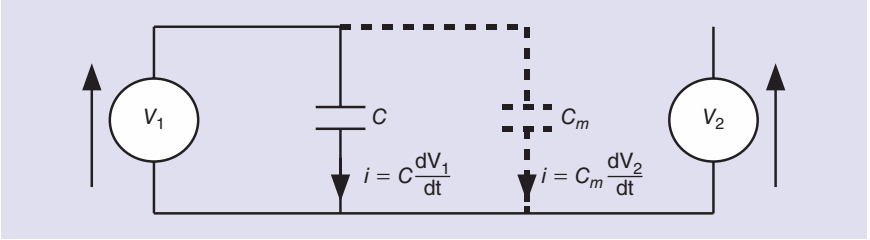

Figure 3. *A simple schematic circuit of a nonlinear capacitor whose value is a function of V_1 and a remote voltage V_2 [13].*

At the end of this cycle, we have gained a net charge of 1 coulomb on the capacitor and dissipated 1.5 joules of energy, even though this is a lossless circuit. We have apparently broken the laws of conservation of charge and energy, and yet, this is how a conventional simulator would treat a circuit containing nonlinear capacitors whose values are dependent on remote voltages.

A means of accounting for this "extra" charge and energy in the electrical domain is to introduce a transcapacitance. We add another capacitance, C_m, into the circuit in parallel with C in Figure 3, and in which the reactive current is determined by

$$I = C_m \frac{dV_2}{dt}. \tag{5}$$

The value of the transcapacitance and the functional dependence on the voltages (V_1 and V_2) are related to the value of the capacitor, C, through

$$\frac{\partial C}{\partial V_2} = \frac{\partial C_m}{\partial V_1} = -1 \tag{6}$$

in this example. If we now let $C_m = -V_1$, as V_2 is stepped from 1 to 2 V while V_1 is held at 2 V in the voltage cycle, then a charge of $C_m \cdot \Delta V_2 = -2$ coulombs is transferred from the source V_1. This is exactly equal to and opposite of the charge transferred from source V_1 in the first voltage transition. If we follow the voltage steps through the complete cycle, we find that the net transfer of charge from source V_1 is zero and the net energy dissipated in the system is zero. We now have a conservative system. The condition described by (6) is called the integrability condition and constrains the possible values of the pair of capacitances C and C_m to ensure charge conservation.

In addition to the problems of implementing a capacitor controlled by two independent voltages, it can be shown that these incorrect descriptions for the model capacitances will lead to inaccuracies in the representation of the large-signal phase response of the transistor, known as the AM-to-PM characteristic, and also in the prediction of intermodulation and related distortion products in power amplifier circuits. Staudinger et al. [14] showed that by changing the model description of the gate capacitors only, using first the classical Schottky junction model (1), then the "Statz" [4] symmetrical capacitance model, and finally a fully charge-conservative model, only the charge-conserving capacitance model could accurately predict the measured third-order intermodulation distortion and adjacent channel leakage ratio data for an RF power amplifier.

Clearly, any large-signal FET model that we want to build needs to be current and charge conservative if we want it to be accurate and run successfully in the circuit simulator. What this means is that the state variables of our model need to be current and *charge*, and not current and capacitance. Such a charge-based approach has been presented by Ward and Dutton [15] and Root and Hughes [12] and further developed by Wood et al. [16], Daniels et al. [17], and Jansen et al. [18].

Conservation of Current and Charge

The conservation of current is embodied in Kirchhoff's current law, which states that the net current entering a circuit node is zero. Generally, in compact

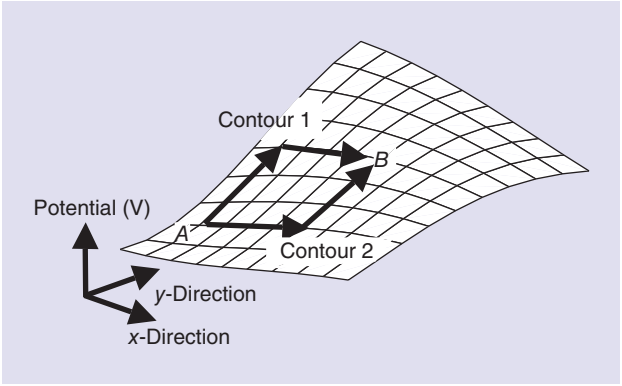

Figure 4. *A two-dimensional electric field in coordinates (x, y). The points A and B represent two potentials in this field, and contour 1 and contour 2 are two different paths connecting A to B. From [11], © 2007 Cambridge University Press. Reprinted with permission.*

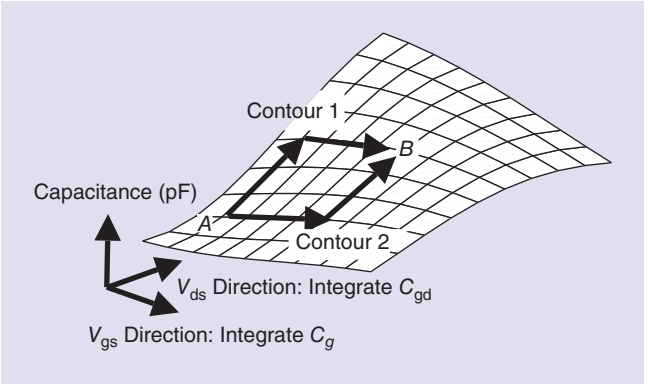

Figure 5. *The two-dimensional capacitance field at the gate, in coordinates (V_{gs}, V_{ds}). The points A and B represent the locations of two instantaneous signal voltages in this field, and contour 1 and contour 2 are two different paths connecting A to B. From [11], © 2007 Cambridge University Press. Reprinted with permission.*

device model construction, we do not need to worry about current conservation, as the simulator takes care of this by solving Kirchhoff's voltage law at each node in the circuit.

The conservation of charge is also something that we tend to take for granted: charge can be neither created nor destroyed, although we have seen that it is all too easy to create nonchargeconserving elements in a circuit simulator. Here, we shall look at how to create a charge-conserving element that we can use in a large-signal model.

Taking the large-signal gate charge Q_g as an example, the concept of charge conservation is described in the form of a conservative field of capacitance. A more familiar example of a conservative field is the electric field. A two-dimensional electric field in x and y is shown in Figure 4; given two arbitrary locations A and B in this field, we know that if we integrate along any path from A to B, we obtain the same potential difference between these points

$$\int_{A,\,\text{contour1}}^{B} \vec{E}\cdot\vec{dl} = \int_{A,\,\text{contour2}}^{B} \vec{E}\cdot\vec{dl} = V_{BA}. \quad (7)$$

A conservative field is also an *irrotational* field: the *curl* of the field vector is zero. For the two-dimensional electric field in our example, the *curl* is written as

$$\text{curl}(\vec{E}) = \frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y} = 0. \quad (8)$$

We can see that this relation has exactly the same form as (6), provided we replace the electric field by a capacitance field, C, and the $x-y$ coordinates become vectors in the directions of V_{gs} and V_{ds}:

$$\vec{C} = C_g(V_{gs}, V_{ds})\vec{u}_{Vgs} + C_{gd}(V_{gs}, V_{ds})\vec{u}_{Vds} \quad (9)$$

$$\vec{V} = V_{gs}\vec{u}_{Vgs} + V_{ds}\vec{u}_{Vds}, \quad (10)$$

where

$$C_g(V_{gs}, V_{ds}) = C_{gs}(V_{gs}, V_{ds}) + C_{gd}(V_{gs}, V_{ds}) \quad (11)$$

is the C_{11} element.

In other words, we have a conservative capacitance field, and we can integrate along any contour between two points in this field to obtain the difference in charge between the two points. Integration around any closed contour in the field brings us back to the starting point, and no charge has been lost or accumulated: charge is conserved. The two-dimensional capacitance field for the gate charge Q_g is shown in Figure 5.

We now have a way of determining the gate charge state variable Q_g from the bias-dependent measured values of C_{gs} and C_{gd}. Starting from some arbitrary bias point in the $\{C_g, C_{gd}\}$ field, we can carry out a line integral in the voltage space to any other bias point to determine the change in gate charge. By doing this over the whole measurement space of the bias-dependent gate capacitances, we build the gate charge state function of the instantaneous voltages V_{gs} and V_{ds}. This is how the Root FET model charge state variables are constructed.

The choice of values for C_{gs} and C_{gd} is not arbitrary; we cannot simply partition the gate capacitance between C_{gs} and C_{gd} in any way we choose. For charge conservation to hold, the values of C_{gs} and C_{gd} are related through the *curl* of the capacitances—the integrability condition. In fact, it is only when this condition is met that the model is able to fit the measured bias dependence of the Y-parameters.

A Charge-Conservative Model

A simple large-signal FET model structure begins to suggest itself. This is shown in Figure 6, which comprises voltage-controlled current and charge sources at the gate and drain ports. The currents and charges are the state variables, and they are instantaneous functions of the controlling gate- and drain-source voltages (V_{gs} and V_{ds}).

The expressions for the instantaneous values of the charges and currents can be found from integrating the conductance and capacitance fields obtained from the Y-parameters over the gate- and drain-source voltages, as shown in Figure 5, and described in detail in [11] and [19]. Other methods of generating the state functions from the measured Y-parameter data can also be applied. These range from a simple two-dimensional integration of the conservative fields, in Mathworks MATLAB, for

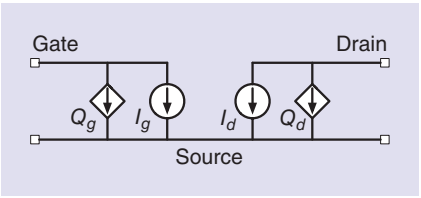

Figure 6. *The schematic circuit for the large-signal model, showing the voltage-controlled gate charge and gate-source current sources, and the voltage-controlled drain charge and drain-source current sources.*

instance, to yield the two-dimensional I and Q functions, to using nonlinear function approximation using artificial neural networks to perform the integration using adjoint techniques [20].

This is essentially a quasi-static approach, assuming that the steady-state small-signal behavior is representative of the large-signal behavior. Often, this is sufficient, but, for devices where the dynamic nonlinear behavior plays an important role, generating the state functions directly from large-signal measurements of the device Y-parameters can be carried out [21], [22].

Conservation of Energy

The conservation of energy is another basic physical principle that cannot be violated, except by accident or design in simulation. The relationship between charge and energy is of the general form

$$U = \int Q(V) \cdot dV. \tag{12}$$

Following our earlier arguments, and the thought experiment, we would expect that the energy is conserved in our charge model of the FET, and this condition places similar constraints upon the two charges, Q_g and Q_d, as these charges place upon the capacitances attached to the gate and drain nodes. This constraint is expressed as an integrability relation for the energy, analogous to the one for the charge. This is written as

$$\frac{\partial Q_g(V_{gs}, V_{ds})}{\partial V_{ds}} = \frac{\partial Q_d(V_{gs}, V_{ds})}{\partial V_{gs}}. \tag{13}$$

This equation states that there is a single energy function $U(V_{gs}, V_{ds})$ that is conserved by the gate and drain charges. The matrix of second partial derivatives of this function U, with respect to the terminal voltages, is related to the measured capacitance functions, through

$$\begin{bmatrix} \frac{\partial^2 U}{\partial V_{gs}^2} & \frac{\partial^2 U}{\partial V_{gs}\partial V_{ds}} \\ \frac{\partial^2 U}{\partial V_{gs}\partial V_{ds}} & \frac{\partial^2 U}{\partial V_{ds}^2} \end{bmatrix} = \begin{bmatrix} C_{gs}+C_{gd} & -C_{gd} \\ -C_{gd} & C_{ds}+C_{gd} \end{bmatrix}. \tag{14}$$

One consequence of using a conservative energy function U is that the capacitance matrix must be symmetrical: there can be no transcapacitance. But a zero transcapacitance is inconsistent with the measured bias-dependent Y-parameter data, from which we have constructed our charge model

$$\begin{bmatrix} C_{gs}+C_{gd} & -C_{gd} \\ C_m - C_{gd} & C_{ds}+C_{gd} \end{bmatrix} = \begin{bmatrix} \frac{\partial Q_g}{\partial V_{gs}} & \frac{\partial Q_g}{\partial V_{ds}} \\ \frac{\partial Q_d}{\partial V_{gs}} & \frac{\partial Q_d}{\partial V_{ds}} \end{bmatrix}. \tag{15}$$

An energy-conserving model based on a single energy function U will not be able to predict the measured bias-dependent capacitances from which it was derived. An energy-conserving model will also be charge conserving, but not necessarily vice versa, as the charge-conserving model will require a transcapacitance. Nevertheless, the benefits of implementing an energy- or charge-conserving model, with the associated constraints enforced by the integrability conditions, are that the model will perform in large-signal simulation without the nonphysical consequences such as unbounded charge growth.

Concluding Remarks

We have seen that it is all too easy to break the fundamental laws of physics when constructing a circuit model of the FET if you don't think about how the elements of the model behave in practice in a circuit simulator. What is surprising, though, is why so many models are created that don't subscribe to the laws of conservation of charge, in particular, when we have seen that it is not that difficult to build a model that is correctly charge conservative. The ramifications of building an incorrect model are easy to see: the simulation will converge to the wrong answer, if indeed it converges at all.

While the error may have been small enough to discount as measurement or modeling error when dealing with simple, fairly linear Class A PAs, now that we are designing and developing amplifiers that operate in the nonlinear regime, and that may include switching and other fast transient behaviors, in DPAs and envelope tracking PAs, for example, the proper modeling of the charge in the device is crucial to the successful design. Since a charge-conservative model is fairly straightforward to construct, why would anyone want to build a model that is incorrect?

Acknowledgment

I would like to thank Cambridge University Press for allowing me to quote extensively from [11, Ch. 6].

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IEEE Region 6 Award for 2014 Corporate Support to Maury Microwave

On 26 June 2014, the IEEE Region 6 Southern Area Award for Outstanding Corporate Service to the Engineering Community for 2014 was presented to Maury Microwave. The award was presented at the Maury Microwave facility in Ontario, Canada, to Greg Maury, chief executive officer, and the members of his senior engineering and management staff. The IEEE Foothill Section presenters were Max Cherubin, IEEE Foothill Section MTT/APS Chapter chair, and Frank G. Freyne, IEEE Foothill Section chair.

Maury Microwave staff accept the IEEE Region 6 Southern Area Award for Outstanding Corporate Service.

This IEEE award acknowledged the continuing efforts by Maury Microwave "…in providing hands-on exposure to microwave calibration theory and techniques, thereby enhancing the RF and microwave knowledge base in the IEEE Foothill Section and greater Los Angeles area." The IEEE especially acknowledged the technical presentations and numerous student group tours conducted at the Maury Microwave facility over the past two years. These tours have attracted upper-division IEEE students from a number of local colleges and universities, including Cal Poly Pomona, the University of California Riverside, Harvey Mudd College, California Baptist University of Riverside, Devry Pomona, and Mt. San Antonio College. The contributions of the senior engineering staff and support team at Maury Microwave, including Rusty Myers and Sathya Padmanabhan, were explicitly noted during the award presentation.

Digital Object Identifier 10.1109/MMM.2014.2356091
Date of publication: 12 November 2014

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