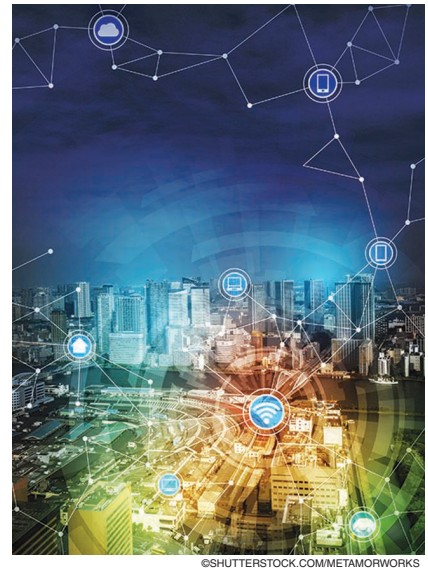
From the Guest Editor's Desk

Enabling Technologies for Efficient 100-Gb/s Wireless Communication Systems

■ **Christian Carlowitz and Noriaki Kaneda**

Recently, major advances in analog front ends for ultrahigh-speed wireless communication systems targeting data rates toward 100 Gb/s have been demonstrated at high carrier frequencies between 100 and 300 GHz. To deliver such performance in a complete system to the end user, various functionalities, such as analog-to-digital converters (ADCs) and high-speed digital signal processors, need to be integrated as well as very high-bandwidth baseband components. Upscaling these components in conjunction with the classic homodyne transceiver front end still comes with major challenges to be addressed, most notably high relative and absolute bandwidth, high frequencies at technological limits as well as low efficiency in terms of power consumption, and system size. Consequently, it is attractive to reconsider central decisions in system architecture to achieve ultrahigh data rates with an efficient implementation. This affects, most notably, the tradeoff between low carrier frequencies with narrow available bandwidth and extremely high spectral efficiency and high frequencies with extremely wide available bandwidth and low spectral efficiency.



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In this focus issue, we review current approaches toward 100 Gb/s wireless communication front-end architecture implementations, with a focus on efficiency, integrated circuit integration, and remaining challenges for implementation in practice. The issue originates from the 2021 IEEE Microwave Theory and Technology Society (MTT-S) International Microwave Symposium workshop "Enabling Technologies for Efficient Ultrahigh Speed Wireless Communication Systems Toward 100 Gb/s," organized by this issue's guest editors, where the topics mentioned in the preceding were addressed and intensively discussed during the panel at the end.

The workshop was initiated by MTT-S Technical Committee (TC) 15 (RF/Mixed-Signal Integrated Circuits and Signal Processing), which focuses on high-speed analog and digital signal processing as well as mixed-signal approaches. From a signal processing standpoint, transceiver architecture design offers a wide range of interesting concepts for efficiency enhancement, especially when going beyond classic approaches, such as the heterodyne or homodyne (zero intermediate frequency) transceiver. Therefore, we also consider polar and outphasing modulators, different carrier frequency ranges, and modulation/demodulation techniques that employ

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Digital Object Identifier 10.1109/MMM.2023.3277352
Date of current version: 13 July 2023

digital approaches and/or shift the boundary between the analog and digital domains.

This focus issue's first article, by Christian Carlowitz and Marco Dietz [A1], picks up the workshop's contents and discussion results as a starting point and presents a comprehensive review of integrated front-end implementations targeting wireless 100 Gb/s and beyond. Starting with a general discussion on transceiver architecture and an overview of available semiconductor technologies, current implementations and their major design choices are discussed for 60-GHz, terahertz CMOS, silicon–germanium terahertz, III-IV-based terahertz, and, briefly, photonics-based transceivers. Afterward, significant remaining challenges for integration and real-world applications are summarized.

It is attractive to reconsider central decisions in system architecture to achieve ultrahigh data rates with an efficient implementation.

The second article, by Zhongxia Simon He, Sining An, and Herbert Zirath [A2], specifically addresses real-time modulation and demodulation techniques. It addresses the remaining challenge of ADC and digital-to-analog converter integration with front ends, which may significantly increase power consumption and complexity. Thus, alternative transmitter and receiver approaches are discussed, which reduce the requirements for analog baseband signal conversion. Among others, outphasing transmitters, pilotless real-time demodulation, and efficient pilot-based receivers are discussed.

While this issue focuses more on electronic integrated transceiver front ends and architectures, there are additional existing reviews with a different scope for further reading. An overview of more photonics-oriented techniques is provided, e.g., in [1], and more in-depth coverage, especially of energy-efficient modulation formats and their impact on transceiver architecture, is given in [2].

Finally, we would like to thank *IEEE Microwave Magazine*'s editorial board for the encouragement in planning this issue. Also, we greatly appreciate the support of our colleagues on the MTT-S RF/Mixed-Signal Integrated Circuits and Signal Processing Committee (TC-15) in pushing forward this issue. Finally, thanks to the authors of this issue's articles for their hard work and excellent job in communicating analog, digital, and mixed-signal processing methods to the microwave theory and technology community for enhancing high-speed communication systems.

References

[1] L. Zhang, X. Pang, S. Jia, S. Wang, and X. Yu, "Beyond 100 Gb/s optoelectronic terahertz communications: Key technologies and directions," *IEEE Commun. Mag.*, vol. 58, no. 11, pp. 34–40, Nov. 2020, doi: 10.1109/MCOM.001.2000254.

[2] P. Heydari, H. Wang, H. Mohammadnezhad, and P. Nazari, "Energy efficient 100+ GHz transceivers enabling beyond-5G wireless communications," *IEEE Wireless Commun.*, vol. 28, no. 1, pp. 144–151, Feb. 2021, doi: 10.1109/MWC.001.2000213.

Appendix: Related Articles

[A1] C. Carlowitz and M. Dietz, "Integrated front-end approaches for wireless 100 Gb/s and beyond," *IEEE Microw. Mag.*, vol. 24, no. 8, pp. 16–34, Aug. 2023, doi: 10.1109/MMM.2023.3277360.

[A2] Z. S. He, S. An, and H. Zirath, "Modulator and demodulator solutions for real-time communication toward 100 Gb/s," *IEEE Microw. Mag.*, vol. 24, no. 8, pp. 35–49, Aug. 2023, doi: 10.1109/MMM.2023.3277361.