Nitrogen-Doped Czochralski Silicon Wafers as Materials for Conventional and Scaled Insulated Gate Bipolar Transistors

Kaoru Kajiwara, Kazutaka Eriguchi, Kazuhiro Fusegawa, Noritomo Mitsugi, Shuichi Samata, Kazuhisa Torigoe, Kazuhiro Harada, Masataka Hourai, and Shin-ichi Nishizawa, *Member, IEEE*

***Abstract*—Nitrogen-doped silicon wafers manufactured using the Czochralski technique (Cz-Si) with an oxygen concentration ([O_I]) of 2.5–5.6 × 10^{17} atoms cm^{-3} are heat treated to simulate the conventional and scaled manufacturing processes of insulated gate bipolar transistors (IGBTs). Subsequently, the oxygen precipitation, lifetime, and gate oxide integrity (GOI) of the Cz-Si wafers are evaluated. After the high-temperature heat treatment that simulates the conventional process, the lifetime of the Cz-Si with an [O_I] of 5.6 × 10^{17} atoms cm^{-3} only degrades slightly even when oxide precipitates are not detected. In contrast, after the low-temperature heat treatment that simulates the scaled process, oxide precipitates are detected and the lifetime reduces substantially at an [O_I] of 5.6 × 10^{17} atoms cm^{-3}. The Cz-Si with [O_I] values below 3.3 × 10^{17} atoms cm^{-3} are considered suitable materials for IGBTs because no oxide precipitate is formed, and the lifetime is not degraded after high- and low-temperature heat treatments. Upon using GOI evaluation, the nitrogen-doped Cz-Si wafers are found to exhibit a breakdown voltage equal to that of an annealed Cz-Si wafer conventionally used for IGBTs. Therefore, nitrogen-doped Cz-Si wafers with [O_I] below 3.3 × 10^{17} atoms cm^{-3} are potential materials for conventional and scaled IGBTs.**

***Index Terms*—Breakdown voltage, carrier lifetime, Czochralski silicon wafer, insulated gate bipolar transistors, semiconductor materials, silicon.**

I. Introduction

In recent years, power devices that can perform highly efficient power conversion and switching have gained considerable attention with the development of electric vehicles, smart grids, and other energy-saving applications. In particular, the market for insulated gate bipolar transistors (IGBTs) has expanded rapidly owing to their application in hybrid and electric vehicles. Additionally, silicon wafers that are free from voids and oxide precipitates, which can degrade gate-emitter breakdown voltage and bulk lifetime of minority carriers, respectively, are required for manufacturing IGBTs [1], [2], [3]. For IGBTs with relatively low breakdown voltages in the range of 600–1200 V, silicon wafers cut from silicon single crystals with a diameter of 200 mm manufactured using the Czochralski technique (Cz-Si) with an oxygen concentration ([O_I]) below 4.5 × 10^{17} atoms cm^{-3} (JEIDA wafers) are typically used as these wafers are oxide precipitate-free after heat treatments [1]. However, voids are present in the as-grown Cz-Si single crystals owing to the limitation of the crystal growth conditions for low [O_I]. Therefore, voids must be eliminated by annealing in an oxygen atmosphere at a high temperature (approximately above 1100 °C) during the wafer or device preparation processes [1], [4], [5]. Simultaneously, the transition from 200 to 300 mm diameter wafers has begun in Europe to improve productivity [6], [7]. However, the thermal stresses caused by the temperature difference between the center and edge are higher for a 300 mm wafer, increasing dislocation propagation [8]. Therefore, a growth technique for obtaining void-free as-grown Cz-Si single crystals with low [O_I] needs to be developed [9], [10].

Nitrogen-doped Cz-Si single crystals with [O_I] below 3 × 10^{17} atoms cm^{-3} (JEIDA wafers) are potential materials for IGBTs [11], [12], because nitrogen-doping suppresses void formation, thereby achieving a void-free as-grown state. Iida *et al.* compared the gate oxide integrity (GOI) of as-received nitrogen-doped Cz-Si wafers with that of an epitaxial wafer [13]. However, a large quantity of oxygen precipitates may have existed owing to the nitrogen-doping following the IGBT device manufacturing processes. This is because these processes are implemented at a high temperature for a long duration compared with those of a typical complementary metal-oxide-semiconductor process, which enhances the growth of oxide precipitates. These oxide precipitates have been reported to affect the GOI [14]; therefore, confirming their impact on the GOI after heat treatment is necessary. However, the properties of nitrogen-doped Cz-Si wafers after heat treatments have not been clarified so far.

Currently, the structures of an IGBT contains a deep trench gate of approximately 6 μm in depth and a p-base layer,

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Kaoru Kajiwara is with the Technology Division, Crystal Engineering Department, SUMCO Corporation, Saga 8490597, Japan, and also with the Interdisciplinary Graduate School of Engineering, Kyushu University, Fukuoka 8168580, Japan (e-mail: kkajiwa1@sumcosi.com).

Kazutaka Eriguchi, Kazuhiro Fusegawa, Noritomo Mitsugi, Shuichi Samata, Kazuhisa Torigoe, and Masataka Hourai are with Technology Division, Advanced Evaluation and Technology Department, SUMCO Corporation, Saga 8494256, Japan.

Kazuhiro Harada is with Technology Division, Crystal Engineering Department, SUMCO Corporation, Saga 8494256, Japan.

Shin-ichi Nishizawa is with the Research Institute for Applied Mechanics, Kyushu University, Fukuoka 8168580, Japan.

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which is in contact with an n-emitter on the cathode side. Therefore, relatively high temperature and heat treatments over long durations are necessary for manufacturing these device structures. However, there are two technical trends in the IGBT device manufacturing process. First, the device processes are low-temperature processes upon changing the wafer diameter to 300 mm. This is motivated by the increasing stress in the wafer owing to the temperature difference between the center and edge of the wafer, which increases dislocation defects [15]. Second, the heat treatment timescale is short owing to the "scaled IGBTs" technique proposed by Tanaka and Omura [16]. IGBT structures can be scaled down with a special scaling coefficient k, by which the trench gate and p-base layer become shallow by a factor of 1/k, resulting in the shortening of the heat treatment timescales. From the aforementioned technical trends, the IGBT device manufacturing process will possibly be conducted at 1000 °C for approximately 10–20 h for the heaviest load process in the future, which will be discussed in Section II-A.

In this study, to reveal the possibility of using nitrogen-doped Cz-Si wafers as materials for IGBTs, the formation of oxide precipitates, minority carrier lifetime, and GOI after heat treatments are investigated using nitrogen-doped Cz-Si wafers with $[O_I]$ of 2.5–5.6 × 10^{17} atoms cm^{-3}. The Cz-Si wafers are subjected to high and low-temperature heat treatment that simulate the conventional and scaled IGBT device manufacturing processes, respectively.

II. Experimental Section

A. Heat Treatment Conditions

In this section, the heat treatment conditions simulating conventional and scaled IGBT device processes are determined. The heat treatment of the IGBTs with the highest temperature and longest duration forms guard ring structures resulting in a high collector emitter voltage, which is realized by diffusing boron into silicon wafers. Saraya *et al.* attempted to form the conventional guard ring structure by heat treatment at 1100 °C for 1300 min [15]. The guard ring is formed by diffusing boron into silicon wafers according to the following equation for diffusion length L [17]:

$$L = \sqrt{t \cdot D_\infty \exp\left(\frac{-E_a}{k_B T}\right)} \quad (1)$$

where t is the heat treatment duration, and D_∞ and E_a are the apparent value of diffusion coefficient at infinite temperature and activated energy of boron in silicon single crystals, respectively. Additionally, k_B is the Boltzmann coefficient and T is the absolute temperature. The relationship between temperature and timescale of the guard ring process of conventional and k = 3 scaled IGBTs estimated from (1) and [15] are shown in Fig. 1. However, the formation of the guard ring structure of scaled IGBTs has not been optimized. Hence, we estimated the guard ring process from [15], in which the scaling of the depth is 1/k, similar to that of the trench gate, p-base layer, etc. As shown in Fig. 1, more than 200 h of heat treatment is necessary for a conventional structure if the process temperature is decreased to 1000 °C. In contrast, only 24 h of heat treatment is approximately equivalent to that of the conventional process at 1100 °C. The low-temperature scaled guard ring process under the two aforementioned technical trends will possibly be implemented at 1000 °C for 10–20 h in the future. The scaling impact of main cell, gate structure on the process temperature and duration can be considered as well. Therefore, the heat treatments conditions simulating conventional and scaled IGBT device processes are determined to be 1100 °C for 15 h and 1000 °C for 15 h, respectively, in this study. Furthermore, each heat treatment condition is subjected to pre-annealing at 780 °C for 3 h to grow the as-grown oxide precipitate nuclei.

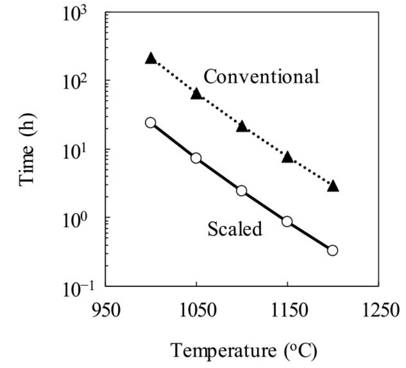

Fig. 1. Forecasted heat treatment temperature and timescale of the guard ring process for conventional and k = 3 scaled IGBTs. Guard ring structures of the scaled IGBTs are assumed to be scaled by 1/k, similar to the scaling of the trench gate, p-base layer, etc.

TABLE I
$[O_I]$ AND NITROGEN CONCENTRATIONS OF THE WAFERS

Condition	$[O_I]$ (JEIDA) $\times 10^{17}$ atoms cm^{-3}	Nitrogen concentration $\times 10^{14}$ atoms cm^{-3}	Voids
High $[O_I]$	5.6	1.4	Absent
Middle $[O_I]$	3.3	1.4	Absent
Low $[O_I]$	2.5	1.6	Absent
Annealed wafer	1.3	Absent	Absent
Void wafer	1.3	Absent	Present

B. Wafers Processing

Five types of silicon wafers (n-type, approximately 250 Ωcm) with a diameter of 200 mm manufactured using Cz-Si single crystals, as shown in Table I, are evaluated. The high, middle, and low $[O_I]$ corresponds to nitrogen-doped Cz-Si wafers with $[O_I]$ of 5.6, 3.3, and 2.5 × 10^{17} atoms cm^{-3}, respectively. The "annealed wafer" in which voids are eliminated by annealing in an oxygen atmosphere is used for IGBTs conventionally. The "void wafer" is not treated with any void annihilation process, such as nitrogen-doping or oxygen annealing, and it includes voids in the central region of the wafer. The various $[O_I]$ values are measured using Fourier transform infrared spectroscopy (ECO-1000S, Thermo Fisher Scientific, Inc.) with a conversion factor of 3.14 × 10^{17} cm^{-2} (JEIDA). Nitrogen is doped in the silicon melt by charging the silicon wafers with a layer prepared using chemical vapor deposition of silicon nitride (Si_3N_4) in a quartz

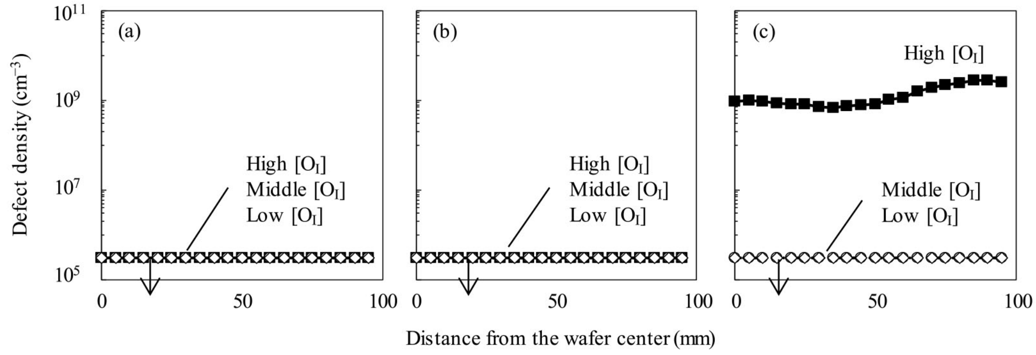

Fig. 2. Defect density distributions along the radial direction of the wafer measured using LST of (a) as-received, (b) Hi and (c) Lo-temp heat treated silicon wafers. The black square, gray circle, and white diamond plots indicate $[O_I]$ values of 5.6, 3.3, 2.5 $\times$ 10^{17} atoms cm^{-3}, respectively.

crucible for the growth of the Cz-Si crystal. The nitrogen concentrations corresponding to various $[O_I]$ is estimated to be 1×10^{14} atoms cm^{-3} by considering a segregation coefficient of 0.0007 between the crystal and silicon melt [18]. The wafers are subjected to high and low-temperature heat treatments in a horizontal quartz tube furnace containing an oxygen (3 %)/nitrogen mixture. The high-temperature condition (Hi-temp) simulating the conventional IGBT process is 780 °C for 3 h followed by 1100 °C for 15 h, whereas the low-temperature condition (Lo-temp) simulating the scaled IGBT (k = 3) process is 780 °C for 3 h followed by 1000 °C for 15 h. The densities of the oxide precipitates are measured by cleaving the wafers along the center using infrared laser scattering tomography (LST) (LST-310A, Semilab Semiconductor Physics Laboratory Co. Ltd). The infrared laser beam was incident on the wafer surface (100) plane, and the light scattered owing to the defects in the <100> direction normal to the cleaved cross-section is observed. The minority carrier lifetime is evaluated by microwave photoconductivity decay (μ-PCD) after chemical passivation using a solution of iodine in ethanol. All the wafers are polished to remove the silicon oxide layer formed during heat treatments before evaluating the minority carrier lifetime. For GOI measurement, 408 planar metal-oxide semiconductors (MOSs) are fabricated per wafer and the time-zero dielectric breakdown in the MOS capacitors is evaluated by measuring the current-voltage characteristics [19]. The Hi and Lo-temp heat treated wafers were re-polished by approximately 2 μm from the wafer surface to remove the silicon-oxide films formed during heat treatment. To confirm the influence of re-polishing on the wafer surface, a wafer with low $[O_I]$ was also re-polished without any heat treatments. After re-polishing, gate oxide films with a thickness of 25 nm were grown on the silicon wafers by annealing in an oxygen atmosphere, and poly silicon electrodes with an area of 10 mm^2 were deposited.

III. Results

Fig. 2 shows the defect density distributions along the radial direction of the wafer measured using LST of the as-received, Hi- and Lo-temp treated silicon wafers. The black square, gray circle, and white diamond plots indicate high, middle, and low $[O_I]$ conditions, respectively. As shown in Fig. 2 (a) and (b), no defects were detected in either of the as-received and Hi-temp treated wafers at any of the $[O_I]$ conditions. In contrast, as shown in Fig. 2 (c), oxide precipitates with a high density of 10^9 cm^{-3} were detected at the high $[O_I]$ values after Lo-temp treatment, although there were no defects at the middle and low $[O_I]$ conditions.

Fig. 3 (a) and (b) illustrate the minority carrier lifetime maps and the average values of these lifetimes over the entire wafers evaluated using the μ-PCD method. The black square, gray circle, and white diamond plots indicate the high, middle, and low $[O_I]$ conditions, respectively. The minority carrier lifetime of the as-received silicon wafer is longer than 5000 μs, which is sufficiently long for an IGBT at all $[O_I]$ values. After the Hi-temp treatment, the middle, and low $[O_I]$ wafers had a long minority carrier lifetime. In contrast, in the high $[O_I]$ condition, the lifetime is 4545 μs, slightly degraded from that of the as-received silicon wafer, despite no defects being detected using LST. After the Lo-temp treatment, the lifetime decreases significantly at the high $[O_I]$ condition because of the presence of oxide precipitates with high densities, as shown in Fig. 1 (c). In contrast, the wafers with middle and low $[O_I]$ maintain a long lifetime equal to that of the as-received silicon wafer.

Fig. 4 shows the distribution maps and fractions of the gate oxide breakdown. The breakdown voltages in the range of 0–1, 1–5, 5–8, and > 8 MV cm^{-2} are labeled as A, B−, B+, and C modes, respectively. The void wafer exhibits a low breakdown voltage with a disk pattern and a C mode fraction of 82.3 %. If the voids are exposed on the wafer surfaces, the gate oxide locally becomes thin, thereby resulting in a lower breakdown voltage than that of a void-free surface. In contrast, the annealed wafer exhibits high GOI quality with the fraction of C mode being 100 %. The nitrogen-doped wafers with $[O_I]$ in the range of 2.5–5.6 $\times$ 10^{17} atoms cm^{-3} exhibit an equivalent GOI quality as that of annealed wafers, the conventional wafers used in IGBTs.

Thick oxide layers are formed on the wafer surfaces during heat treatments, such as at 1000 °C in an oxygen (3 %)/nitrogen mixture. Therefore, such oxide layers should be removed before GOI evaluations corresponding to the Hi- and Lo-temp treatment conditions. In this study, the wafers are re-polished mechanically and chemically after heat treatments to obtain

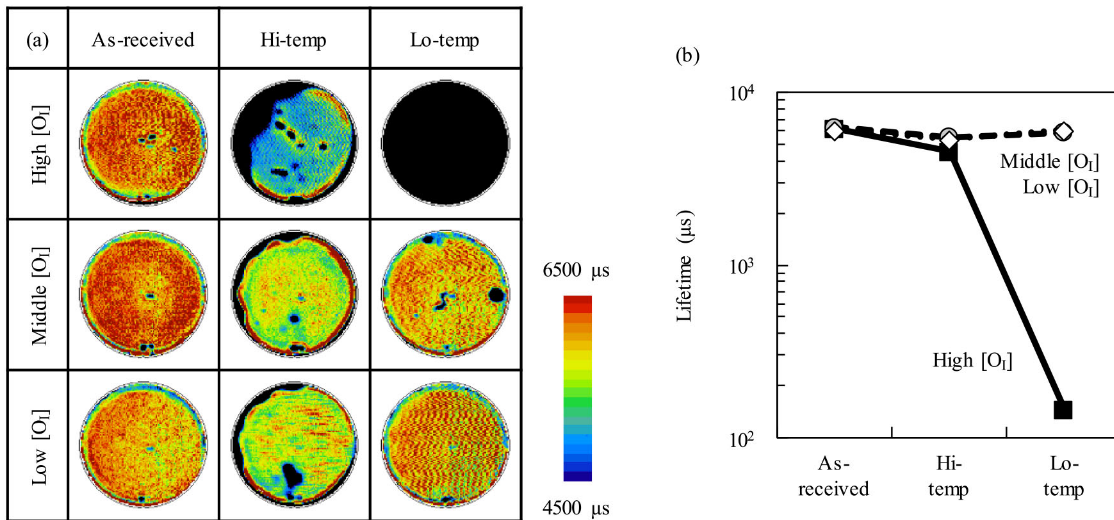

Fig. 3. (a) Minority carrier lifetime maps captured using the μ-PCD method and (b) average value of these lifetimes over the entire wafer. The black square, gray circle, and white diamond plots indicate high, middle and low [O_I], respectively.

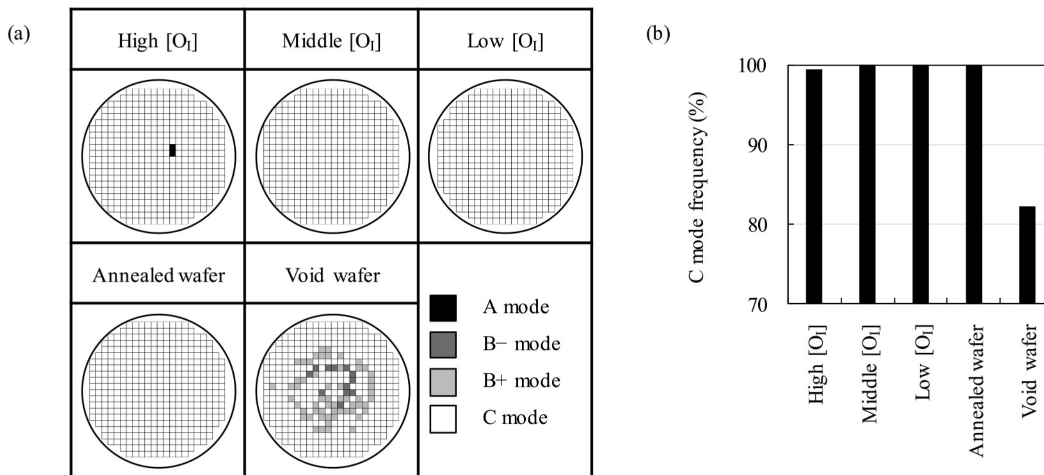

Fig. 4. (a) Distribution maps of for different conditions and (b) fractions of the gate oxide breakdown voltage for the as-received silicon wafers. The breakdown voltages in the range of 0–1, 1–5, 5–8 and $>$ 8 MV cm^{-2} are labeled by A, B$-$, B$+$, and C modes, respectively.

surfaces free from oxide layers. To confirm the quality of the re-polished wafer surfaces, we prepared a reference sample by re-polishing a wafer without any heat treatments using low [O_I] condition, which indicates excellent GOI quality at the as-received condition, as shown in Fig. 4. The distribution maps and fractions of the C mode of the reference sample are shown on the right side of Fig. 5. Unlike the as-received low [O_I] condition shown in Fig. 4, the fraction of C mode after re-polishing decreases by 1 % possibly owing to the particles attached during re-polishing. The left side of Fig. 5 shows the distribution maps and the fractions of the C mode after re-polishing following Hi and Lo-temp treatments. Even though some areas of low breakdown voltage can be seen in the wafer maps, the fractions of the C mode are at similar levels for all conditions including the reference, which has the same quality as that of the conventional wafers used for IGBTs, as shown in Fig. 4. The nitrogen-doped Cz-Si wafers exhibit a GOI quality similar to the as-received silicon wafer after Hi- and Lo-temp treatments.

IV. Discussion

Table II summarizes the [O_I] values required to use nitrogen-doped Cz-Si wafers for conventional and scaled IGBTs from the perspective of oxygen precipitation, minority carrier lifetime, and GOI. For the Hi-temp heat treatment, the minority carrier lifetime reduces slightly at the [O_I] value of 5.6 $\times$ 10^{17} atoms cm^{-3} although no oxide precipitates are detected using LST, as shown in Fig. 2 and Fig. 3. Some oxide precipitates are assumed to exist, the diameter and density of which are too low to be detected using LST. The wafers, whose minority carrier lifetimes degrade after heat treatments, should be avoided because a low lifetime causes an increasing collector-emitter leakage current and on-voltage. Therefore, [O_I] below 3.3 $\times$ 10^{17} atoms cm^{-3} is suitable for conventional IGBTs. The nitrogen-doped Cz-Si wafers exhibit equivalent GOI quality to those of annealed wafers, conventionally used for IGBTs. After the Lo-temp treatments, oxide precipitates with high densities are detected at [O_I] of

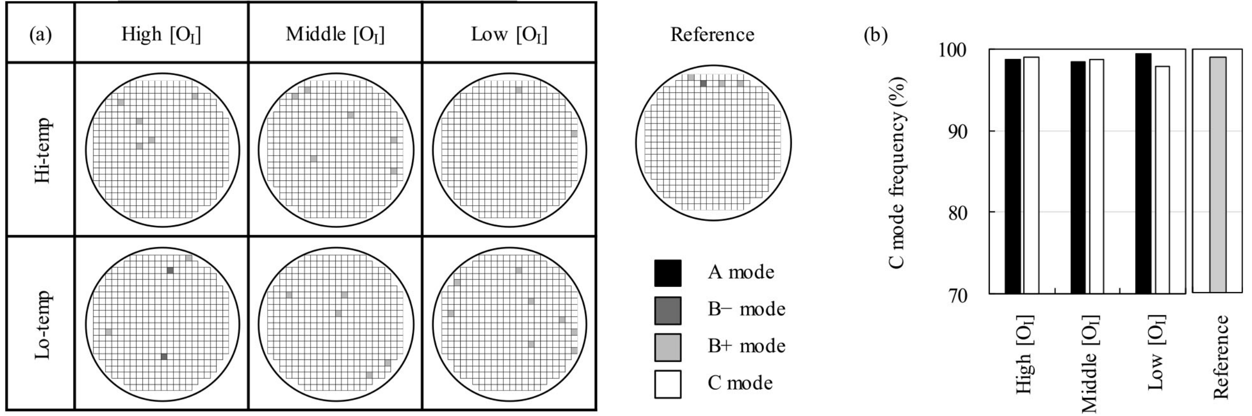

Fig. 5. (a) Distribution maps and (b) fractions of the gate oxide breakdown voltage after Hi and Lo-temp heat treatment. The breakdown voltages in the range of 0–1, 1–5, 5–8 and > 8 MV cm^{-2} are labeled by A, B−, B+ and C modes, respectively. The black and white bars show the C mode frequency after Hi and Lo-temp heat treatment, respectively. The reference is a low $[O_I]$ wafer polished without any heat treatment.

TABLE II
UPPER LIMITS OF $[O_I]$ TO USE NITROGEN-DOPED CZ-SI WAFERS FOR CONVENTIONAL AND SCALED IGBTS

	Criteria	As-received (10^{17} atoms cm^{-3})	Conventional process (10^{17} atoms cm^{-3})	Scaled process (10^{17} atoms cm^{-3})
Oxide precipitates	Not detected	5.6	5.6	3.3
Lifetime	Over 5000 μs	5.6	3.3	3.3
GOI	Equal to that of an annealed wafer	5.6	5.6	5.6

5.6×10^{17} atoms cm^{-3}, thereby substantially reducing the minority carrier lifetime.

The oxygen atoms precipitate onto nuclei that grow as oxide precipitates during heat treatment if the diameters of the nuclei are larger than the critical radius determined by the heat treatment temperature. The critical radius decreases with decreasing temperature because of the increase in the supersaturation of oxygen atoms and therefore, small nuclei remain during Lo-temp treatment. In contrast, the wafers with $[O_I]$ below 3.3×10^{17} atoms cm^{-3} are suitable to be used as the material for scaled IGBTs because oxygen precipitation does not occur and they exhibit long minority carrier lifetimes even after undergoing heat treatment. The breakdown voltage was reported to decrease when the wafer surface has microroughness caused by oxide precipitates [14]. However, the degradation of the breakdown voltage was not observed for any $[O_I]$ value in this study, although oxygen precipitations with high density were detected at an $[O_I]$ of 5.6×10^{17} atoms cm^{-3}. The denuded zone, an oxide precipitate-free region near the wafer surface with a depth of several micrometers, is formed during the thermal process even if a high density of oxide precipitates exists in the bulk. The denuded zone is formed by the out-diffusion of oxygen atoms to the wafer surface from the bulk during heat treatment, thereby resulting in the locally decreasing $[O_I]$ near the wafer surface. In this study, the denuded zone was assumed to be formed by heat treatment, and therefore, the breakdown voltage was equal to that of the as-received silicon wafer. As the wafer surface was passivated using a solution of iodine in ethanol and the surface recombination velocities have high value the minority carrier lifetime exhibits the bulk properties regardless of the formation of the denuded zone. Thus, the silicon wafers with $[O_I]$ of 5.6×10^{17} atoms cm^{-3} have low minority carrier lifetime because of the presence of oxide precipitates.

In conclusion, nitrogen-doped Cz-Si wafers with $[O_I]$ values below 3.3×10^{17} atoms cm^{-3} are suitable as materials for both conventional and scaled IGBTs from the viewpoints of oxygen precipitation, minority carrier lifetime, and GOI.

V. CONCLUSION

Nitrogen-doped Cz-Si wafers are evaluated for their suitability as materials for the conventional and scaled IGBTs, which are assumed to become the standard in the future, from the perspectives of oxygen precipitation, minority carrier lifetime and GOI. For the as-received silicon wafers, no oxide precipitates are observed and thus, the lifetime was long. For the high-temperature heat treatment, which simulated the conventional IGBT device manufacturing processes, no oxide precipitates are detected using LST for $[O_I]$ bellow 5.6×10^{17} atoms cm^{-3}. However, a slight degradation of minority carrier lifetime is observed at an $[O_I]$ of 5.6×10^{17} atoms cm^{-3}. In the case of low-temperature heat treatment, which simulates the scaled IGBT process, oxide precipitates with a high density of 10^9 cm^{-3} are detected, thereby resulting in a substantial reduction in the minority carrier lifetime for an $[O_I]$ of 5.6×10^{17} atoms cm^{-3}. In the wafers with

$[O_I]$ below 3.3×10^{17} atoms cm^{-3}, no oxide precipitates are detected, and the lifetime is maintained at a high value suitable for IGBTs. Using GOI evaluation, the nitrogen-doped Cz-Si wafer was found to possess a breakdown voltage equal to that of an annealed Cz-Si wafer, which is conventionally used for IGBTs. It was thus revealed that the nitrogen-doped Cz-Si wafers with $[O_I]$ below 3.3×10^{17} atoms cm^{-3} can be used for conventional and scaled IGBTs from the viewpoints of oxide precipitates, minority carrier lifetime, and GOI.

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