Guest Editorial
Special Section on the 2020 and 2021 SEMI Advanced Semiconductor Manufacturing Conferences

WE ARE very pleased to introduce this Special Section covering ASMC 2020 and ASMC 2021. These two conferences were held virtually, like most other technical conferences over the last two years; fortunately, the technical community has now reverted to in-person conferences, allowing attendees more personal interaction and the ability to focus on the conference. This includes ASMC 2022 which was held in May of this year, as we hope the COVID-19 pandemic is for the most part behind us.

While conferences are back in-person, the world has profoundly changed. Somehow, when much of normal life stopped for the Covid pandemic, it did not stop or even seem to pause for the tech industry and for many other industries. How did this happen so seamlessly? Due to ongoing innovations in electronics and software, we found that many of our jobs can be done remotely quite effectively. In fact, we've become very aware of the many bonuses of working remotely from home:

- All that daily commute time saved, plus the associated energy cost savings. For those back in the office the roads are less busy.
- The savings in office space for many companies. A more private place to work for those of us used to cubicles.
- The ability to balance work and home life better - to welcome our kids home from school or meet that repair person.
- Some workers have taken the benefits a step further and have relocated to a more cost-effective location, to a more enjoyable location, or to be closer to extended family.

Certainly, some important elements of the traditional workday are missing, like:

- Those impromptu meetings in the hall.
- The exercise walking in from the parking lot and between meetings, which seems trivial, but can actually make a big difference in the course of a day.
- Also, the ambiance of being around your hard-working co-workers to help keep you focused. Many people remember going to the library while in college for an environment boost to get things done.

Fortunately, many companies are embracing this new work and allowing workers the choice of hybrid work policies. With this change, we think all of us IEEE EDS members should give ourselves a pat on the back for enabling this. Without the rapid enhancement in computer power, communications technology, and the corresponding improvements in software over the last 20 years, this virtual or hybrid work age would not have been possible. Consider what you accomplished when you were working from home 20 or even 10 years ago, compared with what's possible for you to achieve today.

With this said, we'll remind you all that one very critical component that enabled these advancements and will continue to do so in the future is the exchange of ideas through conferences such as the SEMI Advanced Semiconductor Manufacturing Conference (ASMC). ASMC brings together semiconductor device manufacturers, equipment and materials suppliers, and academia in a forum to discuss a wide range of important semiconductor manufacturing industry topics including: Yield Enhancement, Advanced Metrology, Defect Inspection, Advanced Equipment and Materials, Factory Automation, Smart Manufacturing, Advanced Process Control, Equipment Optimization, Contamination Free Manufacturing, Advanced Semiconductor Developments, Deep Learning Applications, Materials Integration, and Big Data.

The Advanced Semiconductor Manufacturing Conference, in partnership with the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, annually prepares a Special Section recognizing some of the best papers from the conference. Select authors are invited to submit extended and enhanced versions of their conference papers allowing them to highlight additional progress they have made since the conference. This Special Section includes eight such papers from our two virtual conferences, ASMC 2020 and ASMC 2021, the 31st and 32nd in ASMC's history.

Hong *et al.* [A1] introduce and analyze vehicle-allocation algorithms for overhead hoist transport (OHT) systems in semiconductor fabs. OHT systems are critical to efficient lot delivery and comprise hundreds of vehicles. Limitations of current OHT vehicle allocation algorithms are described, and the performance of multiple algorithms based on the Q learning approach are evaluated and compared to conventional allocation approaches to choose the appropriate algorithms for use in the semiconductor industry.

Flechsig *et al.* [A2] discuss how lot-to-order matching (LTOM) is a crucial process in semiconductor manufacturing, since inefficient allocation and order release have strong adverse effects on wafer fab performance. Their longitudinal case study addressed the issue by summarizing the results of an extensive research project on the automation

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and optimization of the LTOM process for 200 mm and 300 mm wafers at Infineon Technologies Dresden. The project had positive impacts on multiple quantitative and qualitative key performance indicators, e.g., throughput, on-time delivery, tool utilization, cycle and working time savings, collaboration, and employee satisfaction. Congratulations to Christian and co-authors on receiving the SEMI ASMC 2021 Best Student Paper for this work.

Buengener *et al.* [A3] describe application of negative charging for voltage contrast inspection of the 3D NAND word-line contact layer. The authors discovered that negative charging allows a larger voltage to be built up on the word-lines, which they leverage to activate and detect reliability defects.

The benefit of combining metrology techniques, namely X-ray fluorescence and scatterometry is illustrated by Schmidt *et al.* [A4] for the critical case of lateral indentation etching of SiGe nanosheets in Gate-All-Around FET technology. Traditional optical model and Machine Learning performance are compared, taking into consideration the maturity level of the process.

McLaughlin *et al.* [A5] describe an improved method based on Machine Learning to detect color defects after lithography development process. The authors focus on the benefits of image enhancement and optimization by Machine Learning algorithm which, in combination with increase in preventive maintenance and process optimization, enable significant reduction in yield loss.

Reche *et al.* [A6] used synchrotron radiation to perform small angle X-ray scattering (SAXS) on etched line gratings. The authors discovered a method to not only obtain the CD and shape of the etched lines but also the line edge roughness (LER) and line width roughness (LWR) of the lines.

The paper by Alcaire *et al.* [A7] shows that ellipsometry that is usually used as a metrology technique can be used to detect process deviations on a wafer scale. They applied their model-less approach to thickness and CD variations on patterned and unpatterned wafers to determine capabilities and limitations.

Finally, Williams *et al.* [A8] investigated wire bond pad design considerations to develop a robust bond pad design for a power trench FET. The authors completed a detailed analysis using both electrical simulation and physical evaluations of test chips to develop an optimal pad design for the application.

We'd like to recognize Fred Bouchard of SpareTech and Armando Anaya of Northrop Grumman, the conference co-chairs for ASMC 2020, and Alexa Greer of KLA and Ishtiaq Ahsan of IBM, conference co-chairs for ASMC 2021, for their outstanding leadership. We also say good-bye to Margaret Kindling, our SEMI conference coordinator from inception through ASMC 2020, and wish to express our profound thanks for founding ASMC roughly 32 years ago and for being the heart of the conference all these years. Margaret, you are the ultimate positive example in conference stewardship. We welcome Paul Cohen as our new SEMI conference coordinator and congratulate him on a successful ASMC 2021 and ASMC 2022.

Thank-you to the authors of the papers appearing in this Special Section for extending and improving upon their already outstanding papers. Thanks also to all the reviewers for their time and expertise in evaluating these works. Finally, we sincerely express our gratitude to Prof. Reha Uzsoy, TSM Editor-in-Chief, for the opportunity to highlight ASMC 2020 and 2021 in this Special Section, and for his continuing support of ASMC.

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APPENDIX: RELATED ARTICLES

[A1] S. Hong, I. Hwang, and Y. J. Jang, "Practical Q-learning-based route-guidance and vehicle assignment for OHT systems in semiconductor fabs," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 385–396, Aug. 2022.

[A2] C. Flechsig, J. Lohmer, R. Lasch, B. Zettler, G. Schneider, and D. Eberts, "Streamlining semiconductor manufacturing of 200 mm and 300 mm wafers: A longitudinal case study on the lot-to-order-matching process," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 397–404, Aug. 2022.

[A3] R. Buengener *et al.*, "Nondestructive detection of buried and latent defects by negative mode E-beam inspection," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 405–411, Aug. 2022.

[A4] D. Schmidt *et al.*, "Development of SiGe indentation process control for gate-all-around FET technology enablement," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 412–417, Aug. 2022.

[A5] M. P. McLaughlin *et al.*, "Improved color defect detection with machine learning for after develop inspections in lithography," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 418–424, Aug. 2022.

[A6] J. Reche, P. Gergaud, Y. Blancquaert, M. Besacier, and G. Freychet, "Shape and roughness extraction of line gratings by small angle X-ray scattering: Statistics and simulations," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 425–431, Aug. 2022.

[A7] T. Alcaire, D. Le Cunff, S. Soulan, and J.-H. Tortai, "On the fly ellipsometry imaging for process deviation detection," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 432–438, Aug. 2022.

[A8] B. Williams, R. Davis, E. W. Cowell, J. Yerger, B. Greenwood, and T. Ruud, "Source pad design tradeoffs for a power TrenchFET," *IEEE Trans. Semicond. Manuf.*, vol. 35, no. 3, pp. 439–445, Aug. 2022.

Oliver D. Patterson (Senior Member, IEEE) received the S.B. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, the M.S. degree in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, and the Ph.D. degree in electrical engineering from the University of Michigan at Ann Arbor, Ann Arbor, MI, USA. He is a Senior Engineer with Intel, Hillsboro, OR, USA, where his focus is application of E-beam inspection technology for development of advanced semiconductor technologies. He has previously worked for ASML, Globalfoundries, IBM, Lucent Technologies, and Agere Systems. His research interests include the use of e-beam inspection for detection of voltage contrast and physical and pattern fidelity defects and yield improvement in general. He is a member of the ASMC Technical Committee and was the Conference Co-Chairman for ASMC 2014. He has served as the Guest Editor for the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING numerous times.

Delphine Le Cunff received the Bachelor of Engineering degree in material sciences from the National Institute of Applied Science, Rennes, France, in 1992, and the Ph.D. degree in physics from the University of Grenoble, France, in 1995.

She started her career in the semiconductor industry as an Application Engineer working for Therma-Wave, a major optical metrology supplier, from 1997 to 2006. She then joined STMicroelectronics, Crolles, France, where she held different technical and management positions in the metrology area. She is now a Senior Member of Technical Staff and is currently involved in innovation and development in the field metrology, process control, and manufacturing sciences. Her activities cover applications for a large panel of technologies, such as compound semiconductor, 3-D integration, and advanced nodes. Since 2014, she has been a member of the SEMI ASMC Technical and Steering Committees and served as the 2017 Conference Co-Chair.

Ralf Buengener received the Master of Arts degree from the University of Texas at Austin in 1998 and the Doctoral degree from the University of Halle, Germany, in 2003. He started his career with AMD, Dresden, Germany, that later became Globalfoundries. He held several roles in metrology and defect inspection for manufacturing, development, and research, most recently as assignee with Albany Nanotech in 7-nm EUV development. In 2018, he switched from logic to memory when he joined Intel's Nonvolatile Memory Group where he leads pathfinding research for defect inspection for 3-D NAND flash. He is a member of the ASMC Technical Committee and currently serves as a Guest Editor for the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING.

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Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program and in marketing strategy, also through Cornell. Since entering the semiconductor industry in 1980, he has been a hands-on Photolithography Process Sustaining Engineer in an Intel wafer fab; a Senior Plasma Etch Process Engineer with Hitachi High Technologies; the Country Manager for Tegal Japan Inc.; the Vice President of Marketing and Applications with Tegal Corporation; the Global Product Marketing Director of Intevac, Inc.; a Global Product Manager of NorCal Products, Inc.; and the Director of Product Management with Ichor Systems. He wrote the contributed chapter on TSV etching in the book *3D Integration for VLSI Systems*, and has written or co-written an extensive number of articles, papers, and blogs regarding the semiconductor capital equipment business, advanced packaging, and various aspects of semiconductor manufacturing. He is a member of the SEMI Advanced Semiconductor Manufacturing Conference Steering Committee and was the SEMI ASMC 2004 Conference Co-Chair. He is active in the Northern California Chapter of the American Vacuum Society and was the Program Chair for the NCCAVS Technical Symposium 2019 and the Chapter Chair in 2019. He is also a Guest Editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING.

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