Perspectives on Black Silicon in Semiconductor Manufacturing: Experimental Comparison of Plasma Etching, MACE, and Fs-Laser Etching

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***Abstract*—In semiconductor manufacturing, black silicon (bSi) has traditionally been considered as a sign of unsuccessful etching. However, after more careful consideration, many of its properties have turned out to be so superior that its integration into devices has become increasingly attractive. In devices where bSi covers the whole wafer surface, such as solar cells, the integration is already rather mature and different bSi fabrication technologies have been studied extensively. Regarding the integration into devices where bSi should cover only small selected areas, existing research focuses on device properties with one specific bSi fabrication method. Here, we fabricate bSi patterns with varying dimensions ranging from millimeters to micrometers using three common bSi fabrication techniques, i.e., plasma etching, metal-assisted chemical etching (MACE) and femtosecond-laser etching, and study the corresponding fabrication characteristics and resulting material properties. Our results show that plasma etching is the most suitable method in the case of μm-scale devices, while MACE reaches surprisingly almost the same performance. Femtosecond-laser has potential due to its maskless nature and capability for hyperdoping, however, in this study its moderate accuracy, large silicon consumption and spreading of the etching damage outside the bSi region leave room for improvement.**

***Index Terms*—Etching, laser ablation, nanotechnology, optoelectronic devices, photolithography, silicon.**

I. Introduction

BLACK silicon (bSi) is well-known for its surface that consists of micro and/or nanoscale structures, which can significantly improve the performance of different types of devices via, e.g., the reduction of optical losses [1]–[7] or the improvement of electrical properties [8], [9]. Indeed, there are extensive reports on different bSi fabrication techniques, such as plasma etching, metal-assisted chemical etching (MACE) and laser etching, the resulting material properties, the performance of the final devices [10]–[13] as well as the economic aspects [14], [15]. However, the previous studies focus on surface texturing of a large area or even the whole wafer [1]–[20], while there are plenty of applications that require a small active area, even as small as a few μm for single-photon detectors or detector arrays [21]. To meet these requirements, one needs to make bSi fabrication methods either compatible with photolithography or obtain comparable performance in alignment and pattern transfer accuracy.

While some small area bSi devices have been reported, those studies have typically relied on one single fabrication technique only focusing heavily on the device performance but ignoring the bSi characterization. Therefore, there is a need to compare how different bSi fabrication techniques perform with regards to small patterns and what the resulting bSi properties are. For example, both dry and wet bSi etching techniques can pattern the bSi structures using photolithography. However, they are known for their difference in the resulting sidewall characteristics, e.g., the under-etching and the slope [22]. Moreover, they also require proper selection of mask materials [23]. Finally, it is well known that the size of the area on the wafer to be etched will impact the process [24] and thus likely also the bSi nanostructures. On the other hand, when using a laser etching technique for fabricating bSi, there is no need for a separate mask and the total bSi area should not affect the bSi properties unless the pattern size is comparable to the used laser spot size. Other aspects to consider include silicon consumption during etching, i.e., the depth at which the final nanostructures are located under the original surface as well as what happens in the vicinity of the pattern edge both inside and outside the bSi area.

Here, we fabricate patterned bSi areas with varying dimensions ranging from millimeters to micrometers using different bSi fabrication techniques: i) inductively coupled plasma–reactive ion etching (ICP-RIE), i.e., plasma etching, ii) MACE and iii) femtosecond-pulsed laser (fs-laser) etching. In addition to studying the alignment and pattern transfer accuracy of each method, we characterize the resulting material properties including surface morphology, silicon consumption as well as optical and electrical properties. Finally, we compare the different methods from the semiconductor device manufacturing point of view.

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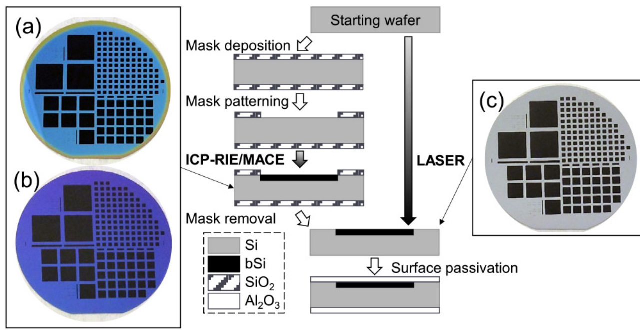

Fig. 1. Process flow chart for surface-patterned and passivated bSi wafers. Optical photographs of the patterned Si wafers directly after bSi formation with the different etching methods are also shown: (a) ICP-RIE, (b) MACE, (c) fs-laser (Note that bSi areas are black to eyes in these photos). ICP-RIE and MACE methods require an etching mask while fs-laser etched bSi can be fabricated directly on the desired areas.

II. Methods

To have a systematic comparison among plasma etching, MACE and fs-laser bSi fabrication methods, all samples were fabricated and characterized using wafers cut from the same ingot. The substrates (supplier Topsil GlobalWafers A/S) were 4-inch boron-doped (p-type) float-zone (FZ) single-side polished crystalline silicon wafers with a resistivity of 1–5 Ω·cm, a thickness of 280 μm and an orientation of (100). In the beginning, the wafers were oxidized at 1000 °C for 84 min by wet oxidation to grow 438±2 nm of SiO_2 on both sides as measured by Ellipsometer Plasmos SD2300. This thermal treatment also eliminates the possible bulk defects [25], [26]. Next, the silicon oxide layer was used as an etching mask for ICP-RIE and MACE as seen in Fig. 1. The oxide was patterned with optical photolithography using a photomask with patterns in various sizes and shapes. In the case of fs-laser etching, the oxide was removed as the fs-laser etching did not require an etching mask.

The bSi surface structures were fabricated by ICP-RIE, MACE and fs-laser etching methods on selected Si areas of separate wafers with parameters used in our previous studies, which were earlier optimized to result in low optical reflection on large or full wafer areas. The ICP-RIE bSi sample was fabricated by a cryogenic process (chamber temperature of −120 °C) using Oxford Instruments Plasmalab System 100 - ICP 180 with detailed setup described in Refs. [3], [4], [27], [28]. The wafers were etched in SF_6/O_2 plasma for 7 min with the flow rates set to 40 and 18 sccm for SF_6 and O_2, respectively, and the chamber pressure during the process was 10 mTorr. The powers of inductively (ICP) and capacitively coupled (CCP) power sources were 1000 and 2 W, respectively, with a bias of 0 V. The MACE bSi sample was fabricated by a two-step MACE process adopted from ref. [29]. The first step used a solution consisting of HF(50%):H_2O_2(30%):H_2O (90:11:363, vol%) and 0.4 mmol/l $AgNO_3$ with a duration of 70 s. The second step used a HF(50%):H_2O_2(30%):H_2O (5:2:54, vol%) solution with a duration of 120 s. Finally, Ag nanoparticles were removed by dipping the samples into a 69 % HNO_3 solution for 15 min and diluted HF solution sequentially. The fs-laser etched bSi sample was fabricated using Azpect/Newport laser micromachining system with Spectra-Physics Spirit 1040-16-SHG laser source (520 nm wavelength, 324 fs pulse duration and 417 kHz repetition rate) [30]. The wafer was selectively etched by using a line hatch pattern with a 35 μm spacing and a 150 mm/s scan speed as controlled by a Galvo scanner, under the laser spot diameter of ∼80 μm and a fluence of 5.4 kJ m^{-2}.

Fig. 1 shows the optical photos of the patterned Si wafers after (a) ICP-RIE, (b) MACE and (c) fs-laser etching, respectively. Since the ICP-RIE and the MACE processes consumed a different thickness of SiO_2, the resulting patterned SiO_2 films have a different color in Fig. 1(a) and (b). As a final step for the bSi fabrication by ICP-RIE and MACE, the silicon oxide mask was removed using a buffered oxide etch (BOE) solution.

For surface passivation, after cleaning with standard RCA solutions, an Al_2O_3 layer was grown on both sides of each wafer with an atomic layer deposition (ALD) tool Beneq TFS-500. The deposition used alternating vapor precursors of trimethylaluminum (TMA) and H_2O in 200 °C for 200 cycles, resulting in 20 nm film thickness as characterized with an ellipsometer. Finally, the samples were annealed in N_2 ambient at 400 °C for 30 min to activate the passivation [31].

The surface morphology of the fabricated bSi samples was observed with a Zeiss Supra 40 Field-Emission Scanning Electron Microscope (SEM). The step profile from the unetched surface to the tips of the nanostructures was measured using a Bruker Dektak XT stylus profilometer. The optical properties were measured using a Cary 5000 UV-Vis-NIR spectrophotometer equipped with an integrating sphere and the light spot focused on the sample was about 5 × 10 mm^2. The reflectance (R) and transmittance (T) of the samples were measured to calculate the absorption (A) using A = 1 − R − T. Moreover, calibrated lifetime images were obtained by measuring the photoluminescence (PL) count with a spatial resolution of 30 μm using BT Imaging LIS-R2+ and calibrating the PL count by μPCD measurement from Semilab WT-85 [32].

III. Results

A. Alignment and Pattern Transfer Accuracy, and Surface Morphology

Fig. 2 shows optical microscope images of both the photomask (1st column) and the bSi patterns obtained using different fabrication methods. The ICP-RIE (2nd column) and MACE (3rd column) bSi patterns look identical to the photomask at a low magnification. However, for a circle area with a diameter of 90 μm predefined by the photomask (last row), the higher magnification shows a difference of ∼−0.2 μm and ∼+1.6 μm from the photomask to the corresponding ICP-RIE and MACE patterns, respectively. This comparison indicates that ICP-RIE most likely has a positive sidewall slope while MACE has an isotropic nature, which results in slightly larger pattern size compared to that in the photomask. Please notice that here the comparison is done to the photomask pattern and not to the actual resist or oxide mask pattern

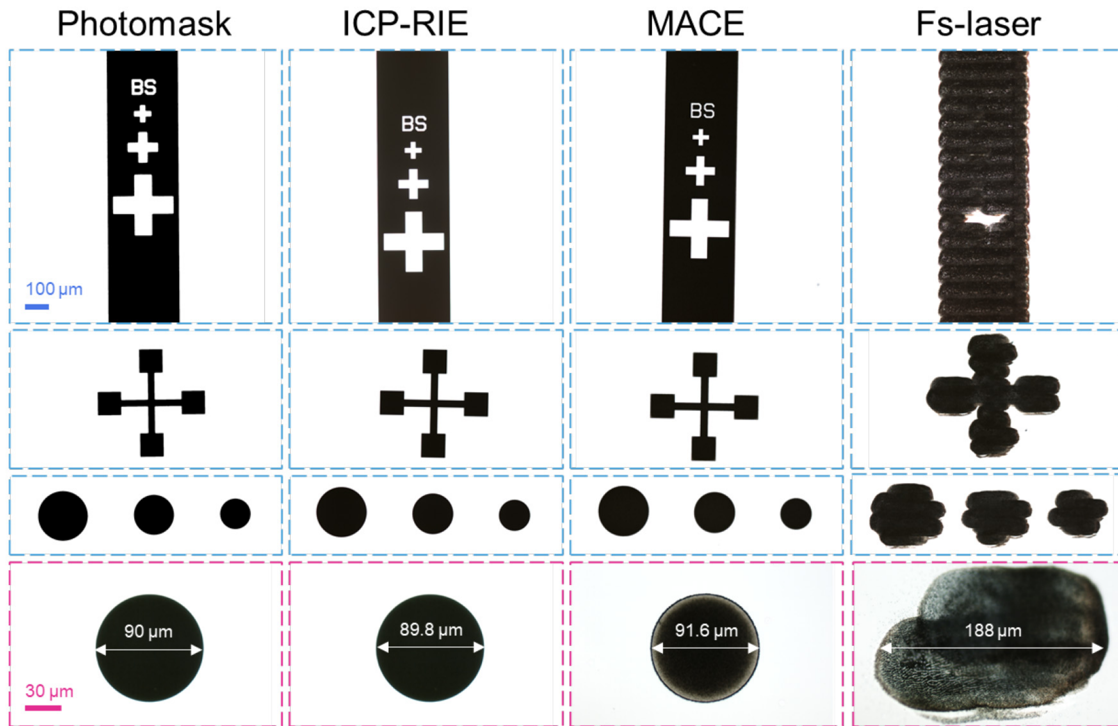

Fig. 2. Optical microscope images of small features on the photomask and on the patterned wafers etched with different methods. The 100 µm scale bar applies to all images in the first three rows, and the 30 µm scale bar applies to the last row. The diameters on the last row are measured with ImageJ software. Note that the color does not represent the actual reflectance.

on the wafer. Depending on the lithography parameters, the deviation between the photomask and the lithographic feature could possibly add some inaccuracy. Nevertheless, because the lithography parameters used here were identical for both ICP-RIE and MACE, they are directly comparable with each other. In addition to the pattern size, with the high magnification, the edge of the MACE pattern shows roughness and there is a clear contrast gradient near the edge, which probably indicates a nonuniform etching profile (which will be further characterized later). Fs-laser etched patterns (4th column) deviate significantly from the photomask even with the low magnification both in terms of size and shape. It is worth mentioning that the rough patterns are created by direct laser 'writing' and the fabrication is not specifically optimized for a high size accuracy.

To see the etched features more closely, we use SEM as shown in Fig. 3. Firstly, we focus on the letter "B" corresponding to that in Fig. 2 (note that the polarity of the pattern is opposite to the circles presented in Fig. 2). Fig. 3(a) and 3(b) show the resulting dimensions in ICP-RIE and MACE etched wafers, respectively. In addition, as already visible in Fig. 2, our fs-laser processing is not able to reproduce such a small pattern. The schematic in Fig. 3(c) summarizes the obtained dimensions on the wafer as compared to the photomask. In the photomask the width of the letter "B" is 9 µm. After ICP-RIE, the width of the planar region on the wafer is ~8.4 µm and the pattern spreads as the etching depth increases reaching a value of ~9.3 µm at the bottom. For MACE, the corresponding values are ~6.0 µm and ~8.7 µm, respectively. These imply that in the case of ICP-RIE, there is only slight under etching taking place and the resulting sidewall has indeed a positive slope, whereas for MACE, the under etching is more pronounced and the sidewall has a gentler positive slope. As mentioned earlier, for more accurate absolute under etching determination, actual lithographic features could be used as the reference. Fig. 3(d)–(f) show more closely both the sidewall and the nanostructures close to it. For ICP-RIE the sidewall is smooth, and the nanostructures are similar both near and far from the edge. For MACE, the sidewall roughness is apparent, and the nanostructures seem to be shorter near the sidewall. As mentioned earlier, after fs-laser etching there is no distinctive edge as the size of the nanostructures becomes gradually smaller as the distance from the center of the laser spot increases.

As seen in Fig. 3(g)–(i), far away (>50 µm) from the edge, the nanostructures look typical consisting of rather randomly formed different sizes and shapes. Both ICP-RIE and MACE result in similar needle-like nanostructures with large height-to-width ratio. In more detail, for ICP-RIE the majority of the structures are individual needles with rather uniform height and base dimensions. For MACE the typical structures are somewhat shorter and there is more variation in the base dimensions most probably due to uneven sizes of Ag nanoparticles deposited during the first MACE step. In contrast, the fs-laser etching results in much larger structures with hierarchical micro- and nano-sized features. These observations agree with those obtained from larger areas previously [1], [3]–[5], [28]–[30]. However, it is also well known that the morphology of the etched structures depends heavily on the used etching parameters.

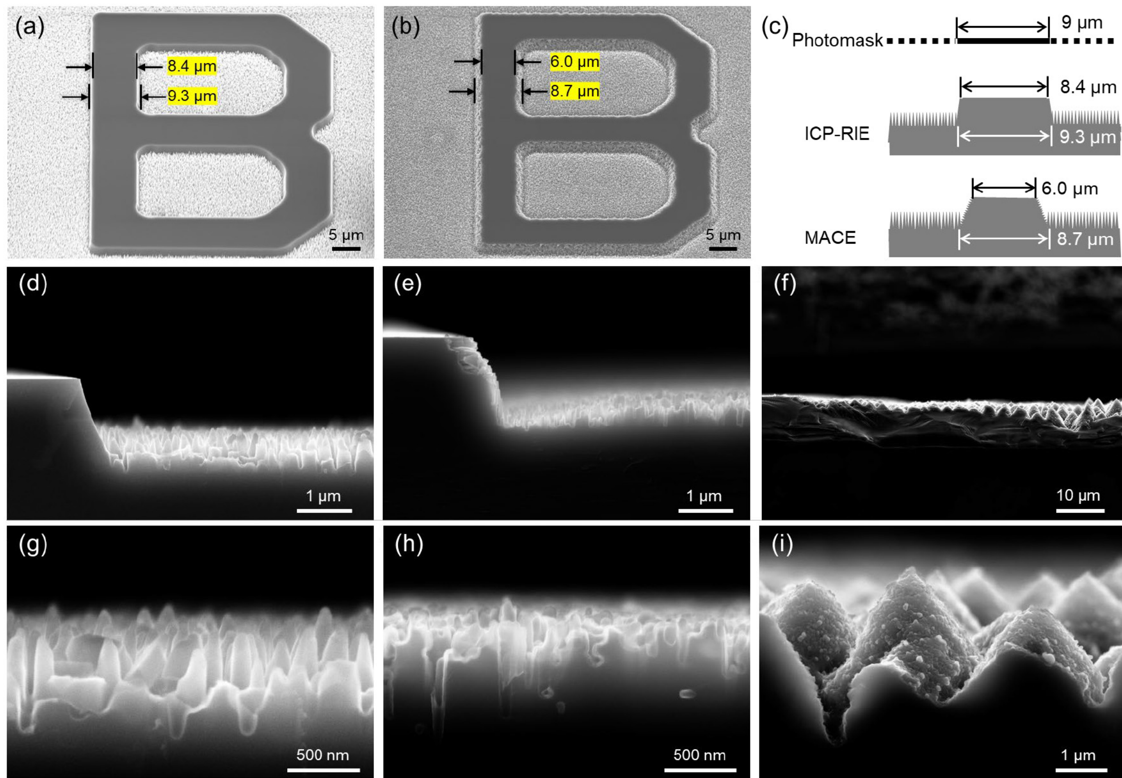

Fig. 3. Tilted SEM views obtained by (a) ICP-RIE and (b) MACE using the same mask pattern. (c) Schematic drawing on the comparison between the pattern size on the photomask and the resulting dimensions on the wafer after ICP-RIE and MACE. Cross-sectional SEM images of the etched area both at and far away from the edge after (d,g) ICP-RIE, (e,h) MACE and (f,i) fs-laser, respectively.

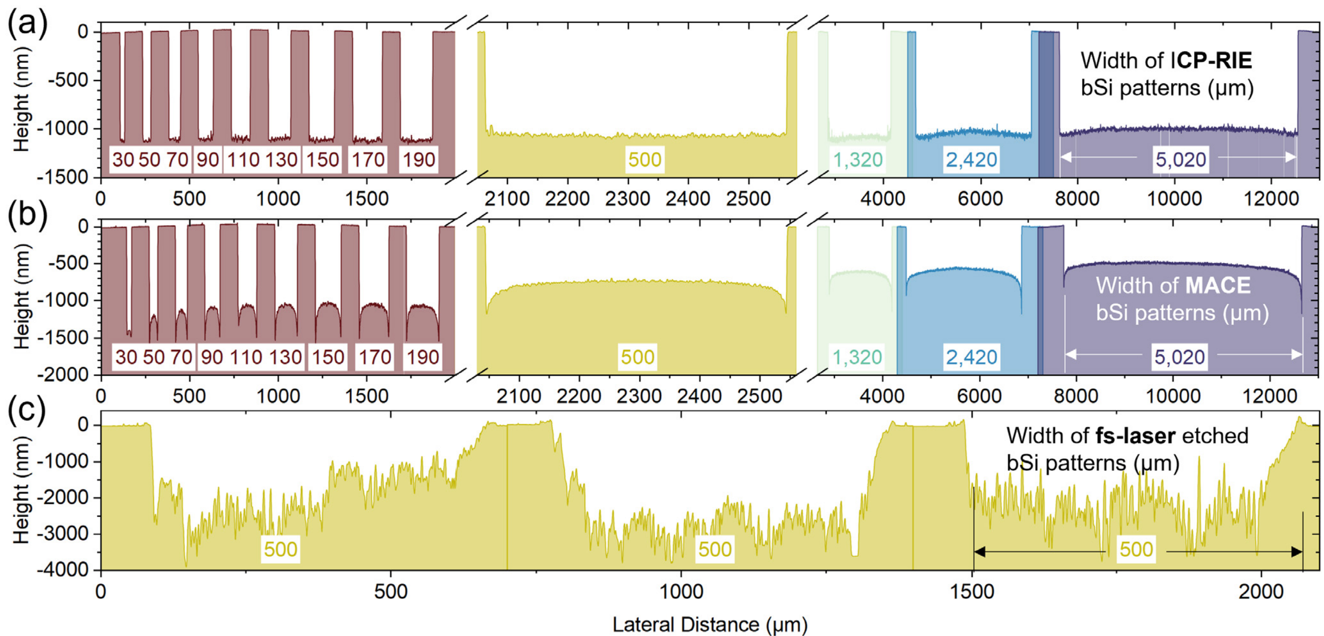

Fig. 4. Macroscopic etching profiles as well as the depth of the etched step as measured with profilometry from bSi patterns with varying widths fabricated by (a) ICP-RIE and (b) MACE. (c) For fs-laser bSi the profilometer result is shown only for a 0.5 mm wide groove. Note different x- and y-axis scales.

B. Silicon Consumption and Macroscopic Etching Profiles

Fig. 4 shows macroscopic etching profiles as well as the depth of the etched step as measured with profilometry from bSi patterns with varying width. In Fig. 4(a), the ICP-RIE patterns have relatively flat etching profiles, meaning the etching rate of ICP-RIE is rather uniform not only near the edge as mentioned above, but also far away from the edge. However, in the case when the mask pattern is in the range of millimeters the etch depth starts to slowly decrease. Overall, ICP-RIE consumes a Si thickness of $\sim$1.1 μm. In the case of

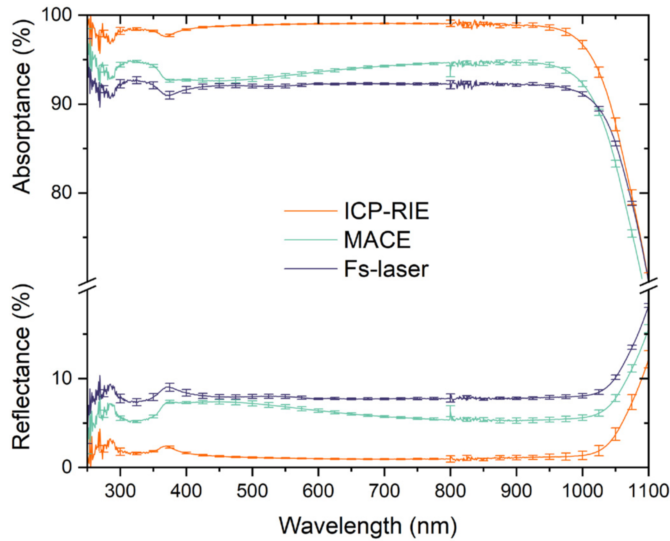

Fig. 5. Optical reflectance and absorptance spectra measured from patterned bSi areas. For each fabrication method, the spectra are averaged from 5 different patterns with a size of 10 × 10 mm^2 and the error bars denote the standard deviation from the average values.

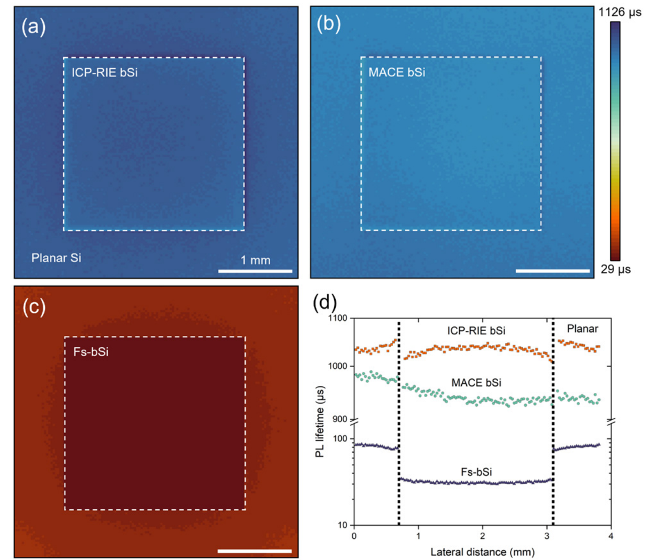

Fig. 6. (a–c) Lifetime calibrated PL images measured from patterned wafers etched by ICP-RIE, MACE, and fs-laser methods, respectively with the same scale bar (1 mm). The side length of each patterned bSi area is 2.5 mm. (d) Line scan of lifetime for the different bSi fabrication methods.

MACE, it is noticeable from Fig. 4(b) that the etching profile is very much curved, as the etching profile is deeper near the edges and shallower in the center. For example, with a 500 μm wide bSi pattern a difference in height of about 400 nm is measured and the lateral range of the curved region is about 200 μm. The observation of this curved profile in small MACE patterns has not been reported before to our knowledge but could be a crucial factor for designing small devices. Moreover, the etching rate seems to depend much more on the mask pattern width for MACE than for ICP-RIE. The MACE consumes Si only ∼0.5 μm in larger structures while in small structures the consumption is as high as ∼1.5 μm. In contrast, due to the larger etching structures, the fs-laser patterned bSi area in Fig. 4(c) has much more fluctuated etching profiles and the Si consumption is several micrometers. Finally, it is good to notice that the stylus used for the profilometry has a larger tip (∼2 μm) than the spacing of the bSi structures so that it cannot reach the bottom of the nanostructures. Consequently, the profilometer measurements only show the approximate level at which the tips of the bSi structures are located.

C. Optical Properties and Minority Carrier Lifetime

Fig. 5 shows the total optical reflectance and absorptance from patterned bSi areas. Low reflectance (below 10%) in a wide spectral range is measured in all samples of the same size with high pattern-to-pattern repeatability. As indicated by the typical morphologies seen in the closer SEM inspection, the obtained reflectance and absorptance values are indeed in the same range than reported earlier on large areas [1], [3]–[5], [28]–[30]. Based on SEM one could expect differences between the edge and center area especially for MACE due to the clear difference in the nanostructure size. However, considering that the light spot size used in the measurements was close to the actual pattern size, the effect of the edges is efficiently averaged out and thus this potential difference is not visible in the results. It is good to keep in mind that the optical properties originating from different surface morphologies, are also highly dependent on the fabrication process parameters. For instance, if one needs to optimize the reflectance, based on our experience, that often leads to compromises in etching duration and Si consumption. More precisely, the etching duration is usually correlated to the resulting depth of the nanostructures and hence also to the reflectance [18]. It is also worth mentioning that possible post-etching processes could slightly affect the optical properties, e.g., due to the chemical etching of surface textures during the following cleaning steps [29], [33] or due to the deposition of a passivation film [28].

Lifetime calibrated photoluminescence imaging is performed for the surface passivated bSi patterns, as shown in Fig. 6(a)–(c). For direct comparison the line scan from each PL image is plotted in Fig. 6(d). As seen, the minority carrier lifetimes in both planar and patterned bSi areas from ICP-RIE and MACE are very similar and reach a high value of 1 ms. For the fs-laser method, the bSi area has a much lower lifetime with an average of about 25 μs and therefore it exhibits a clear contrast with the planar area. Moreover, rather surprisingly, the maximum lifetime in the planar region is much lower than in the cases of ICP-RIE and MACE reaching only about 100 μs, even at a distance of 1 mm from the lasered area. The result means that the effect of fs-laser on lifetime is not limited to the patterned bSi area but extends laterally even up to 5 mm (not shown) to the adjacent planar areas. The low lifetime in the laser processed area is attributed to various types of laser-induced defects and contaminants in earlier studies [10]–[13]. In our recent study, we were able to recover the lifetime in a similarly laser processed bSi area back to ms-level by etching a very thin (a few μm) layer away from the sample surface after laser processing [34]. This result indicates that the damage originating from the fs-laser texturing extends only to the depth of a few μm in vertical direction. We would expect the damage to behave similarly also in lateral direction.

Therefore, the reason for the significant extension of the low lifetime area outside the lasered areas remains unclear and would be worth of further studies.

IV. DISCUSSION

We have shown that the alignment and pattern transfer accuracy depend on the used bSi fabrication techniques. While plasma etching and MACE methods are compatible with photolithography and the alignment is not an issue, we observed some challenges in pattern transfer accuracy. More specifically, ICP-RIE resulted in relatively accurate pattern dimensions down to μm-scale and with proper process tuning it should be possible to reach even totally vertical sidewalls with negligible under-etching that improves the accuracy further. Naturally, the ultimate limit for the smallest possible area comes from the dimensions of the actual nanostructures (i.e., the width of a single nanostructure). MACE showed more pronounced deviation due to the under-etching, and due to the isotropic nature of the process it would be challenging to further improve the accuracy. In contrast, our fs-laser etching process resulted in significant spreading of the patterns, which is sure to limit its integration into μm-level devices. However, it should be possible to further improve the pattern accuracy by using smaller laser spot size, which can be achieved with a shorter wavelength and an increasing numerical aperture of the laser optical system [35].

For both ICP-RIE and MACE methods, we chose SiO_2 hard mask to sustain a CMOS-compatible process. When selecting proper mask materials, in addition to the selectivity, one needs to also consider the etching conditions. For example, in the ICP-RIE the cryogenic temperature may set some limitations, e.g. some photoresists are known to suffer from cracking [24]. For MACE, the used chemicals are often rather harsh, such as HF and HNO_3, limiting the possible material candidates. Nevertheless, there are some promising results with photoresist [36]. Naturally none of these issues need to be considered in the case of fs-laser.

As all the methods to fabricate black silicon are based on etching, the final nanostructures are located below the original wafer surface. While it is theoretically possible that the tips of the nanostructures are at the same level than the wafer surface, in practice they are usually much lower – for instance in this study from ∼1 μm (ICP-RIE and MACE) to a few μm (fs-laser) below the surface. We found out that similar to the traditional dry and wet etching, the etch depth of bSi structures depends on the pattern dimensions. In the case of ICP-RIE this dependency was almost negligible, whereas in MACE the etch depth was clearly higher for smaller mask patterns. This behavior could be explained by the so-called loading effect, which has roots in reactant supply and consumption balance [24]. All these need to be taken into consideration in device designs and process flows as the whole device is no longer at one constant level. For instance, if the doping is done prior to the bSi etching, the doped areas may be totally removed or at least are quite different if most of the dopants are etched away. On the other hand, if the doping is done after bSi formation, it can be challenging to form the electrical contact between the doped bSi and the doped planar surface if the doping profile in the latter is not deep enough or if there is significant variation in the mask pattern dimensions leading to different bSi structure depths. Another challenge related to silicon consumption is confronted when the bSi is to be fabricated on a thin epitaxial layer. In that case the Si consumption determines the minimum required thickness of the epilayer and in the worst case the smallest structures penetrate through the epilayer.

Based on the reflectance curves presented in Fig. 5, the optical properties seem not to depend on the size of the etched area as the reflectance spectra are similar to what we have obtained in full wafers. However, with our equipment we were able to measure accurately only rather large areas (>1 cm^2). Therefore, if one is interested in looking at the optical properties in μm-scale areas, a better means to evaluate them is the morphology of the nanostructures obtained via SEM. In ICP-RIE no differences were seen in the morphology between the center and the edge of the bSi area. In the case of MACE, SEM revealed somewhat smaller nanostructures close to the edge of the bSi area, which indicates challenges for patterned bSi areas that are in μm range. For fs-laser method, as inferred from the different bSi structures near and away from the pattern edge, the optical properties change gradually, and the lowest reflectance seems to be achieved only tens of μm away from the edge independent of the size of the bSi area.

Minority carrier lifetime is a crucial parameter in devices that require the collection of excited minority carriers, e.g., in photodiodes. Our results show that in ICP-RIE and MACE the bSi surface does not limit the lifetime when passivated with ALD Al_2O_3. This indicates that the methods do not introduce defects or damage in the nanostructures. Fs-laser etched bSi surfaces, on the other hand, seem to suffer from severe recombination clearly limiting the lifetime. Interestingly, the low lifetime in the fs-laser etched samples extends even outside the lasered areas. This means that, e.g., in arrayed devices the spacing between the bSi patterns cannot be small, if the interplay with the neighboring pixels would be an issue.

V. CONCLUSION

We have fabricated bSi with ICP-RIE (plasma etching), MACE and fs-laser etching methods with varying mask pattern dimensions ranging from mm to μm. Our focus has been in systematic comparison of resulting bSi material properties between the different etching methods. The results demonstrate that with ICP-RIE, bSi can be formed with high alignment and pattern transfer accuracy without compromising neither optical nor electrical properties even in the case of μm-scale patterns. In many cases the performance of MACE reached surprisingly close to that of ICP-RIE. The most distinctive differences were noticed in the etch depth dependency on the mask pattern width and the flatness of the macroscopic bottom profile of the etched feature. While femtosecond-pulsed laser is an attractive alternative for bSi fabrication due to its maskless nature and capability for hyperdoping, the laser

system used in this study seemed not directly applicable for fabricating bSi in μm-scale patterns.

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References

[1] K. Chen, O. E. Setälä, B. Radfar, U. Kroth, V. Vähänissi, and H. Savin, "Harnessing carrier multiplication in silicon solar cells using UV photons," *IEEE Photon. Technol. Lett.*, vol. 33, no. 24, pp. 1415–1418, Dec. 15, 2021, doi: 10.1109/LPT.2021.3124307.

[2] S. Huang *et al.*, "Black silicon photodetector with excellent comprehensive properties by rapid thermal annealing and hydrogenated surface passivation," *Adv. Opt. Mater.*, vol. 8, no. 7, Apr. 2020, Art. no. 1901808, doi: 10.1002/adom.201901808.

[3] M. A. Juntunen, J. Heinonen, V. Vähänissi, P. Repo, D. Valluru, and H. Savin, "Near-unity quantum efficiency of broadband black silicon photodiodes with an induced junction," *Nat. Photon.*, vol. 10, no. 12, pp. 777–781, Dec. 2016, doi: 10.1038/nphoton.2016.226.

[4] H. Savin *et al.*, "Black silicon solar cells with interdigitated back-contacts achieve 22.1% efficiency," *Nat. Nanotechnol.*, vol. 10, no. 7, pp. 624–628, Jul. 2015, doi: 10.1038/nnano.2015.89.

[5] M. Garin *et al.*, "Black-silicon ultraviolet photodiodes achieve external quantum efficiency above 130%," *Phys. Rev. Lett.*, vol. 125, no. 11, Sep. 2020, Art. no. 117702, doi: 10.1103/PhysRevLett.125.117702.

[6] S.-X. Ma *et al.*, "Enhanced responsivity of co-hyperdoped silicon photodetectors fabricated by femtosecond laser irradiation in a mixed SF_6 /NF_3 atmosphere," *J. Opt. Soc. Amer. B*, vol. 37, no. 3, pp. 730–735, Mar. 2020, doi: 10.1364/JOSAB.374044.

[7] F. Yang *et al.*, "Dual protection layer strategy to increase photoelectrode–catalyst interfacial stability: A case study on black silicon photoelectrodes," *Adv. Mater. Interfaces*, vol. 6, no. 8, Apr. 2019, Art. no. 1802085, doi: 10.1002/admi.201802085.

[8] T. P. Pasanen, H. S. Laine, V. Vähänissi, J. Schön, and H. Savin, "Black silicon significantly enhances phosphorus diffusion gettering," *Sci. Rep.*, vol. 8, no. 1, p. 1991, Dec. 2018, doi: 10.1038/s41598-018-20494-y.

[9] T. P. Pasanen *et al.*, "Impact of black silicon on light- and elevated temperature-induced degradation in industrial passivated emitter and rear cells, " *Progr. Photovolt. Res. Appl.*, vol. 27, no. 11, pp. 918–925, Nov. 2019, doi: 10.1002/pip.3088.

[10] X. Liu, P. R. Coxon, M. Peters, B. Hoex, J. M. Cole, and D. J. Fray, "Black silicon: Fabrication methods, properties and solar energy applications," *Energy Environ. Sci.*, vol. 7, no. 10, pp. 3223–3263, 2014, doi: 10.1039/C4EE01152J.

[11] Q. Tan, F. Lu, C. Xue, W. Zhang, L. Lin, and J. Xiong, "Nano-fabrication methods and novel applications of black silicon," *Sens. Actuat. A, Phys.*, vol. 295, pp. 560–573, Aug. 2019, doi: 10.1016/j.sna.2019.04.044.

[12] Z. Fan *et al.*, "Recent progress of black silicon: From fabrications to applications," *Nanomaterials*, vol. 11, no. 1, p. 41, Dec. 2020, doi: 10.3390/nano11010041.

[13] M. Otto *et al.*, "Black silicon photovoltaics," *Adv. Opt. Mater.*, vol. 3, no. 2, pp. 147–164, Feb. 2015, doi: 10.1002/adom.201400395.

[14] C. Modanese, H. S. Laine, T. P. Pasanen, H. Savin, and J. M. Pearce, "Economic advantages of dry-etched black silicon in passivated emitter rear cell (PERC) photovoltaic manufacturing," *Energies*, vol. 11, no. 9, p. 2337, Sep. 2018, doi: 10.3390/en11092337.

[15] N. Van Toan, X. Wang, N. Inomata, M. Toda, I. Voiculescu, and T. Ono, "Low cost and high-aspect ratio micro/nano device fabrication by using innovative metal-assisted chemical etching method," *Adv. Eng. Mater.*, vol. 21, no. 8, Aug. 2019, Art. no. 1900490, doi: 10.1002/adem.201900490.

[16] X. Jin *et al.*, "High-performance free-standing flexible photodetectors based on sulfur-hyperdoped ultrathin silicon," *ACS Appl. Mater. Interfaces*, vol. 11, no. 45, pp. 42385–42391, Nov. 2019, doi: 10.1021/acsami.9b16667.

[17] M. Anwar, Y. Sabry, P. Basset, F. Marty, T. Bourouina, and D. Khalil, "Black silicon-based infrared radiation source," in *Proc. Silicon Photon. XI*, Mar. 2016, Art. no. 97520E, doi: 10.1117/12.2211668.

[18] K. N. Nguyen, P. Basset, F. Marty, Y. Leprince-Wang, and T. Bourouina, "On the optical and morphological properties of microstructured black silicon obtained by cryogenic-enhanced plasma reactive ion etching," *J. Appl. Phys.*, vol. 113, no. 19, May 2013, Art. no. 194903, doi: 10.1063/1.4805024.

[19] Y. Zhang *et al.*, "Negative photoconductivity in sulfur-hyperdoped silicon film," *Mater. Sci. Semicond. Process.*, vol. 98, pp. 106–112, Aug. 2019, doi: 10.1016/j.mssp.2019.04.002.

[20] A. Y. Vorobyev and C. Guo, "Direct creation of black silicon using femtosecond laser pulses," *Appl. Surf. Sci.*, vol. 257, no. 16, pp. 7291–7294, Jun. 2011, doi: 10.1016/j.apsusc.2011.03.106.

[21] F. Acerbi, G. Paternoster, A. Gola, N. Zorzi, and C. Piemonte, "Silicon photomultipliers and single-photon avalanche diodes with enhanced NIR detection efficiency at FBK," *Nucl. Instrum. Methods Phys. Res. Sect. A, Accelerators Spectrometers Detectors Assoc. Equip.*, vol. 912, pp. 309–314, Dec. 2018, doi: 10.1016/j.nima.2017.11.098.

[22] M. Yusuf *et al.*, "Optimized deep reactive-ion etching of nanostructured black silicon for high-contrast optical alignment marks," *ACS Appl. Nano Mater.*, vol. 4, no. 7, pp. 7047–7061, Jul. 2021, doi: 10.1021/acsanm.1c01070.

[23] R. K. Dey, H. Ekinci, and B. Cui, "Effects of mask material conductivity on lateral undercut etching in silicon nano-pillar fabrication," *J. Vac. Sci. Technol. B*, vol. 38, no. 1, Jan. 2020, Art. no. 12207, doi: 10.1116/1.5123601.

[24] V. Lindroos, M. Tilli, A. Lehto, and T. Motooka, *Handbook of Silicon Based MEMS Materials and Technologies*. Amsterdam, The Netherlands: Elsevier, 2010.

[25] N. E. Grant *et al.*, "Permanent annihilation of thermally activated defects which limit the lifetime of float-zone silicon," *Physica Status Solidi*, vol. 213, no. 11, pp. 2844–2849, Nov. 2016, doi: 10.1002/pssa.201600360.

[26] J. Ott, T. P. Pasanen, P. Repo, H. Seppänen, V. Vähänissi, and H. Savin, "Passivation of detector-grade float zone silicon with atomic layer deposited aluminum oxide," *Physica Status Solidi*, vol. 216, no. 17, Sep. 2019, Art. no. 1900309, doi: 10.1002/pssa.201900309.

[27] L. Sainiemi *et al.*, "Non-reflecting silicon and polymer surfaces by plasma etching and replication," *Adv. Mater.*, vol. 23, no. 1, pp. 122–126, Jan. 2011, doi: 10.1002/adma.201001810.

[28] P. Repo *et al.*, "Effective passivation of black silicon surfaces by atomic layer deposition," *IEEE J. Photovolt.*, vol. 3, no. 1, pp. 90–94, Jan. 2013, doi: 10.1109/JPHOTOV.2012.2210031.

[29] K. Chen, T. P. Pasanen, V. Vahanissi, and H. Savin, "Effect of MACE parameters on electrical and optical properties of ALD passivated black silicon," *IEEE J. Photovolt.*, vol. 9, no. 4, pp. 974–979, Jul. 2019, doi: 10.1109/JPHOTOV.2019.2917787.

[30] X. Liu, B. Radfar, K. Chen, T. P. Pasanen, V. Vähänissi, and H. Savin, "Tailoring femtosecond-laser processed black silicon for reduced carrier recombination combined with >95% Above-Bandgap Absorption," *Adv. Photon. Res.*, vol. 3, Apr. 2022, Art. no. 2100234, doi: 10.1002/adpr.202100234.

[31] G. Dingemans, M. C. M. van de Sanden, and W. M. M. Kessels, "Influence of the deposition temperature on the c-Si surface passivation by Al_2O_3 Films Synthesized by ALD and PECVD," *Electrochem. Solid-State Lett.*, vol. 13, no. 3, p. H76, 2010, doi: 10.1149/1.3276040.

[32] H. M. Ayedh *et al.*, "Fast wafer-level characterization of silicon photodetectors by photoluminescence imaging," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2449–2456, May 2022, doi: 10.1109/TED.2022.3159497.

[33] T. P. Pasanen, H. S. Laine, V. Vahanissi, K. Salo, S. Husein, and H. Savin, "Impact of standard cleaning on electrical and optical properties of phosphorus-doped black silicon," *IEEE J. Photovolt.*, vol. 8, no. 3, pp. 697–702, May 2018, doi: 10.1109/JPHOTOV.2018.2806298.

[34] X. Liu *et al.*, "Millisecond-level minority carrier lifetime in femtosecond laser-textured black silicon," *IEEE Photon. Technol. Lett.*, early access, Jul. 12, 2022, doi: 10.1109/LPT.2022.3190270.

[35] M. Y. Shen, C. H. Crouch, J. E. Carey, and E. Mazur, "Femtosecond laser-induced formation of submicrometer spikes on silicon in water," *Appl. Phys. Lett.*, vol. 85, no. 23, pp. 5694–5696, Dec. 2004, doi: 10.1063/1.1828575.

[36] A. G. Nassiopoulou, V. Gianneta, and C. Katsogridakis, "Si nanowires by a single-step metal-assisted chemical etching process on lithographically defined areas: Formation kinetics," *Nanoscale Res. Lett.*, vol. 6, no. 1, p. 597, Dec. 2011, doi: 10.1186/1556-276X-6-597.