

Guest Editorial

Special Section on the 2019 SEMI Advanced Semiconductor Manufacturing Conference

DEAR readers—We hope this editorial finds you and your family safe as we and the world battle—or, hopefully at the time of this publication, recover from—perhaps the greatest world-wide health crisis in the last century, COVID-19. Fortunately, the contributions of our semiconductor manufacturing industry over the last 40 years have put us in a much more comfortable position than those who faced past pandemics. It is likely that many of you have been working from home using your high-speed Internet connection and one of multiple computers that you and most families own. The worldwide Internet and computing infrastructure that our industry has enabled allows many engineers and others to VPN into work, communicate and share documents via e-mail, and attend video meetings. On the personal side, you can keep up with family and friends, with the latest news, and information and instructions from the government. Semiconductors allow your children to attend (or perhaps teach) school remotely. Certainly school aged children will be missing contact with their friends, but, fortunately, they can still video chat, message, or at least call friends with their mobile phones. The whole family can enjoy their favorite shows and movies via streaming services, and of course try new video games.

On the global scale, our industry has enabled many tools for the health industry to combat COVID-19, tools such as gene sequencing in an effort to develop a vaccine, and advanced semiconductor technology is essential for creating and running computer models to predict the course of the disease with and without strong counter measures such as social distancing. Three-dimensional printing is being used to more quickly generate medical supplies, and crowd sourced temperature readings are being used to monitor average client temperatures by county. Factories are ever-more automated, allowing production in the semiconductor industry, and other industries to continue with skeleton staff. This backdrop is a good reminder that we in the semiconductor industry should continue to do what we are doing, which is doubling semiconductor capability every two years or so for the same cost. One critical component is the exchange of ideas through conferences such as the SEMI Advanced Semiconductor Manufacturing Conference (ASMC). This IEEE TSM Special Section highlights the 2019 30th ASMC conference which was held in Saratoga Springs, NY, USA, May 6 through May 9, 2019.

ASMC brings together semiconductor device manufacturers, equipment and materials suppliers, and members of academia in a forum to discuss a wide variety of important semiconductor manufacturing industry topics, including: Yield Enhancement, Advanced Metrology, Defect Inspection, Advanced Equipment and Materials, Factory Optimization, Advanced Process Control, Contamination Free Manufacturing, Materials Integration, and Photonics. Two parallel session tracks during the conference provide options to match the interests of each attendee without being overwhelming.

ASMC 2019 also allowed for extensive networking opportunities, since only through continuous collaboration can our industry continue to deliver the improvements that system level users have grown accustomed to. Session breaks, catered through the generosity of multiple corporate sponsors, make it very easy to catch up with old friends and to make new contacts. Two major social events are held after the first and second days of the conference. Day One culminated as usual with a poster session where one can meet individually with the more than 40 participating authors. Day Two ended with a major reception at the Canfield Casino (a historic building a nice stroll down Broadway from the conference center) complete with welcoming speeches from several of the important Saratoga Springs local dignitaries.

The 2019 conference (sponsored and organized by SEMI, with technical sponsorship from the IEEE Electron Devices Society) featured discussions on how technology/manufacturing is adapting to provide affordable solutions to support automotive and 5G applications. Robert Czetina, Vice President, Automotive Development Center, Infineon Technologies Austria AG, presented a keynote, “Megatrends Shaping the Automotive Market—Driven by Innovative Semiconductors,” that discussed new challenges semiconductor design and manufacturing teams need to meet to support the current and future needs of the automotive industry. Christine Dunbar, Vice President, RF Business Unit, GLOBALFOUNDRIES, focused on semiconductor manufacturing challenges needed to support 5G in her keynote, “You, Me & 5G: How 5G Will Change the Way We Work and Live.”

The well-received tutorial, “System Level Heterogeneous Integration Will Drive Fundamental Change in Manufacturing,” taught by Bill Bottoms, Ph.D., Co-Chair of the IEEE Heterogeneous Integration Roadmap effort, highlighted how semiconductor device packaging alternatives can support further system integration in light of the slowing

of Moore's law. This tutorial blended front end of the line semiconductor technologies with packaging alternatives that maximize integration and reduce system level costs.

ASMC 2019 also featured a panel discussion on "Time to Yield vs Time to Productivity: What Matters Most in the Age of More than Moore." Panelists for this session were five notable experts from along the semiconductor supply chain: Shiva Rai, Ph.D., Strategic Marketing Manager, 200mm Equipment Product Group (EPG), Applied Materials; Douglas A. Lawson, Executive Vice President—Corporate Marketing, Axcelis Technologies; Deb Leach, Vice President—Global Sourcing and Supply Chain, GLOBALFOUNDRIES; David Gross, Sr. Director—Manufacturing Technology, SkyWater Technology; and Jan Vardaman, President, TechSearch International. The panel discussion explored how best to reduce overall costs in manufacturing for system level products.

Robert Maire of Semiconductor Advisors closed out the conference with a very provocative forecast for the future of our industry entitled "Positioning is Everything—Where Are We in the Cycle."

In addition to awarding conference best paper and conference best student paper awards, ASMC, in partnership with the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, annually prepares a Special Section recognizing some of the best papers from the conference. Select authors are invited to submit papers that are extended and enhanced versions of their conference papers allowing them to highlight additional progress they have made since the conference. This Special Section on ASMC 2019 includes five such papers.

The first paper, by Narendra Chaudhary and Serap A. Savari discusses the use of deep neural networks to estimate the roughness of nanostructures in scanning electron microscopy images. Their training method uses supervised learning datasets of single-line and multiple-line SEM images as well as edge position information and multiple visualization tools. Results show a significant reduction in memory and computation needed for edge estimation with only a small impact on accuracy.

The second paper, by E. Gebreselasie *et al.*, describes characterization of eFuse programming for a variety of RF BiCMOS technology silicides. Ti, Co, Pt, and Ni salicide processes optimized for a range of CMOS technology nodes down to 90 nm were fabricated using 0.35 μm SiGe BiCMOS. On-wafer circuitry was used to program discrete eFuse elements to compare their pre- and post-programmed resistances as well as their behavior during programming between each salicide process employed. This work demonstrates the compatibility of eFuse technology across a range of process technology nodes, as well as its robustness in high reliability applications.

The third paper, by Artem Zhakov *et al.*, demonstrates how an artificial neural network-based approach is applicable

to automatic fault detection and classification in OHT rail systems used for material transport in 300 mm wafer fabs. By augmenting a synthetic data set with training data collected from measurements in off-line testing, the authors adapted their initial ANN model to better analyze real conditions in a working wafer fab. During in-fab testing, the trained ANN could correctly identify all four expected faults in OHT rails. Once fully integrated in the OHT network, this new measuring system can create real-time reports of current rail conditions; with these fault detection results, maintenance work assignments can be determined automatically, in a reliable and timely fashion. As a result, costly schedule-oriented preventive maintenance of OHT rail systems can potentially be replaced by condition-oriented maintenance.

The fourth paper, by Frieder H. Baumann *et al.*, reports on the use of an automated recipe for collection of EDS tomograms using a CD-TEM. This is advantageous since collection of the required 20–40 X-ray maps can take 1–4 hours, and automation both saves operator time and makes use of typically available off-hour CD-TEM time. In addition, this paper describes how detector shadowing can be reduced, using a special specimen holder and modified grids, to minimize radiation damage. These concepts were tested using examples from modern FinFET and non-volatile memory devices.

The fifth paper, by Richard F. Hafer *et al.*, describes an innovative way to use a large pixel-size e-beam inspection for detecting yield issues due to overpolish of replacement metal gate. This high volume manufacturing inspection was motivated by a disconnect between the established kerf structure used for process control and wide-gate structures. The inspection leverages the strong back-scattered electron signal of tungsten which protects underlying work function metal films. The premise of the inspection is that if no tungsten is remaining, then the work function metals are likely damaged.

Congratulations to Christopher Ebert, Linde, and Franz Heider, Infineon Technologies Austria AG, and Margaret Kindling, SEMI conference coordinator, for leading the effort to put together another outstanding Advanced Semiconductor Manufacturing Conference. Thank-you to the authors of the papers appearing in this Special Section for extending and improving upon their already outstanding papers. Thank-you also to all reviewers for their time and expertise in evaluating these works. We sincerely express our gratitude to Prof. Reha Uzsoy, TSM Editor-in-Chief, for the opportunity to highlight ASMC 2019 in this Special Section, and for his continuing support of ASMC, and we are also grateful to Rosemary Schreiber for her assistance in preparing this Special Section.

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Jeanne Paulette Bickford (Senior Member, IEEE) received the B.S. and Ph.D. degrees in chemistry from the University of Vermont, Burlington, VT, USA, in 1974 and 1986, respectively. Until her retirement in 2018, she was a Distinguished Member of Technical Staff and a Master Inventor with GLOBALFOUNDRIES, Essex Junction, VT, USA, leading ASIC product manufacturing integration and design for manufacturing for technologies from 7 to 65 nm. She was with IBM Microelectronics, where she held a variety of jobs in manufacturing engineering, project management, product engineering, and product development. She has 29 published papers and 93 issued U.S. patents in the field of semiconductor design for manufacturing. She is currently an Associate Editor and a Guest Editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING. She is a member of the SEMI ASMC Steering Committee and was the ASMC 2016 Conference Co-Chair.



Oliver D. Patterson (Senior Member, IEEE) received the S.B. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, the M.S. degree in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, and the Ph.D. degree in electrical engineering from the University of Michigan at Ann Arbor, Ann Arbor, MI, USA. He is a Distinguished Member of Technical Staff with ASML, San Jose, CA, USA. He serves the role of Principle Technologist for Hermes-Microvision, an ASML company and the industry's leading E-beam inspection tool supplier. He has previously worked with GLOBALFOUNDRIES, IBM Microelectronics, Lucent Technologies, and Agere Systems. His research interests include the use of e-beam inspection for detection of voltage contrast, physical and pattern fidelity defects and yield improvement in general. He is a member of the ASMC Technical Committee and was the conference Co-Chairman for ASMC 2014. He has served as a Guest Editor for the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING numerous times.



Stefan Radloff received the B.S. degree in mechanical engineering from the University of Tulsa, Tulsa, OK, USA, in 1993, and the M.S. degree in mechanical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1995. In 1995, he joined Intel, Chandler, AZ, USA, where he has been a part of Intel's Global Supply Management, Technology and Manufacturing Group. Since 2006, he has been a Technologist and has worked in a variety of roles across Intel's capital supply chain organization, including key roles in Intel's 300- and 450-mm wafer size transition programs. He has expertise in factory integration, industry standards, automation and equipment interfaces, wafer carriers, equipment performance, and supply chain management. He was the Co-Chair of the SEMI Advanced Semiconductor Manufacturing Conference in 2013.



Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program, and in marketing strategy, also through Cornell. Since entering the semiconductor industry in 1980, he has been a hands-on Photolithography Process Sustaining Engineer in an Intel wafer fab; a Senior Plasma Etch Process Engineer with Hitachi High Technologies; the Country Manager for Tegal Japan Inc.; the Vice President of Marketing and Applications with Tegal Corporation; the Global Product Marketing Director with Intevac, Inc.; and a Global Product Manager with Nor-Cal Products, Inc. He wrote the contributed chapter on TSV etching in the book *3D Integration for VLSI Systems*, and has written or co-written an extensive number of articles, papers, and blogs regarding the semiconductor capital equipment business, advanced packaging, and various aspects of semiconductor manufacturing. He is a member of the SEMI Advanced Semiconductor Manufacturing Conference Steering Committee, and was the SEMI ASMC 2004 Conference Co-

Chair. He is active in the Northern California Chapter of the American Vacuum Society for many years. He was the Program Chair for the NCCA VS Technical Symposium 2019 and the Chapter Chair in 2019. He is also a Guest Editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING.