A Precision Mismatch Measurement Technique for Integrated Capacitor Array Using a Switched Capacitor Amplifier

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***Abstract*—This paper presents a precision mismatch measurement method to characterize an integrated capacitor array. Conventional mismatch measurement methods using floating gate capacitance measurement (FGCM) have measurement error due to the large input-referred noise and the small input signal range of the source follower. In order to improve the measurement accuracy, we propose a new measurement method using a parasitic-insensitive switched capacitor amplifier and the correlated double sampling (CDS) technique. The CDS technique eliminates the measurement error from parasitic capacitances, switching errors, and the offset voltage of the amplifier. In order to verify the proposed method, a test chip was fabricated using a 0.18-μm CMOS process. The chip consists of a 4 × 16 metal–insulator–metal capacitor array and a measurement circuit. The measured standard deviation of the capacitance mismatch, $\sigma(\Delta C_n/<C>)$, ranges from 0.0067% to 0.0130%, and the measured standard deviation of the short-term repeatability, $\sigma(\Delta(\Delta C_n/<C>))$, is 0.0025%. These results show that the measurement accuracy of the proposed method is improved by ten times over that of the FGCM method.**

***Index Terms*—Capacitor array mismatch measurement, correlated double sampling (CDS), short-term repeatability, standard deviation of capacitance mismatch, switched capacitor amplifier.**

I. Introduction

THE INTEGRATED capacitor is an important component in many analog circuits such as active filters, analog-to-digital converters (ADCs), digital-to-analog converters (DACs). The performance of analog circuits is strongly affected by the matching characteristics of the capacitors [1]. Practically, most capacitors in analog circuits are designed as capacitor arrays in order to achieve high accuracy. In order to improve the matching property of the capacitor array, the array is designed with dummy capacitors or with large capacitances [2]. As a result, the capacitor array in high performance analog circuits consumes a large silicon area. However, high performance analog circuits using the capacitor array can be implemented in a small area through layout techniques ensuring accurate matching property of the capacitor array. Therefore, a high-precision measurement method is needed to measure the matching property of the capacitor array.

For the accurate matching characterization of a capacitor-pair, several capacitor mismatch measurement methods have been researched [3]–[12]. The traditional mismatch measurement methods are classified into the voltage-based measurement method [3]–[10], which is so-called the floating gate capacitance measurement (FGCM) method, and the frequency-based measurement method [11], [12]. The FGCM method presented in [3]–[10] measures the output voltage of the source follower, which is determined by the dividing ratio of a capacitive divider consisting of a capacitor under test (CUT) and a reference capacitor. The frequency-based measurement method presented in [11] and [12] measures the output frequency of a ring oscillator, which is determined by the capacitance of the CUT.

A study using the FGCM method to measure the mismatch property of a capacitor array was recently reported [13]. Although the FGCM method has the advantage of simple implementation using a source follower circuit, the measurement accuracy deteriorates in evaluating the capacitance mismatch of a capacitor array. The dividing ratio of a capacitive divider decreases as the number of capacitors in the capacitor array increases, so the input signal of the source follower in the FGCM circuit is reduced. The reduced input signal and the large input-referred noise of the source follower reduce the measurement accuracy of the FGCM method. The frequency-based measurement method is not also appropriate to measure the capacitance mismatch of a capacitor array because it cannot eliminate the measurement error from the large parasitic capacitances between the bottom plate of floating capacitors and the substrate. Accordingly, a new mismatch measurement method that is less affected by electrical noise and that can eliminate the measurement error from the parasitic capacitances is required for the matching characterization of the capacitor array.

In this paper, we propose a mismatch measurement method using a switched capacitor (SC) amplifier for the matching characterization of a capacitor array. To reduce the measurement error due to electrical noise, we use a SC amplifier with low input-referred noise and a fixed input signal range irrespective of the number of capacitors in the capacitor array. In addition, we employ the correlated double sampling (CDS)

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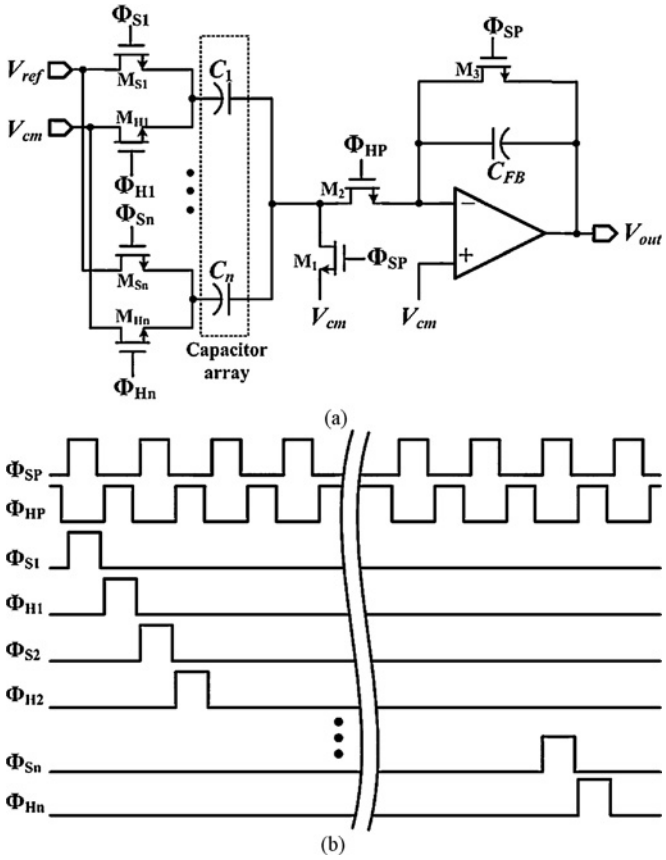

Fig. 1. (a) Schematic and (b) timing diagram of the switched capacitor amplifier for the proposed measurement method.

technique to eliminate the measurement error due to parasitic capacitances, switching errors, and the offset voltage of the amplifier.

In Section II of this paper, we explain the operation principle of the proposed measurement method and the structure of the test chip. In Section III, we discuss the measurement results of the proposed measurement method. Finally, the conclusions are given in Section IV.

II. Proposed Method and Test Structure

A. Operation Principle of Proposed Measurement Method

The schematic and the timing diagram of the proposed measurement method are shown in Fig. 1. The proposed measurement circuit consists of sampling switches ($M_{S1} - M_{Sn}$), holding switches ($M_{H1} - M_{Hn}$), a capacitor array, switches ($M_1 - M_3$) for a parasitic-insensitive SC amplifier, a feedback capacitor (C_{FB}), and an operational amplifier. The operation of the proposed measurement circuit is divided into a sampling phase and a holding phase, and is controlled by timing signals ($\Phi_{S1} - \Phi_{Sn}$, $\Phi_{H1} - \Phi_{Hn}$, Φ_{SP}, and Φ_{HP}). In the sampling phase, M_1, M_3, and one of the sampling switches are turned on and the other switches are turned off in order to select the capacitor for measurement and to initialize the SC amplifier. The voltage across the selected capacitor tracks to $V_{ref} - V_{cm}$ while the feedback capacitor is fully discharged. In the holding phase, M_2 and the holding switch connected to the selected capacitor are turned on and the other switches are turned off. The charge on the selected capacitor is transferred to the feedback capacitor, and the output voltage of the SC amplifier is determined by the ratio between the selected capacitor and the feedback capacitor. If the switching error can be neglected, the output voltage of the SC amplifier can be expressed as

$$V_{out} = \frac{C_n}{C_{FB}} \left(V_{ref} - V_{cm} \right) + V_{cm}, \tag{1}$$

where C_n, C_{FB}, V_{ref}, and V_{cm} are the selected capacitor in the capacitor array, the feedback capacitor, the reference voltage, and the common voltage, respectively.

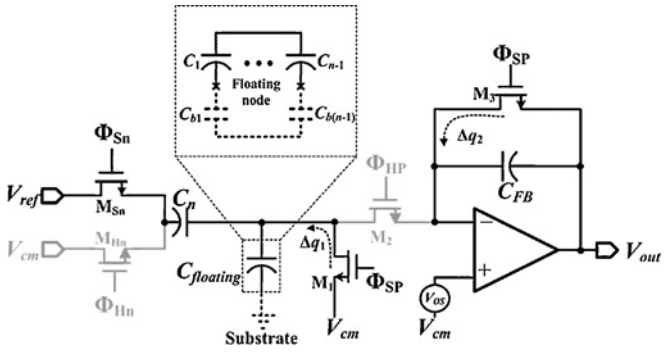

Fig. 2. Output voltage error generation mechanism of the parasitic-insensitive SC amplifier at the transition from the sampling phase to the holding phase.

The output voltage error of the SC amplifier occurs due to the offset voltage of the amplifier (V_{OS}), the parasitic capacitance ($C_{floating}$), and switching error such as the charge injection and the clock feed through of the switches. The output voltage error generation mechanism of the SC amplifier in the proposed measurement method is described in Fig. 2. $C_{floating}$ is the total parasitic capacitance formed by the unselected capacitors and the parasitic capacitors ($C_b - C_{b(n-1)}$). C_b is the capacitance between an unselected capacitor and the substrate. It can be expressed as

$$C_{floating} = \sum_{i=1}^{n-1} \frac{C_i \times C_{bi}}{C_i + C_{bi}}. \tag{2}$$

In Fig. 2, Δq_1 and Δq_2 are the charges from the switching errors of M_1 and M_3, respectively. To make the switching error into a constant offset, we employ a parasitic-insensitive SC amplifier [14]. At the transition to the holding phase, the M_1 and M_3 switch errors introduce the SC amplifier constant offset because the nodes of the switches are biased by V_{cm}. After the selected sampling switch, M_{Sn}, turns off, the total charge between the top plate of the selected capacitor and the top plate of the feedback capacitor cannot change, as no conducting path for the electrons exists. Consequently, the switch errors of the parasitic-insensitive SC amplifier become the constant offset. At the holding phase, the output voltage of the parasitic-insensitive SC amplifier can be expressed as

$$\begin{aligned} V_{out} = {} & \tfrac{C_n}{C_{FB}} \left(V_{ref} - V_{cm} \right) + \tfrac{(C_n - C_{floating})}{C_{FB}} V_{OS} \\ & + V_{cm} + V_{OS} + \tfrac{1}{C_{FB}} \left(\Delta q_1 + \Delta q_2 \right). \end{aligned} \tag{3}$$

V_{OS}, Δq_1, and Δq_2 contribute the offset error. However, the second term on the right-hand side of (3) varies with the

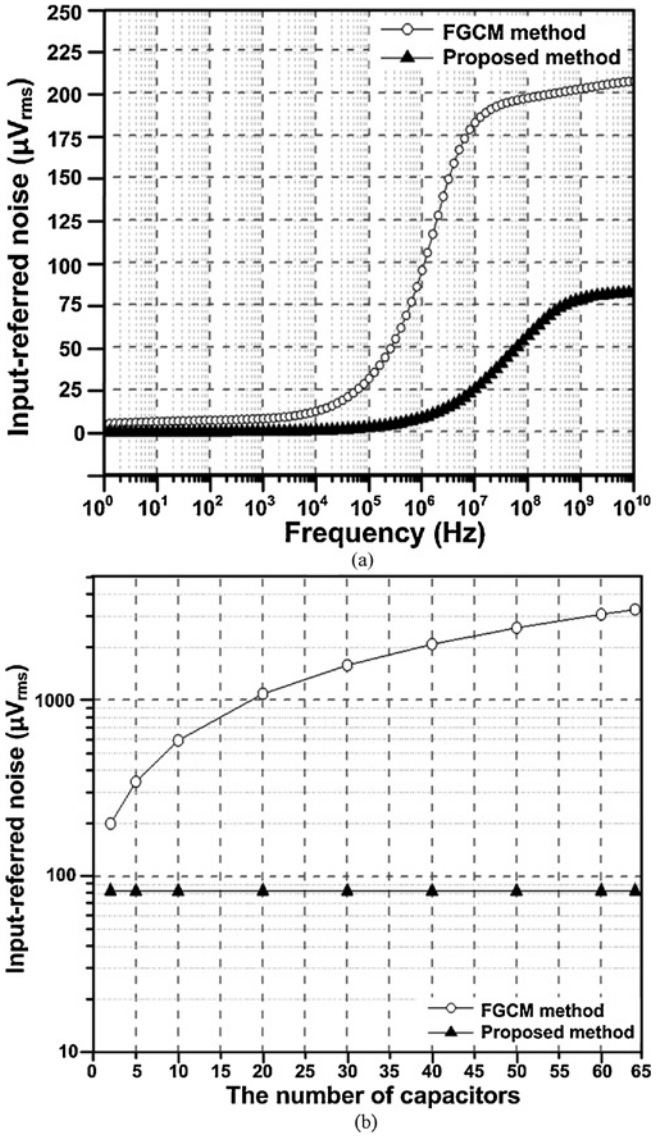

Fig. 3. Simulation results of (a) input-referred noise with respect to frequency in measuring the capacitor-pair and (b) input-referred noise, which is integrated from 1 Hz to 10 GHz, with respect to the number of capacitors.

differential value of C_n and $C_{floating}$. This term becomes the measurement error. To eliminate the measurement error, the proposed measurement method adopts the CDS technique. When the V_{ref} is V_{ref1} in the first measurement, the output voltage of the parasitic-insensitive SC amplifier is given by

$$V_{out\_m1} = \frac{C_n}{C_{FB}}\left(V_{ref1} - V_{cm}\right) + \frac{(C_n - C_{floating})}{C_{FB}} V_{OS} + V_{cm} + V_{OS} + \frac{1}{C_{FB}}(\Delta q_1 + \Delta q_2). \quad (4)$$

When the V_{ref} is V_{cm} in the second measurement, the output voltage of the parasitic-insensitive SC amplifier is given by

$$V_{out\_m2} = \frac{(C_n - C_{floating})}{C_{FB}} V_{OS} + V_{cm} + V_{OS} + \frac{1}{C_{FB}}(\Delta q_1 + \Delta q_2). \quad (5)$$

The difference in the output voltages is computed as

$$V_{outn} = V_{out\_m1} - V_{out\_m2} = \frac{C_n}{C_{FB}}(V_{ref1} - V_{cm}), \quad (6)$$

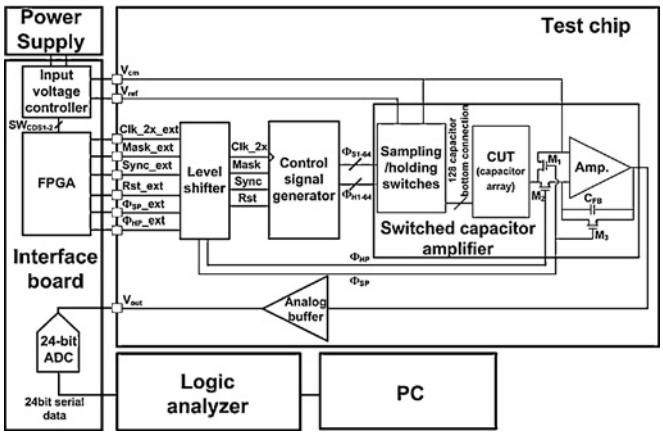

Fig. 4. Block diagram of the test chip and the setup environment of the proposed measurement method.

where V_{out_m1} and V_{out_m2} are the measured output voltages in the first and second measurement, respectively. Equation (6) shows that the measurement error is eliminated by the CDS technique. The measured capacitance mismatch of the selected capacitor can be expressed as

$$\frac{\Delta C_n}{< C >} = \frac{C_n - < C >}{< C >} = \frac{V_{outn} - < V_{out} >}{< V_{out} >}, \quad (7)$$

where $<V_{out}>$ is the average output voltage of the parasitic-insensitive SC amplifier and $<C>$ is the average capacitance of the capacitors in the capacitor array.

The noise of the measurement circuit also affects the measurement accuracy. The ideal input-referred noise [15] of the parasitic-insensitive SC amplifier can be expressed as

$$\overline{v_{n,in}^2} = \frac{2k\mathrm{T}}{C_{sampling}}\left(1 + \frac{1/6}{1 + 2R_{on}g_m}\right), \quad (8)$$

where $C_{sampling}$ is a selected capacitor in the capacitor array, k is the Boltzmann constant, T is the absolute temperature, R_{on} is the on-resistance of the sampling switch, and g_m is the transconductance of the amplifier. Equation (8) indicates that the noise of the parasitic-insensitive SC amplifier is dominated by the capacitance of the sampling capacitor, and is not related to the number of capacitors. Fig. 3 (a) and (b) show the simulation results of the input-referred noise with respect to frequency and the number of capacitors, respectively. In Fig. 3, the sampling capacitance and the feedback capacitance of the proposed measurement method are 1.6 pF and 0.8 pF, respectively, and the capacitance of the CUT in the FGCM method is 1.6 pF. Fig. 3 (a) shows that the input-referred noise of the proposed measurement circuit is lower than that of the FGCM circuit using the source follower with a length of 20 μm and a width of 100 μm in measuring the capacitor-pair. As shown in Fig. 3 (b), the input-referred noise of the FGCM circuit in [13] increases with respect to the number of capacitors in the capacitor array, whereas the noise of the proposed measurement circuit is constant. The simulated input-referred noise of the parasitic-insensitive SC amplifier is approximately 82.6 $\mu\mathrm{V_{rms}}$. When the capacitance of the sampling capacitor is 1.6 pF, the ideal minimum noise of the parasitic-insensitive SC amplifier is calculated to be about

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	D
D	C_{17}	C_{18}	C_{19}	C_{20}	C_{21}	C_{22}	C_{23}	C_{24}	C_{25}	C_{26}	C_{27}	C_{28}	C_{29}	C_{30}	C_{31}	C_{32}	D
D	C_{33}	C_{34}	C_{35}	C_{36}	C_{37}	C_{38}	C_{39}	C_{40}	C_{41}	C_{42}	C_{43}	C_{44}	C_{45}	C_{46}	C_{47}	C_{48}	D
D	C_{49}	C_{50}	C_{51}	C_{52}	C_{53}	C_{54}	C_{55}	C_{56}	C_{57}	C_{58}	C_{59}	C_{60}	C_{61}	C_{62}	C_{63}	C_{64}	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Fig. 5. Map of the capacitor array. D is a dummy capacitor that is connected to the ground.

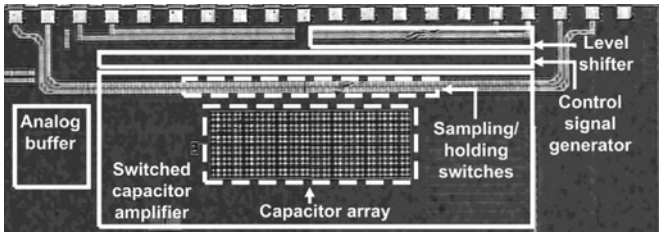

Fig. 6. Microphotograph of the fabricated test chip.

71.9 μ V_{rms} using (8). The difference between the simulation result and the calculated result occurs because the switches and the amplifier are not ideal. The noise immunity of the proposed measurement method is higher than that of the FGCM method because the input signal range of the parasitic-insensitive SC amplifier is fixed at $V_{ref} - V_{cm}$, and the input-referred noise of the parasitic-insensitive SC amplifier is lower than that of the source follower in the FGCM method. When the number of capacitors is 64, the input-referred noise of the proposed measurement method is about forty times less than that of the FGCM method.

B. Test Chip Structure

In order to verify the proposed method, a test chip was fabricated using a 0.18-μm 1-poly 4-metal CMOS process with 5 V analog CMOS devices. The block diagram of the test chip and the setup environment of the proposed measurement method are shown in Fig. 4. The test chip consists of a parasitic-insensitive SC amplifier with a 4 $\times$ 16 capacitor array and sampling/holding switches, a control signal generator, a level shifter, and an analog buffer. The capacitor array was fabricated using a metal-insulator-metal (MIM) capacitor. The control signals, which are Clk_2x_ext, Mask_ext, Sync_ext, Rst_ext, Φ_{SP}_ext, and Φ_{HP}_ext, are generated by the external field-programmable gate-array (FPGA) in the interface board. These control signals should be converted to 5 V control signals by the level shifter because the parasitic-insensitive SC amplifier uses 5 V control signals. The Clk_2x and Mask signals are used to generate the $\Phi_{S1} - \Phi_{S64}$ and $\Phi_{H1} - \Phi_{H64}$ signals in the control signal generator. The Rst and Sync signals are used to reset and synchronize, respectively, in the proposed measurement method. V_{ref} and V_{cm} are generated by the external power supply and are controlled by the input voltage controller in the interface board. The input voltage controller is controlled by the CDS control signals ($SW_{CDS1} - SW_{CDS2}$) generated by the FPGA. The output voltage of the parasitic-insensitive SC amplifier is transferred to an external 24-bit delta-sigma ADC through the analog buffer. The digital output code of the ADC is captured by a logic analyzer, and the captured digital code is then transferred to the PC for processing of the measured data.

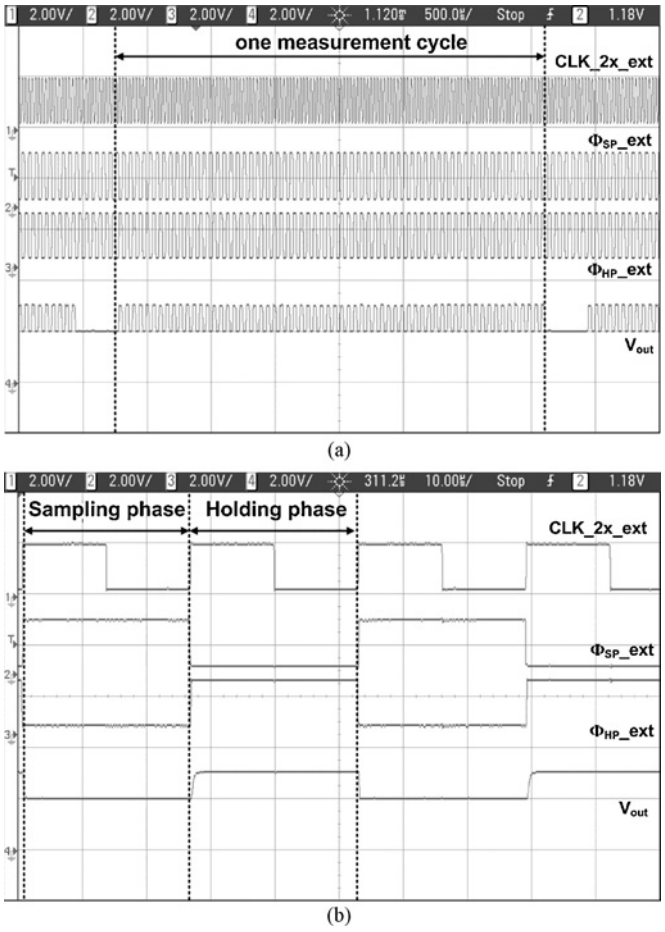

Fig. 7. Output voltage waveforms of the test chip at (a) one measurement cycle and (b) unit cycle.

In order to measure the matching property of the 4 $\times$ 16 capacitor array, the capacitor array is implemented as shown in Fig. 5. The top plate of the capacitors in the capacitor array is connected to the common node, whereas the bottom plate of each capacitor is connected to the sampling and holding switches. The areas of the capacitors in the capacitor array and the feedback capacitor are 40 μm $\times$ 40 μm and 20 μm$\times$40 μm, respectively. A microphotograph of the fabricated test chip is shown in Fig. 6.

III. Measurement Results and Parameter Extraction

A. Measurement Results of Test Chip and Parameter Extraction of Capacitance Mismatch

In order to verify the operation of the fabricated test chip, we measured the output voltage of the analog buffer using an oscilloscope. When V_{ref} is 2.5 V and V_{cm} is 2 V, the measured waveforms are shown in Fig. 7. The function of the test chip was confirmed by the measurement results. The number of the output voltage is 64 for the 4 $\times$ 16 capacitor array

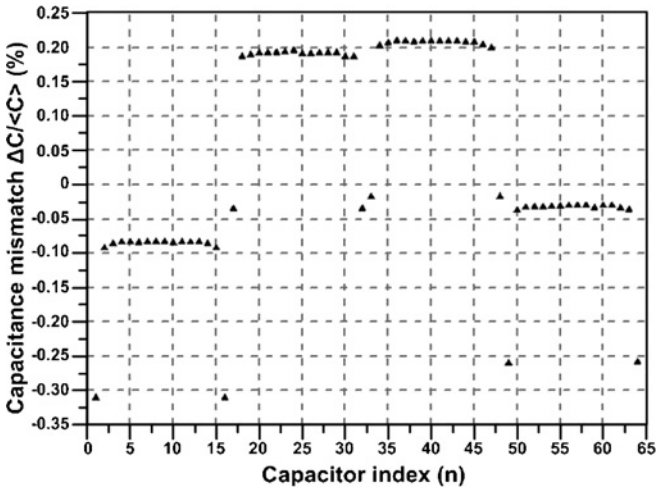

Fig. 8. Measured capacitance mismatch of the 4 × 16 capacitor array.

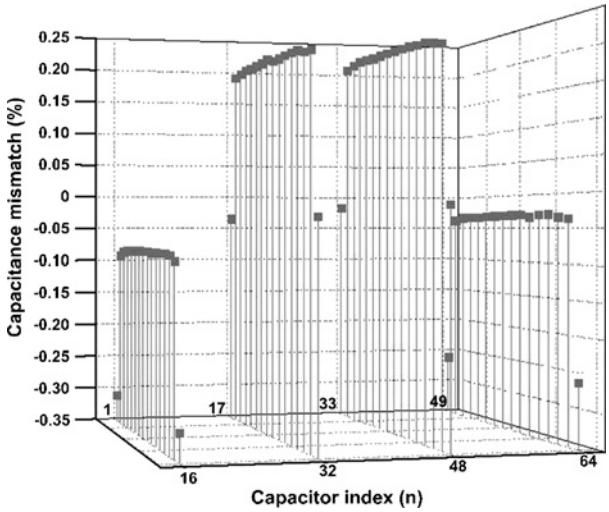

Fig. 9. 3-D scatter plot of the capacitance mismatch depending on the positions of capacitors.

during one measurement cycle. The proposed measurement method performs 100 measurement cycles to reduce the noise influence of the measurement system.

The mismatching parameters of the capacitor array can be extracted from the measured results. The capacitance mismatch of the capacitor is calculated using (7), and is shown in Fig. 8. The measured results show that the capacitance mismatch of the capacitor array is affected by the positions of the capacitors. Fig. 9 shows a 3-D scatter plot of the capacitance mismatch depending on the positions of the capacitors. The capacitance decreases from the center to the corner because the capacitor is affected by the dummy capacitors. Furthermore, the left side and the right side in Fig. 9 are asymmetrical because the capacitor array is affected by the parasitic capacitance between the bottom interconnection line metal and the top interconnection line metal of the capacitor array. The parasitic capacitance has different values because the bottom interconnection line metals of the capacitors have different lengths depending on the positions of the capacitors. Therefore, the capacitance of the right side is larger than that of the left side because the bottom interconnection line metal of the right side is longer than that of the left side.

B. Measurement Accuracy and Short-Term Repeatability of Proposed Measurement Method

In order to confirm the measurement accuracy of the proposed measurement method, we calculated the standard deviation of the measured capacitance mismatch. The measurement accuracy is affected by the noise of a measurement system, such as measurement circuit noise, environmental noise, and installation noise. Environmental noise is caused by conditions at the measurement site such as an electromagnetic interference. The installation noise is caused by a non-ideal measurement setup which is in turn caused by the accuracy limitation and the calibration error of the measuring instruments. In order to reduce the noise influence of the measurement system, several measurement cycles are performed and one measurement result is acquired by averaging these measurement cycles. When the number of the measurement cycle is small, the noise of the measurement system is a significant part of the measured result [6]. In order to avoid reduced measurement accuracy due to the noise of the measurement system, the proposed measurement method used 100 measurement cycles. The measurement accuracy is estimated using the standard deviation of the measured capacitance mismatch. To evaluate the standard deviation of the measured capacitance mismatch, we measured 50 test chips and the results are shown in Fig. 10. The standard deviation of the measured capacitance mismatch is given by

$$\sigma\left(\Delta C_n / < C >\right) = \sqrt{\frac{1}{50}\sum_{j=1}^{50}\left(\left(\frac{\Delta C_n}{\langle C\rangle}\right)_j - \left\langle\frac{\Delta C_n}{\langle C\rangle}\right\rangle\right)^2}, \tag{9}$$

where $(\Delta C_n / <C>)_j$ and $<\Delta C_n / <C>>$ are the measured capacitance mismatch of each test chip and the average capacitance mismatch of 50 test chips with respect to the capacitor index, respectively. The calculated standard deviation of the measured capacitance mismatch with respect to the capacitor index ranges from 0.0067% to 0.0130% and is shown in Fig. 11.

In addition, the short-term repeatability is verified in order to confirm the stability of the proposed measurement method. The short-term repeatability is the deviation between the measurement results under the same conditions. The short-term repeatability is acquired by calculating the difference in consecutive measurements at the same capacitor, and is defined as

$$\Delta\left(\frac{\Delta C_n}{< C >}\right) = \left(\frac{\Delta C_n}{< C >}\right)_1 - \left(\frac{\Delta C_n}{< C >}\right)_2, \tag{10}$$

where $(\Delta C_n / <C>)_1$ and $(\Delta C_n / <C>)_2$ are two consecutive measurement results with respect to the capacitor index, n. When 50 test chips are consecutively measured with 100 repetitions, the total number of measured short-term repeatability measurements is 320,000. The measured short-term repeatability of the proposed measurement method ranges from

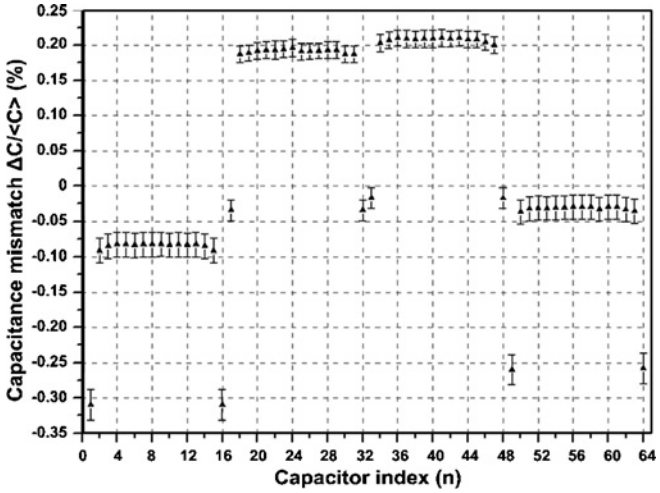

Fig. 10. Measured capacitance mismatch of 50 test chips. (▲) is the average capacitance mismatch of 50 test chips with respect to the capacitor index.

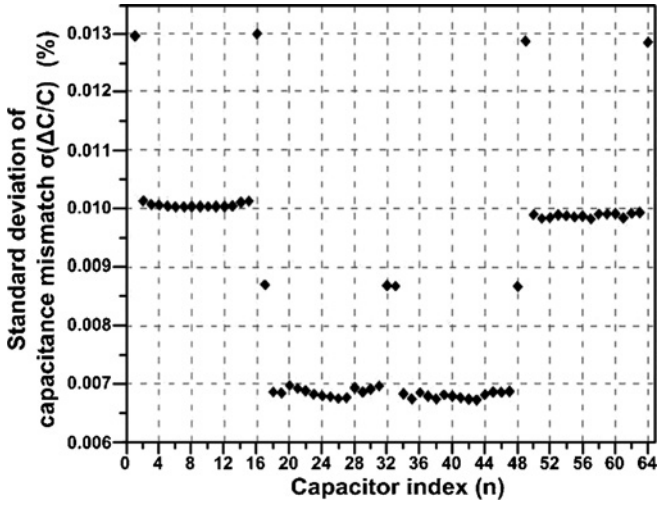

Fig. 11. Standard deviation of the capacitance mismatch with respect to the capacitor index.

-0.0060% to 0.0064%. The histogram and the cumulative probability plot of the short-term repeatability are shown in Fig. 12. The standard deviation of the short-term repeatability is given by

$$\sigma\left(\Delta\left(\frac{\Delta C_n}{<C>}\right)\right) = \sqrt{\frac{1}{320000}\sum_{i=1}^{320000}\left(\Delta\left(\frac{\Delta C_n}{<C>}\right)_i - \left\langle\Delta\left(\frac{\Delta C_n}{<C>}\right)\right\rangle\right)^2}, \tag{11}$$

where $\Delta(\Delta C_n/<C>)_i$ and $<\Delta(\Delta C_n/<C>)>$ are the measured short-term repeatability of the proposed measurement method and the average short-term repeatability, respectively. The calculated standard deviation of the short-term repeatability is about 0.0025%.

A comparison of the FGCM method and the proposed measurement method is summarized in Table I. The standard deviation of the measured capacitance mismatch means

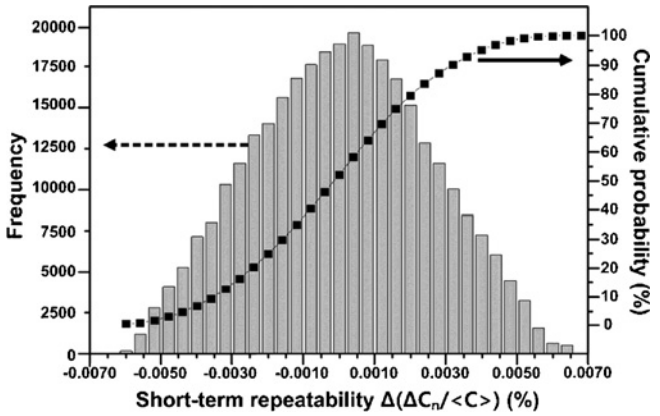

Fig. 12. Histogram and cumulative probability plot of the short-term repeatability of the proposed measurement method.

TABLE I
COMPARISON OF THE FGCM METHOD AND THE PROPOSED METHOD

Parameter	FGCM [13]	Proposed Method
Process	0.18-μm CMOS	0.18-μm CMOS
Number of capacitors	20	64
Capacitance mismatch of capacitor array $\Delta C_n/<C>$	-0.20 to 0.20%	-0.33 -0.22%
Standard deviation of capacitance mismatch $\sigma(\Delta C_n/<C>)$	0.060–0.100%	0.0067–0.0130%
short-term repeatability $\Delta(\Delta C_n/<C>)$	NA	-0.0060 to 0.0064%
Standard deviation of short-term repeatability $\sigma(\Delta(\Delta C_n/<C>))$	NA	0.0025%

that the measurement accuracy of the proposed measurement method is improved by ten times compared with that of [13]. The measured short-term repeatability indicates that the proposed measurement method has highly stable measurement outputs. Both the measurement accuracy and the short-term repeatability are affected by the noise of the measurement system. The accuracy and the short-term repeatability of the measurement results improve as the noise of the measurement system decreases. Therefore, as indicated by the results shown in Table I, the measurement accuracy and the short-term repeatability of the proposed measurement method are enhanced due to the low input-referred noise of the proposed measurement method.

IV. CONCLUSION

We introduce a measurement method that employs a parasitic-insensitive SC amplifier and the CDS technique for the matching characterization of a capacitor array. The proposed measurement method has high measurement accuracy because it has high noise immunity and eliminates the measurement error from the parasitic capacitance, the switching error, and the offset voltage of the amplifier. A test chip was fabricated to verify the proposed measurement method. The estimated measurement accuracy of the proposed measurement method ranges from 0.0067% to 0.0130%. This means that

the proposed measurement method can be used for measuring very low capacitance mismatches. Furthermore, the proposed measurement method can measure the capacitor array which is composed of many capacitors because the method is not affected by the number of capacitors.

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