

# Guest Editorial

## Special Section on the 2022 SEMI Advanced Semiconductor Manufacturing Conference

**T**HE 2022 ASMC, our 33rd, returned to Saratoga Springs, NY as an in-person conference after 2 years as a virtual conference. While we are all grateful for the digital world's enhancements that allowed this conference to be held remotely, attendees were happy to return to an in-person event where networking is much easier.

The SEMI Advanced Semiconductor Manufacturing Conference (ASMC) offers an outstanding opportunity to share and openly discuss innovative semiconductor manufacturing ideas relevant to leading-edge semiconductor manufacturers, as well as mature, but still vital, trailing-edge wafer fabs. ASMC brings together semiconductor manufacturers, equipment suppliers and academia as conference paper authors, presenters, panelists and attendees. The conference is sponsored and organized by Semiconductor Equipment and Materials International (SEMI), with technical sponsorship from the IEEE Electron Devices Society and the IEEE Electronics Packaging Society (previously known as the IEEE Components, Packaging, and Manufacturing Technology Society -CPMT).

The day one keynote featured Dr. Huiming Bu, Vice President, Hybrid Cloud Technology & Research & Albany Operation, IBM, who spoke about the Future of Semiconductors: Chips and Chiplets.

The day two keynote, "Product Innovation and the Acceleration of Design: Demand Drivers on a Secure and Resilient Supply Chain" was given by Deirdre Hanford, Chief Security Officer, Synopsys. She discussed challenges in the semiconductor industry from a design perspective. On day three, Bill Wiseman, Senior Partner and Global Co-Leader, Semiconductor Practice, McKinsey & Co gave an invited presentation on the Future of the U.S. Semiconductor Ecosystem.

Robert Maire, President Semiconductor Advisors closed out the conference with a keynote entitled "Insuring the Future of the Strategic Semiconductor Industry in the U.S." A highlight of the conference was the panel discussion lead by Fred Bouchard where the discussion centered around big data and artificial intelligence for operations management. The numerous supply chain issues seen throughout the pandemic in all industries and including the semiconductor industry made this an extremely timely and interesting discussion as we all reassess how we manage our supply chains.

The core of ASMC is made up of the many peer-reviewed papers that are presented in parallel session tracks. These papers cover a broad range of topics representative of the many challenges facing the semiconductor manufacturing industry including: Advanced Equipment, Processes & Materials, Advanced Metrology, Advanced Semiconductor Developments, Advanced Process Control, Contamination-Free Manufacturing, Defect Inspection, Failure Analysis, Industrial Engineering, Smart Manufacturing, Yield Enhancement and Yield Methodologies. This Special Section is a compilation of enhanced versions of some of the best papers from ASMC 2022. These papers were selected based both on the quality of the work they describe, and because they represent the range of topics covered at ASMC.

The paper by Xing et al. [A1] deals with the semiconductor industry conversion to modular fluid delivery system architectures. Benefits (smaller size/footprint, easily customizable configurability, ease of maintenance, and increased equipment productivity), serviceability, sealing mechanisms, and contamination control are discussed.

The next generation of semiconductor devices will require state-of-the-art statistical analyses to reduce measurement uncertainties. In [A2], Akpabio and Savari address this requirement. Their paper discusses procedures to generate prediction intervals based on image denoising and other image processing techniques and demonstrates significant improvement over earlier methods developed for the deep convolutional neural network EDGNet.

Chan et al. [A3] discuss inline electrical testing to monitor the baseline of analog computing hardware using phase change memory (PCM) technology. Tightening the PCM resistance distribution is necessary to meet analog computation requirement. A new yield methodology is introduced, and a study of heater process variation (which affects the heater height and the PCM resistance) is discussed.

In the paper by Edwards et al. [A4], the authors demonstrate the merits of a novel socket inspection system with the ability to detect a wide variety of defects in real-time and prevent excursions during production. The inspection system employs a variety of advanced image processing and computer vision techniques to identify potential outliers, and uses deep learning to sift through defect candidates, learn features to differentiate between true defects and natural socket deterioration, and correctly classify socket defects with very high accuracy.

Zhang et al. [A5] discuss enabling the use of glass wafers in a conventional Si fab. While the Si industry has created highly

sophisticated process capabilities in terms of feature size and high precision, combining these process capabilities with glass wafers creates new possibilities not only in novel device performance, but also economies of scale. Using glass requires overcoming multiple challenges - (lack of) glass opacity, conductivity, as well as metallic and particle contamination. The paper discusses challenges as well as solutions.

The paper by Patterson et al. [A6] introduces a new negative mode e-beam inspection technique that uses beam density as a control knob. This technique provides throughput, unique defect detection, wafer safety and charging advantages as compared to positive mode inspection for CMP layer analysis. Ways to achieve a negative mode are reviewed.

Thank-you to the authors of the papers appearing in this Special Section for extending and improving upon their already outstanding papers. Thanks also to all the reviewers for their time and expertise in evaluating these works. Finally, we sincerely express our gratitude to Prof. Reha Uzsoy, TSM Editor-in-Chief, for the opportunity to highlight ASMC 2022 in this Special Section, and for his continuing support of ASMC.

#### APPENDIX: RELATED ARTICLES

- [A1] G. Xing, P. Werbaneth, R. Treur, and P. Barros, "Modular fluid delivery system architectures drive configurability options, enhance semiconductor manufacturing equipment productivity, and improve process performance," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 311–318, Aug. 2023, doi: [10.1109/TSM.2023.3271286](https://doi.org/10.1109/TSM.2023.3271286).
- [A2] I. I. Akpabio and S. A. Savari, "On uses of noise analysis for the uncertainty quantification of line edge roughness estimation," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 319–326, Aug. 2023, doi: [10.1109/TSM.2023.3270230](https://doi.org/10.1109/TSM.2023.3270230).
- [A3] V. Chen et al., "Yield methodology and heater process variation in phase change memory (PCM) technology for analog computing," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 327–331, Aug. 2023, doi: [10.1109/TSM.2023.3284313](https://doi.org/10.1109/TSM.2023.3284313).
- [A4] C. Edwards, A. Vaske, N. McDaniel, D. Pradhan, and D. Panda, "Real-time change detection for automated test socket inspection using advanced computer vision and machine learning," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 332–339, Aug. 2023, doi: [10.1109/TSM.2023.3273175](https://doi.org/10.1109/TSM.2023.3273175).
- [A5] J. Zhang, C.-H. Ng, and S. Kouassi, "Enabling the use of high-precision glass wafers in a conventional Si Fab," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 340–344, Aug. 2023, doi: [10.1109/TSM.2023.3276165](https://doi.org/10.1109/TSM.2023.3276165).
- [A6] O. D. Patterson, et al., "Novel control method and applications for negative mode E-beam inspection," *IEEE Trans. Semicond. Manuf.*, vol. 36, no. 3, pp. 345–350, Aug. 2023, doi: [10.1109/TSM.2023.3284367](https://doi.org/10.1109/TSM.2023.3284367).

JEANNE PAULETTE BICKFORD, *Guest Editor*  
(Retired from) GLOBALFOUNDRIES  
Essex Junction, VT 05452 USA

OLIVER D. PATTERSON, *Guest Editor*  
Intel  
Hillsboro, OR, USA

DELPHINE LE CUNFF, *Guest Editor*  
STMicroelectronics  
38920 Crolles, France

RALF BUENGENER, *Guest Editor*  
Intel  
Santa Clara, CA, USA

STEFAN RADLOFF, *Guest Editor*  
Intel  
Chandler, AZ 85226 USA

PAUL WERBANETH, *Guest Editor*  
Independent Consultant  
Pittsburgh, PA, USA



**Jeanne Paulette Bickford** (Senior Member, IEEE) received the B.S. and Ph.D. degrees in chemistry from the University of Vermont, Burlington, VT, USA, in 1974 and 1986, respectively. Until her retirement in 2018, she was a Distinguished Member of Technical Staff and a Master Inventor with GLOBALFOUNDRIES, Essex Junction, VT, USA, leading ASIC product manufacturing integration and design for manufacturing for technologies from 7 to 65 nm. She was with IBM Microelectronics, where she held a variety of jobs in manufacturing engineering, project management, product engineering, and product development. She has published 29 papers and 94 issued U.S. patents in the field of semiconductor design for manufacturing. She is currently an Associate Editor and a Guest Editor for IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING. She is a member of the SEMI ASMC Steering Committee and was the ASMC 2016 Conference Co-Chair.



**Oliver D. Patterson** (Senior Member, IEEE) received the S.B. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, the M.S. degree in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, and the Ph.D. degree in electrical engineering from the University of Michigan at Ann Arbor, Ann Arbor, MI, USA. He is a Senior Engineer with Intel, Hillsboro, OR, USA, where his focus is application of E-beam inspection technology for development of advanced semiconductor technologies. He has previously worked for ASML, GLOBALFOUNDRIES, IBM, Lucent Technologies, and Agere Systems. He was the Conference Co-Chairman for ASMC 2014. He has served as a Guest Editor for the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING numerous times. He is a member of the IEEE EDS Committee on Semiconductor Manufacturing and the ASMC Technical Committee.



**Delphine Le Cunff** received the Bachelor of Engineering degree in material sciences from the National Institute of Applied Science, Rennes, France, in 1992, and the Ph.D. degree in physics from the University of Grenoble, France, in 1995. She started her career in the semiconductor industry as an Application Engineer working for Therma-Wave, a major optical metrology supplier from 1997 to 2006. Then, she joined STMicroelectronics, Crolles, France, where she held different technical and management positions in the metrology area. She is currently a Senior Member of Technical Staff and is currently involved in innovation and development in the field metrology, process control, and manufacturing sciences. Her activities cover applications for a large panel of technologies, such as compound semiconductor, 3-D integration, and advanced nodes. She served as the 2017 Conference Co-Chair. Since 2014, she has been a member of the SEMI ASMC Technical and Steering Committees.



**Ralf Buengener** received the Master of Arts degree from the University of Texas at Austin in 1998, and the Doctoral degree from the University of Halle, Germany, in 2003. He started his career with AMD, Dresden, Germany, that later became Globalfoundries. He held several roles in metrology and defect inspection for manufacturing, development, and research, most recently as assignee with Albany Nanotech in 7-nm EUV development. In 2018, he switched from logic to memory when he joined Intel's Nonvolatile Memory Group, where he leads pathfinding research for defect inspection for 3-D NAND flash. He currently serves as a Guest Editor for the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING. He is a member of the ASMC Technical Committee.



**Stefan Radloff** received the B.S. degree in mechanical engineering from the University of Tulsa, Tulsa, OK, USA, in 1993, and the M.S. degree in mechanical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1995. In 1995, he joined Intel, Chandler, AZ, USA, where he has been a part of Intel's Global Supply Management, Technology and Manufacturing Group. Since 2006, he has been a Technologist and has worked in a variety of roles across Intel's capital supply chain organization, including key roles in Intel's 300- and 450-mm wafer size transition programs. He has expertise in factory integration, industry standards, automation and equipment interfaces, wafer carriers, equipment performance, and supply chain management. He was the Co-Chair of the SEMI Advanced Semiconductor Manufacturing Conference in 2013.



**Paul Werbaneth** received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA. He recently completed studies in spoken Japanese from Cornell Summer FALCON Program and in marketing strategy, also through Cornell. Since entering the semiconductor industry in 1980, he has been a hands-on Photolithography Process Sustaining Engineer in an Intel wafer fab; a Senior Plasma Etch Process Engineer with Hitachi High Technologies; the Country Manager for Tegal Japan Inc.; the Vice President of Marketing and Applications with Tegal Corporation; the Global Product Marketing Director of Intevac, Inc.; a Global Product Manager of NorCal Products, Inc.; and the Director of Product Management with Ichor Systems. He wrote the contributed chapter on TSV etching in the book *3D Integration for VLSI Systems*, and has written or co-written an extensive number of articles, papers, and blogs regarding the semiconductor capital equipment business, advanced packaging, and various aspects of semiconductor manufacturing. He was the SEMI ASMC 2004 Conference Co-Chair, the Program Chair for the NCCAVS Technical Symposium 2019, and the Chapter Chair in 2019. He is active in the Northern California

Chapter of the American Vacuum Society. He is also a Guest Editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING and a member of the SEMI Advanced Semiconductor Manufacturing Conference Steering Committee.