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Physics-Based Models for Magneto-Electric Spin-Orbit Logic Circuits

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ABSTRACT Spintronic devices provide a promising beyond-complementary metal-oxide-semiconductor (CMOS) device option, thanks to their energy efficiency and compatibility with CMOS. To accurately capture their multiphysics dynamics, a rigorous treatment of both spin and charge and their inter-conversion is required. Here, we present physics-based device models based on 4 × 4 matrices for the spin-orbit coupling (SOC) part of the magneto-electric spin-orbit (MESO) device. Also, a more rigorous physics model of ferroelectric and magnetoelectric (ME) switching of ferromagnets, based on Landau–Lifshitz–Gilbert (LLG) and Landau–Khalatnikov (LK) equations, are presented. With the combined model implemented in a SPICE circuit simulator environment, simulation results were obtained which show feasibility of the MESO implementation and the functional operation of buffers, synchronous oscillators, and majority gates.

INDEX TERMS Beyond complementary metal-oxide-semiconductor (CMOS) logic, magnetoelectric (ME), SPICE, spin-orbit (SO), spintronic devices.

I. INTRODUCTION–SIMULATIONS OF BEYOND CMOS CIRCUITS

THE scaling of integrated circuits based on complementary metal-oxide-semiconductor (CMOS) transistors has been carried out over the last four decades in agreement with the Moore's law [1], [2]. In the last 15 years, power density is becoming a more critical limitation [3]. To address this issue and to assure continued scaling, beyond CMOS devices have been explored. They are intended to complement CMOS and be monolithically integrated in the same die. Compared with traditional CMOS-based circuits, new computing variables – ferroelectric polarization and magnetization – were utilized in beyond CMOS devices. Via systematic benchmarking [4], spintronic devices were found to be a promising option with a better energy efficiency. To describe such spintronic device-based circuits, a method has been developed, where 4 × 4 matrices represent various spintronic components [5]–[9]. 4 × 4 matrices relate a four-component current (one charge + three spin) to a four-component voltage. To utilize the potential of spintronics for saving energy in computing, various logic devices have been proposed. Among them, devices involving magnetoelectric (ME) effects, such as magneto-electric spin-orbit (MESO) [10], [11], CoMET [12], ASFOR [13], and SOTFET [14], are expected to operate with a lower energy.

In this work, we build on the previous models of MESO [10], [11], [15]. Here, we replace the approximate compact models by models based on more rigorous physics of switching. Then, we use these device models to construct a few representative circuits. This model development enables a more rigorous and precise analysis of the tight coupling and interplay of multiple nontrivial physics phenomena involved in the MESO operation. Specifically, 4 × 4 matrices derived from the drift-diffusion equations are used to solve the spin-to-charge conversion in the spin-orbit (SO) output of MESO. In the ME input part of MESO, the dynamics of coupled ferroelectric–antiferromagnetic–ferromagnetic (FE–AFM–FM) layers is captured with both the Landau–Lifshitz–Gilbert (LLG) equation and the Landau–Khalatnikov (LK) equation [16], [17]. Meanwhile, since all aspects of the device and circuit are simulated in a SPICE environment [18], convenient design and technology co-optimization (DTCO) is enabled across materials, devices, and circuits.

II. LIMITATIONS OF PRIOR TREATMENT OF SPINTRONIC CIRCUITS

In a recent MESO model update, we proposed to modify the original single-sided MESO device to a differential one [15]. Fig. 1 shows cascading of two differential MESO devices, where a vertical blue plane designates a cross section through the device's SO output part. Compared with the single-sided version, there are two primary changes: 1) both outputs ($+V_{out}/-V_{out}$) of the SO part in the first MESO form a

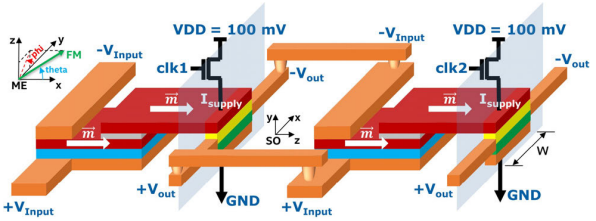

FIGURE 1. **Side view of two cascaded stages of differential MESO. The "slice" through the SO part is shown by a blue vertical plane. +/−V_{in} and +/−V_{out} are two pairs of input–output terminals. Coordinates in two insets.**

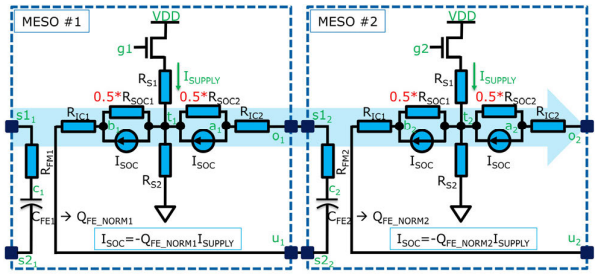

FIGURE 2. **Prior circuit schematic of two cascaded stages of MESO with a differential output and electrically isolated stages [15].**

differential signal and are connected to the top and bottom electrodes (BEs) of the ME capacitor in the second MESO, respectively, and 2) an electrically insulating but magnetically coupling layer (gray) is inserted between the two ferromagnetic (FM) layers (red). These changes brought multiple advantages: 1) enablement of differential input–output signals; 2) prevention of interference between adjacent MESO devices; 3) elimination of footer transistors in each stage; and 4) simplification of clocking control from multiple overlapping clocks to just two non-overlapping clocks.

The equivalent circuit model for two cascaded differential MESO is shown in Fig. 2. With differential inputs/outputs and with an insulating layer, each blue-dash box (MESO #1, for instance) represents an isolated inverter circuit. The branch including nodes $s1_1$-c_1-$s2_1$ (subscript number indicates MESO device number 1 or 2) is the ME input part, where resistance R_{FM} and capacitance C_{FE} are in series. These two elements are used to represent the delay due to switching of the FM layer (top electrode of C_{ME}) and the ferroelectric capacitor (blue layer in Fig. 1). The other branch consists of the vertical path of V_{DD}-t_1-gnd and the differential output loop of t_1-a_1-o_1-u_1-b_1-t_1. R_{S1} and R_{S2} approximate the resistance of the layer stack that the vertical current traverses. In the loop, R_{ISOC} is split into two halves, each with I_{SOC} in parallel. This is done to capture the charge–spin–charge conversion from the vertical path to the loop. The interconnect resistance is modeled by R_{IC1} and R_{IC2}.

While MESO's primary behavior is captured by this simplified model, the delicate dynamics and underlying physics is not properly accounted for. Particularly, the 1-D LK equation was used in the C_{FE} element. This gave a general estimate on FE switching but did not comprehend either the dynamics of the FM and AFM order parameters or their coupling. More importantly, the 3-D nature of the spin–charge interconversion occurs in various layers and material parameters vary across multiple layers in the whole device. The desire to

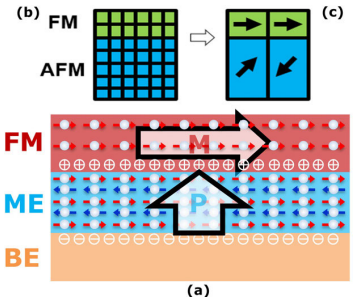

FIGURE 3. **(a) Cross section scheme of the ME input part. The evolution of the model from (b) discretized micromagnetic simulation domain to the (c) macrospin compact model.**

model these effects more rigorously motivated this upgrade utilizing physics-based models.

III. ME COMPACT MODEL

In the ME input part, the top FM layer, the middle ME layer, and the BE layer essentially form a multiferroic capacitor as shown in Fig. 3(a). The switching of this capacitor involves both ferroelectric and magnetic dynamics, and the coupling between them. This switching stage provides the greatest contribution to the delay and thus needs to be treated accurately.

For ferroelectric dynamics, when free charge is accumulated on the FM and BE electrodes, the resulting vertical electrical field E forces polarization P toward pointing in the same direction. In a crystal unit cell of multiferroic BFO, P prefers to point toward vertices of the cubic lattice. Besides, it can switch over a nontrivial two-step trajectory involving a 71° and 109° turning of the polarization state [19]. Therefore, polarization P is not parallel to the electric field E. [Polarization in Fig. 3(a) is shown to be vertical only for simplicity's sake.] This ferroelectric switching can be modeled with the LK equation

$$\gamma_{FE}\frac{\partial \vec{P}}{\partial t} = -\frac{\partial\left(F_{bulk}+F_{elas}+F_{elec}+F_{me}\right)}{\partial \vec{P}} \tag{1}$$

$$F_{me}\left(\vec{P},\vec{M}_i\right) = F_{DMI} = \sum_{i=1}^{n} D_{i,j}\left(\vec{N}\times\vec{M}_c\right) \tag{2}$$

where $\gamma_{FE}, \vec{P}, t, F_{bulk}, F_{elas}, F_{elec}$, and F_{me} stand for the FE damping constant, FE polarization, time, bulk FE energy, FE elastic energy, FE electric energy, and ME coupling energy, respectively [16], [17]. Specifically, the ME coupling energy can be calculated with (2), where $F_{DMI}, i, n, j, D_{i,j}, \vec{N}$, and $\vec{M}_c$ are Dzyaloshinskii–Moriya interaction (DMI) energy [20], [21], index of the lattice cell of interest, number of neighboring lattice cells, index of such cell, DMI constant, Neel vector, and canted magnetization, respectively. Hence, $F_{me}(\vec{P},\vec{M})$ is the coupling path between the ferroelectric order $\vec{P}$ and the antiferromagnetic order. In other words, this set of equations models how the applied electric field changes the FE and AFM orders in the ME layer

$$\frac{d\vec{M}}{dt} = -\gamma\vec{M}\times\vec{H}_{eff} - \frac{\alpha}{M_s}\vec{M}\times\frac{d\vec{M}}{dt} \tag{3}$$

$$F_{ex,int}\left(\vec{M}_{j,AFM},\vec{M}_{i,FM}\right) = J_{ex,int}\frac{\vec{M}_{i,FM}\cdot\left(\vec{M}_{i,FM}-\vec{M}_{j,AFM}\right)}{\Delta_{i,j}^2}. \tag{4}$$

For the magnetic dynamics of the ME part, the FM and ME layers can be meshed and simulated with a micromagnetic

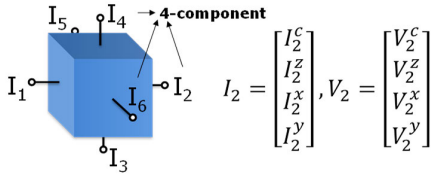

FIGURE 4. Geometry of an SOC module in a MESO device and 4 × 1 vectors for current and voltage of charge and spin. Here, superscript c stands for charge and superscript x/y/z stands for the electron's spin polarized in three orthogonal directions. Subscripts 1, 2, . . . , 6 are index of different facets of the cuboid.

solver as shown in Fig. 3(b)/(c). The governing equation for the magnetic dynamics is the LLG equation without thermal noise (3) [22], where $\vec{M}, t, \gamma, \vec{H}_{\text{eff}}, \alpha,$ and M_s are the magnetization vector, time, gyromagnetic ratio, total effective field, damping constant, and saturation magnetization, respectively. However, conventional micromagnetic simulation takes an excessive amount of time. To accelerate the simulation, the mesh in (b) can be approximately replaced by four macrospins with renormalized values of coupling between them as in (c). Due to the FM and antiferromagnetic exchange coupling within FM and AFM layers, respectively, the top pair of spins are close to parallel, and the bottom pair of spins are close to antiparallel. The antiferromagnetic Neel vector and the canted magnetization can be expressed as follows: $\vec{N} = (\vec{M}_1 - \vec{M}_2)/(|\vec{M}_1| + |\vec{M}_2|)$ and $\vec{M}_c = (\vec{M}_1 + \vec{M}_2)/(|\vec{M}_1| + |\vec{M}_2|)$.

Now the AFM order in the ME layer also interact with the magnetization in the FM layer via the interfacial exchange coupling as expressed by (4), where $F_{\text{ex,int}}, J_{\text{ex,int}}, \vec{m}_{i,\text{FM}}, \vec{m}_{j,\text{AFM}},$ and $\Delta_{i,j}$ are the interfacial exchange energy, interfacial exchange constant, magnetization vector for FM, magnetization vector for AFM, and the spin-to-spin distance, respectively [16], [17]. With the setup above for ME part, the LK equation and LLG equation can be solved together, using material parameters as inputs.

IV. SO EFFECT MODELED WITH 4 × 4 MATRICES

In the exploration of spintronics, various advantageous device options have been proposed. Consequently, the question arises of how to simulate them in a unified framework. To address this, the charge-and-spin transport problem has been reformulated in terms of 4 × 4 matrices with magnetic dynamics included [6]–[8]. The elements common to various spintronics devices have been formulated and built into a set of representative modules. Hence, modeling a specific spintronics device is reduced to constructing a circuit from these modules. This was termed the "modular approach to spintronics"

$$\begin{bmatrix} I^c \\ I^z \\ I^x \\ I^y \end{bmatrix} = G^E \begin{bmatrix} V^c \\ V^z \\ V^x \\ V^y \end{bmatrix} = \begin{bmatrix} G^{cc} & G^{cz} & G^{cx} & G^{cy} \\ G^{zc} & G^{zz} & 0 & 0 \\ G^{xc} & 0 & G^{xx} & 0 \\ G^{yc} & 0 & 0 & G^{yy} \end{bmatrix} \begin{bmatrix} V^c \\ V^z \\ V^x \\ V^y \end{bmatrix} \quad (5)$$

Here, the modular approach is applied to the SO output part of a MESO device. The primary physical effects are the drift-diffusion and interconversion of charge and spin currents. Fig. 4 illustrates a module for a cuboid piece of a spin-orbit-coupling (SOC) layer, which is key for the SO

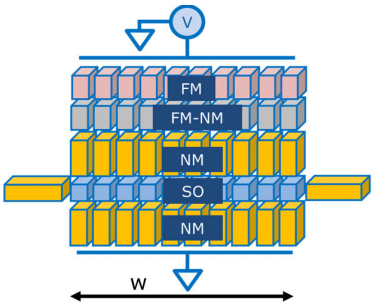

FIGURE 5. Scheme for discretization of a "slice" through the SO part into a mesh of cuboids with different categories. From top to bottom, there are layers of FM, ferromagnetic–nonmagnetic (FM–NM), nonmagnetic (NM) top, SO and NM bottom. Differential outputs use two NM modules as interconnection.

part of the device. To consider both charge and spin, the scalar of current and voltage at each port of a regular circuit model are represented by a 4 × 1 vector. The superscripts of c, x, y, and z stand for charge and three projections of spin on the respective axes. The subscripts of $1, 2, \ldots, 6$ are the indexes of cuboid facets. Hence, the overall current or voltage vector will have 24 elements, and a 24 × 24 tensor matrix is used to represent the conductance and dissipation of this cuboid. The generalized form of the SOC conversion is rederived from model 3 of [23]. The matrix form is shown in (5), where $I^\eta = (I_1^\eta, I_2^\eta, \ldots, I_6^\eta)^T$, $V^\eta = (V_1^\eta, V_2^\eta, \ldots, V_6^\eta)^T$ with $\eta = c, z, x, y$. Each element in the 4 × 4 matrix of (5) is also a 6 × 6 sub-matrix. Therefore, the 4 × 1 vector and the 4 × 4 matrix of (5) are replaced by a 24 × 1 vector and a 24 × 24 matrix. The elements of the 24 × 24 matrix are functions of the cuboid geometry, conductivity, spin diffusion length, and spin Hall angle. Despite the ongoing discussion on the reciprocity of the forward/inverse SOC effect and the equivalence of spin Hall effect in the bulk to the Rashba–Edelstein effect at an interface [24], [25], these physics behaviors are treated with the same SOC module here. Despite their different microscopic origin, the phenomenological model considered here can be calibrated by experiment to capture these different effects.

Similar approaches have been applied to other functional modules, like FM module, ferromagnetic–nonmagnetic (FM–NM) interface module, and nonmagnetic (NM) module [8]. To account for the magnetization dynamics, terminals for magnetization orientation angles have been built for the FM module as well.

Once these modules are prepared, we take a vertical "slice" of the SO part, discretize it, and map each cuboid to a corresponding module as shown in Fig. 5. Specifically, we have FM, FM–NM, NM, SO, and NM layers from top to bottom. Additional NM modules are placed on the left and right sides of SO to represent an interconnecting wire. By varying the mesh size, one can account for the non-uniformity of quantities with varying granularity. The spin polarization in the SO part is strongly linked to the FM magnetization obtained from the ME part. During the operation of the SO slice, spin unpolarized free charge carriers (i.e., electrons with equal amount of spins up and down) could flow from the top and first traverse the FM layer. The FM forces the majority of magnetic moments (proportional to spins) of free carriers to align to the magnetization. In other words,

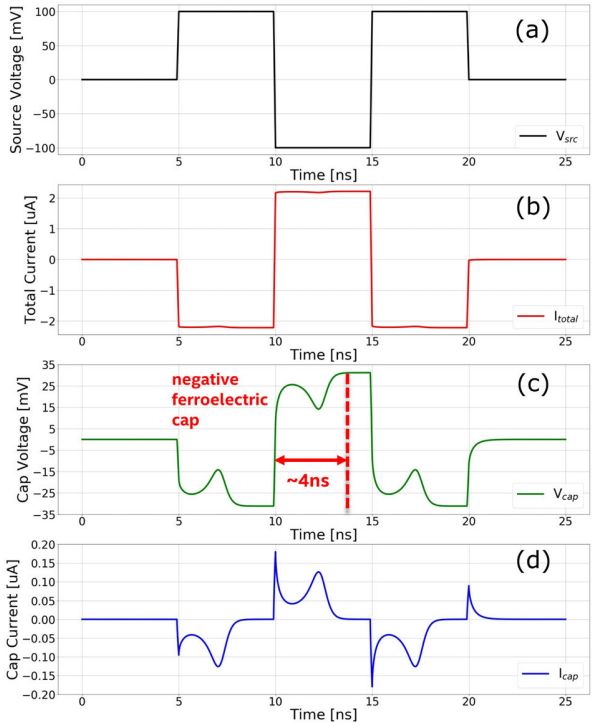

FIGURE 6. Time evolution of (a) supply driving voltage, (b) driving current in the SO part, (c) voltage at the ME capacitor, and (d) current to the capacitor.

spin polarization of electrons injected from FM depends on the magnetization of the FM layer. Next, the partially polarized spin current encounters the FM–NM interface, where interface resistance may do additional spin filtering [26]. The charge current is conserved in the following NM layer, while its spin polarization will decrease according to the spin flip length within it. Eventually, the spin-polarized current flows into the SO layer, which implements the spin-to-charge conversion. In the conductance matrix in (5), the diagonal elements stand for the intrinsic conductance for charge and for electron spins. The off-diagonal elements stand for the interaction of spin and charge. In the SO layer, most of the vertical spin current is expected to be converted to a horizontal charge current flowing toward the differential interconnects. As a result, the charge current is generated to drive the ME part of the next MESO logic stage. The carriers which did not experience scattering in the SO layer continue flowing vertically through the bottom NM layer to the ground.

By mapping the SO (slice) part into spintronics modules, this model can relate the material parameters to the input–output voltage/current, and the magnetization values. With this modular numerical modeling procedure, the spin-charge-coupled drift-diffusion equations are solved along with the magnetic dynamics.

V. DYNAMICS OF COMBINED ME AND SO PARTS

Using the above model, the initial MESO circuit simulations examined how an SO slice switches the ME capacitor.

To drive the SO slice, the top charge terminal is connected to an ideal voltage source $V_{\rm src}$ with a variable polarity. Its amplitude is 100 mV, pulsewidth is 5 ns, and the rise/fall time is 0.1 ns as in Fig. 6(a). In graph (b), the vertical charge current, $I_{\rm total}$, flows between $V_{\rm src}$ and gnd, and its amplitude

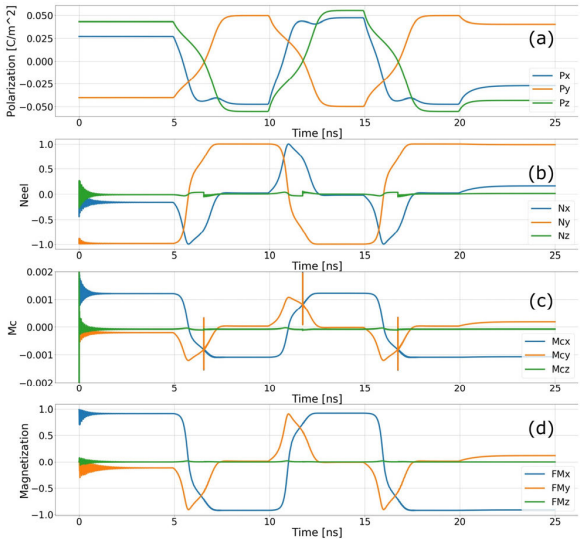

FIGURE 7. Time evolution of (a) ferroelectric polarization, (b) antiferromagnetic Neel vector, (c) canted magnetization, and (d) magnetization in the FM electrode in the ME layer. Each variable is a vector and projected onto *x*-/*y*-/*z*-directions.

is $\sim$2.2 μA. Graph (c) shows the charge voltage $V_{\rm cap}$ across the ME capacitor electrodes. Each time $V_{\rm src}$ changes polarity, the resulting $V_{\rm cap}$ will switch its polarity as well. During each transient ramp up/down, the absolute value of $V_{\rm cap}$ would increase, decrease, and increase again to saturation. This is caused by the transient negative capacitance [27]. The saturation level of $V_{\rm cap}$ is $\sim$31 mV, which is above the assumed coercive voltage $\sim$20 mV in the ME material. This $V_{\rm cap}$ saturation level is essentially determined by the product of $I_{\rm soc}$ and $R_{\rm soc}$, which stands for inverse SOC current and SO lateral equivalent resistance. It takes about 4 ns for $V_{\rm cap}$ to saturate. The varying charge current through the ME capacitor, $I_{\rm cap}$, is shown in Fig. 6(d). The nonlinear behavior also stems from the transient characteristics of ferroelectric switching. Once $V_{\rm cap}$ saturates, $I_{\rm cap}$ reduces to zero, which means the charging of capacitor is complete. The peak amplitude of $I_{\rm cap}$ is $\sim$0.2 μA, provided that the inverse SOC current conversion efficiency is $\sim$10%.

In Fig. 7, the time evolution of FE polarization in the ME, the AFM Neel vector in the ME, the canted magnetization M_c in the ME, and the FM magnetization are shown. In graph (a), the polarization switches between two opposite orientations, $+x-y+z$ and $-x+y-z$. This is because the polarization is pointing from the center of a cube to one of its vertices in the crystal lattice cell. Each time when $V_{\rm src}$ and $V_{\rm cap}$ switch polarities, the FE polarization changes its sign if $V_{\rm cap}$ exceeds the FE coercivity. In graph (b), the AFM order simultaneously follows the polarization, which makes the Neel vector to alternate between positive and negative y-directions, which is the in-plane easy axis. In graph (c), the canted magnetization M_c switches between positive and negative x-directions, which is the in-plane easy axis. In graph (d), with the coupling to M_c, the FM magnetization aligns in the same direction. Hence, the main projection of FM is on the x-axis.

With this combined ME–SO simulator, various parameter dependencies can be explored. In the following, we present one example where the width of the SO slice is varied to

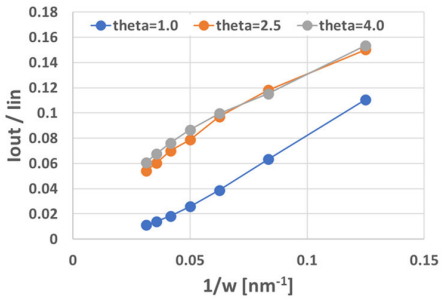

FIGURE 8. Dependence of the ratio of the output current to the input current on the SO slice width at various values of the spin Hall coefficient.

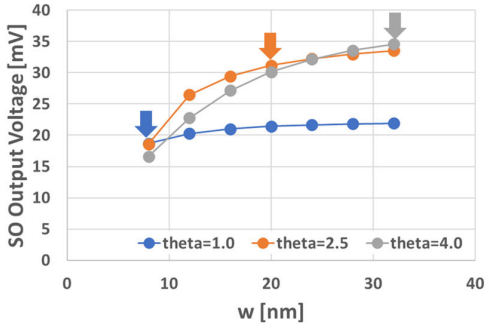

FIGURE 9. Dependence of the output voltage from the SO part on the magnet width at various values of the spin Hall coefficient.

understand its scaling behavior. In the setup of Figs. 6 and 7, the width of the SO slice per one output wire, w, is 20 nm (2 nm $\times$ ten columns as in Fig. 5). By tuning the number of cube columns in the SO slice and repeating the same simulation, a series of results was generated. The ratio of I_{cap} and I_{total} (also the I_{out} and I_{in}) of the SO slice has been obtained and plotted versus $1/w$. Using the spin Hall angle, Θ, of 1.0, 2.5, and 4.0, similar curves were obtained and plotted in Fig. 8. The simulation results show that current conversion efficiency of the SO slice, $I_{\text{out}}/I_{\text{in}}$, has a quasi-linear dependence on $1/w$. In other words, with narrower w of the SO slice, a higher $I_{\text{out}}/I_{\text{in}}$ leads to more output current and makes the ME capacitor able to be charged faster with the same current from power supply. This would continue to be beneficial with further scaling down of the SO width. Comparison of different Θ values also confirms that the current conversion efficiency is higher for larger Θ.

Similarly, the maximum of V_{cap} absolute value is obtained as a function of w as shown in Fig. 9. At smaller w, V_{cap} decreases too, which is mainly caused by the decrease of the internal resistance of the current source R_{ISOC}. This behavior is more obvious for the case with a larger spin Hall angle. To ensure the normal functionality of the MESO device/circuit, the absolute value of V_{cap} needs to be larger than the coercive voltage of the ME material. To address this requirement, when w of SO further scales down, either the decrease in the output voltage needs to be compensated by another factor, or the ME input coercive voltage needs to be decreased by the material optimization. Comparing curves at different Θ values, we notice that the saturation level of V_{cap} increases with larger Θ, but this increase also gradually saturates. At different w values (labeled by down arrows),

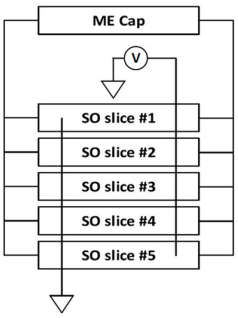

FIGURE 10. Circuit schematic of the 3-D structure in the SO part via parallel vertical "slices." The top/BEs of all SO slices are merged and connected to the power supply and to ground, respectively.

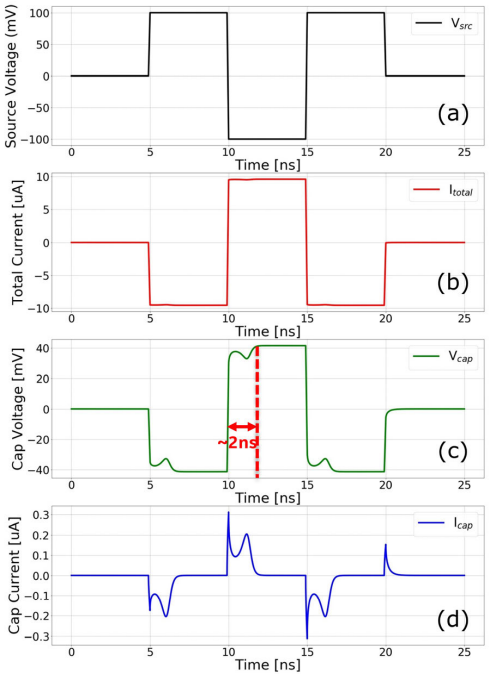

FIGURE 11. Five SO slices driving the ME capacitor. Time evolution of (a) power supply VDD, (b) power supply current, (c) voltage across ME capacitor, and (d) charging current for ME.

the optimal Θ for higher V_{cap} is different. This suggests that the spin Hall effect optimization should go hand in hand with the device scaling: at relatively large w, higher Θ is preferred; while for smaller w, Θ requirement would be relaxed.

VI. 3-D EFFECT IN THE SO PART

So far, an individual MESO device was modeled with the complete ME part and a single SO slice. Further study suggests that there are nonzero charge/spin currents in the direction perpendicular to the output wires. Hence, a full model, where SO part comprises multiple SO slices in parallel, becomes necessary to handle the 3-D nature of SO effects as in Fig. 10.

Fig. 11 shows the simulation results for five SO slices used to switch the ME part. The corresponding terminals of five SO slices are merged to form a full SO output. The same ideal voltage source as in Section V is used for the driving force. In graph (a), the voltage waveform has the same amplitude

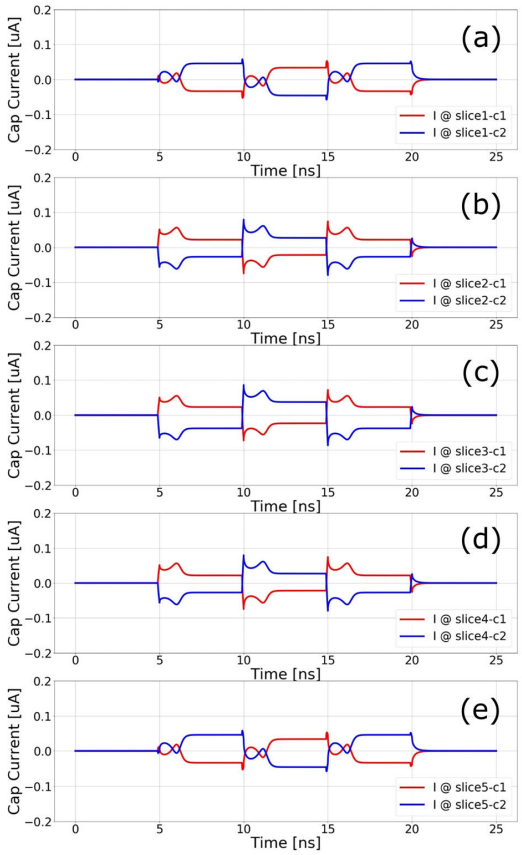

FIGURE 12. **Time evolution of lateral charge current flowing into/out of the differential output terminals for each SO slice.**

of 100 mV and 5-ns pulsewidth. In graph (b), the amplitude of current from power supply has increased from 2.2 μA (in the one slice case) to $\sim$9 μA (in the five-slice case). This is mainly because more SO slices in parallel reduce the resistance between the power supply and the ground. In graph (c), V_{cap} across the ME capacitor shows similar behavior as before. But there are two interesting changes. One is that the saturation level of V_{cap} increases from 31 mV before, in Section V, to 40 mV now. This indicates that the multi-slice interaction leads to increase of SOC output voltage. Intuitively, when the spin current is injected into the SO layer, the inverse SO effect creates charge currents toward all surfaces of the SO layer: not just left and right, but also the front and back surfaces. This results in the potential differences between these surfaces. Modeling more SO slices allows us to capture these 3-D effects.

The other change is the time it takes for V_{cap} to saturate, which is mainly attributed to differences in I_{cap}. In graph (d), we see that the charging current, I_{cap}, also increases with more SO slices included. As a result, charging the ME capacitor takes a shorter time $\sim$2 ns instead of $\sim$4 ns with a single SO slice.

Fig. 12 shows the lateral currents flowing into/out of the differential output of each SO slice in the 3-D MESO model. Each graph corresponds to one SO slice, and the two curves are measured on each of the output charge terminals. Hence, in each graph, the two curves have the same amplitude and opposite signs. It can also be noticed that the currents in

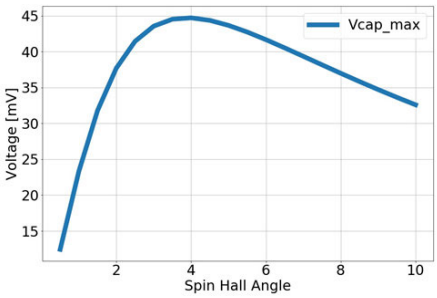

FIGURE 13. **SO part differential output voltage as a function of the spin Hall angle (Θ) in SO layer.**

these five SO slices are not identical. Slices show symmetric behaviors with respect to the central slice. For instance, the slice (a) is similar to (e), and slice (b) is similar to (d). To validate that this is caused by the inter-slice interaction, the slice-to-slice interconnections were cut off in a control simulation (not shown here), which made each slice reduce to having the same behavioral state.

The full 3-D MESO model, sensitivity study of several parameters is enabled. Here, we revisit the dependence on a major factor, spin Hall angle (Θ). As shown in Fig. 13, Θ is swept from 0.5 to 10 [28]. For each Θ value, similar switching simulation was done to extract the maximal SO output voltage or V_{cap}. Previously, this V_{cap} was expected to increase with larger Θ. In contrast, the simulation results show a surprising non-monotonic trend, where V_{cap} versus Θ first increases, then saturates, and finally decreases. The optimal Θ value is $\sim$4 and as shown in the earlier discussion, it varies with both geometric and material parameters. In the simplified SO "model 1" of [23], the open-circuit charge voltage for the inverse spin Hall effect can be described by (6). The $V_{\text{so}}, \theta, \sigma, t, \lambda,$ and I_3^z are the charge output voltage, spin Hall angle, conductivity, thickness, diffusion length, and injected spin current into the SO layer, respectively. In (6), Θ is present in the numerator and its second power is in the denominator as well. The general explanation for this behavior is that once spin current is injected vertically, the left/right surface would have a charge voltage built up. This accumulated charge voltage would inversely create an opposite vertical spin current to resist the injected spin current. As a result, the net injected spin current would be lower, and the output voltage would reduce as well

$$V_{\text{so}} = \left(V_1^c - V_2^c\right)\big|_{I_1^c = I_2^c = 0} = \frac{\theta}{2\sigma\theta^2 + \sigma\frac{t}{\lambda}\coth\frac{t}{2\lambda}}\frac{I_3^z}{w}. \quad (6)$$

VII. MESO CIRCUIT SYMBOL

We proceed analyzing MESO circuits using the 3-D physics-based compact models of MESO as elements in larger circuits. The models of the ME part and the SO part that were used in Sections I–VI are wrapped into the circuit symbols as shown in Fig. 14. These ME and SO symbols are connected via the pins "theta" and "phi" to transmit the values of the magnetization orientation angles. For the ME part, the differential input nodes, n1 and n2, are the top and BEs of the ME capacitor. The SO symbol provides the charge and spin *c*/*z*/*x*/*y* pins from left, right, top, and right surfaces. The spin-related terminals are grounded,

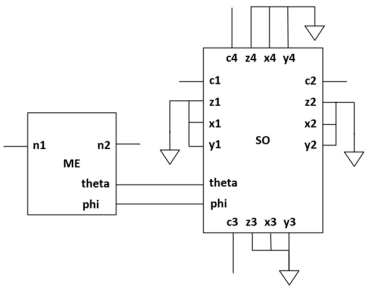

FIGURE 14. Circuit schematic of the ME part and SO part within the MESO 3-D device symbol.

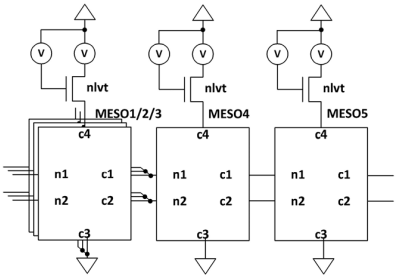

FIGURE 15. Circuit schematic of a three-input MESO majority gate. Each of MESO #1/2/3 is power gated by a transistor (not drawn for simplicity).

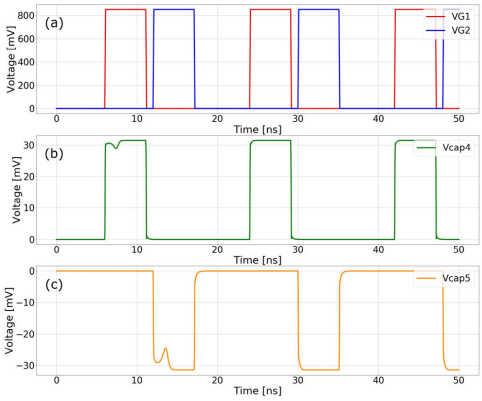

FIGURE 16. Time evolution of (a) clock signals and (b) and (c) V_{cap} voltage for three-input MESO majority gate.

and the charge terminals can connect to other charge-based components.

VIII. MESO MAJORITY GATE

A primary circuit that MESO can implement efficiently is the majority gate. Instead of using more than ten CMOS transistors to implement a three-input majority gate, MESO logic only needs one MESO device with one NMOS transistor. In addition, with the single MESO device as inverting logic, the majority gate would form a complete logic family and enable the design of any arbitrary circuit logic function.

In Fig. 15, MESO symbols are used to construct such a three-input majority gate. The three-input state driving MESO #1, 2, and 3 devices have their $c1$ and $c2$ terminals merged, respectively. The merged $c1$ and $c2$ then connect to the middle MESO #4, which serves as a minority gate function. Using MESO #5 as the load and an inverter as well, the minority gate is converted back into the majority gate.

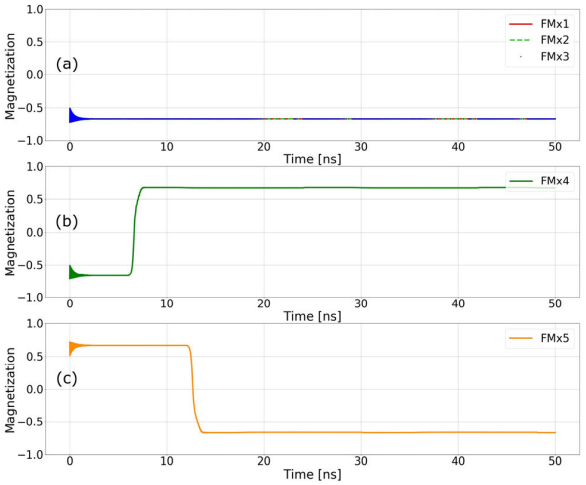

FIGURE 17. Time evolution of the FM layer magnetization projected along in-plane easy-axis direction in each MESO device of three-input majority gate. (a) MESO#1/2/3. (b) MESO#4. (c) MESO#5.

The input n1/n2 terminals of the three-input state driving MESO devices are floating as the ME capacitor maintains its state. The output $c1/c2$ of MESO #5 are floating as the ME input is isolated from the SO output. To control this majority gate, two non-overlapping clock signals are needed, where the first clock controls MESO #1, 2, and 3 and the second clock controls #4. For MESO #5, the power gating transistor and voltage sources are plotted for consistency but are not necessary for the operation.

In Fig. 16, a case with specific initial conditions is shown as an example. In graph (a), the VG1 and VG2 are two non-overlapping clock signals applied to MESO #1, 2, 3, and #4, respectively. The amplitude is 0.85 V and the pulsewidth is 5 ns. Delay from VG1 to VG2 is 6 ns and rise/fall time is 0.1 ns. When VG1 becomes high, the MESO #1, 2, and 3 will be enabled and generate a nonzero voltage V_{cap4} at the terminals $n1/n2$ of MESO #4. The voltage is shown in graph (b), with an amplitude of 31 mV and pulsewidth of 5 ns. This voltage will update the ME capacitor state in MESO #4. When VG2 becomes high, only MESO #4 is enabled, which generates a nonzero V_{cap5} across $n1/n2$ of MESO #5 as shown in graph (c). This voltage will update the ME capacitor state in MESO #5 and complete the majority gate function. When the first pulses of VG1/VG2 are on, V_{cap4} and V_{cap5} show transient characteristics of negative capacitance, which is the signature of the ME capacitor switching. For the following VG1/VG2 pulses, despite the nonzero V_{cap4} and V_{cap5}, the switching is not shown and the already switched ME capacitors are just saturated and relaxed again each cycle.

In Fig. 17, the corresponding magnetization projection, FMx, along the in-plane easy-axis direction is plotted versus simulation time for each of the MESO stages. In this case, the MESO #1, 2, 3, 4, and 5 have been initialized as -1, -1, -1, -1, and $+1$, respectively. -1 or $+1$ refers to the sign of the FMx. Throughout the procedure, the MESO #1/2/3 state remain the same as graph (a). Since three-input MESO #1, 2, and 3 are all -1, their minority state is $+1$. Hence, MESO #4 is driven to switch from initial -1 state to this

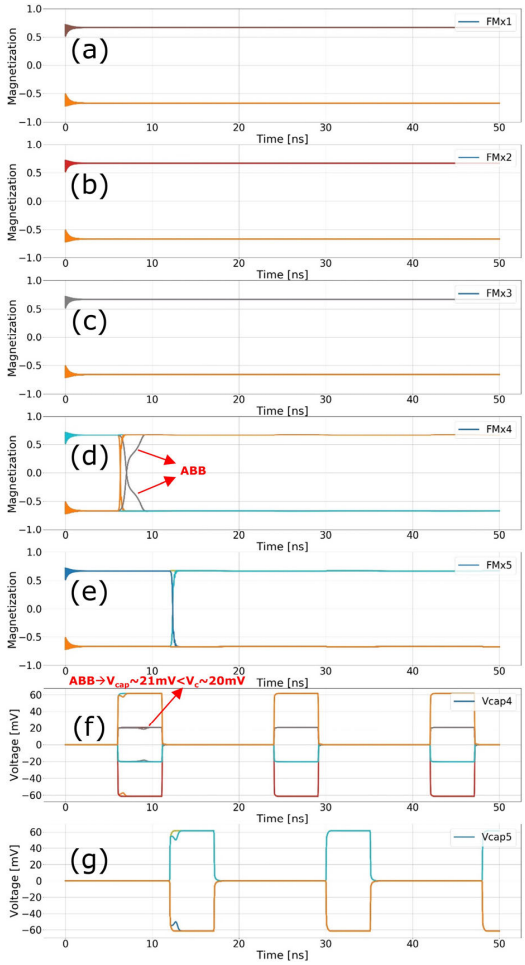

FIGURE 18. Time evolution of magnetization along in-plane easy-axis direction for (a)–(e) MESO #1-5 and (f)–(g) V_{cap} of MESO #4/5 in a three-input majority gate for all $2^5 = 32$ initial conditions. The power supply voltage is increased to 200 mV and all the cases are functional.

minority state +1 at around 6 ns. This realizes the minority-gate function. As shown in the MESO ring oscillator section (in the supplementary material), each MESO stage can serve as an inverter. Since MESO #4 switches to +1 state, MESO #5 would further invert from +1 to −1 state. The −1 state in MESO #5 is essentially the majority state of the MESO #1, 2, and 3.

This provides the initial demonstration for three-input majority gate with the physics-based MESO model. To exhaustively validate the three-input MESO majority gate, the cases with different initial conditions have been simulated and results were postprocessed with a Python script. For five MESO devices, there are $2^5 = 32$ possible initial conditions. The magnetization projection of MESO devices #1 to #5 and V_{cap} for MESO #4 and #5 versus time, were simulated. All the magnetization for the input MESO devices #1 to #3 remain unchanged throughout the simulation. For MESO #4, some cases switch, but several cases turn out to have incomplete switching. By checking V_{cap} of MESO #4, it is found that the V_{cap} absolute value for these half-switched cases are ∼10 mV. Since the ME capacitor has a coercive voltage of 20 mV, the switching cannot occur. Meanwhile, one aspect in common for these unswitched cases is that the input MESO stages have "ABB" combinations, such as +1/−1/−1, or +1/−1/+1 and so on. We further find that the current between the converged joint nodes $c1/c2$ makes the SO output voltage lower than that of an individual MESO driving device. Like the MESO behavior in [15] circuit study, a larger number of inputs is expected to cause more reduction of voltage at the differential output.

To solve this issue of a smaller input signal, especially for a larger fan-in majority gate, and to ensure that this majority gate can operate with various initial conditions, the power supply VDD was increased from 100 to 200 mV. As shown in Fig. 18, with higher VDD, all the cases with different initial conditions can switch MESO #4 and MESO #5 completely as in graphs (d) and (e). For MESO #4, some cases still show a longer switching time, which is also caused by an "ABB" input combination and shrinkage of V_{cap}. From V_{cap} of MESO #4 and #5 in Fig. 18(f) and (g), it can be noticed that the saturation level of voltage still has two groups, which are around 50+ and 20+ mV, respectively. The 20+ mV V_{cap} cases are also the ones with "ABB" input combinations. However, by increasing VDD, all the logic functionalities for this three-input majority gate are realized and validated.

In larger-scale realistic designs and realistic tape out, the reduction of V_{cap} signal with more inputs to the majority gate is indeed a critical factor to consider. With the device and process variations, this needs more signal margin to account for tolerances. While the issue here is roughly solved by an increase of the supply voltage, it costs more energy consumption. More importantly, it indicates that more optimization of materials for both the ME part and the SO part is necessary. For the SO part, better spin–charge conversion efficiency needs to be explored to enhance both output voltage and current levels. For the ME part, lower coercive voltage and coherent switching is critical for normal logic function and lower energy switching.

IX. CONCLUSION–INSIGHTS INTO MESO OPERATION FROM SIMULATIONS

In this work, a multiphysics-based model is built for the MESO logic device. The FE/AFM/FM material systems are seamlessly integrated and simulated in the SPICE circuit simulation environment. This closes the gap between the material, device, and circuit simulation. With this methodology, the design space could be explored to better understand the MESO behavior, such as geometric scaling, 3-D nonuniform spin-to-charge conversion, as well as the non-monotonic dependence on spin Hall angle. The synchronous ring oscillator and the majority gate circuits are designed and validated by simulation. The strong correlation between the device parameter metrics and circuit behavior can be observed, which will guide future optimization.

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