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Power Performance Analysis of Digital Standard Cells for 28 nm Bulk CMOS at Cryogenic Temperature Using BSIM Models

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ABSTRACT Cryogenic CMOS is a crucial component in building scalable quantum computers, predominantly for interface and control circuitry. Further, high-performance computing can also benefit from cryogenic boosters. This necessitates an in-depth understanding of the power and performance trade-offs in the cryogenic operation of digital logic. In this article, we analyze digital standard cells in a 28 nm high-k metal gate (HKMG) CMOS foundry process design kit (PDK). We have developed Berkeley Short-channel IGFET Model (BSIM)4 of cryogenic CMOS and calibrated them with experimental measurements. Since low-temperature operation leads to an exponential decrease in the leakage current of the transistors, we further tune the threshold voltage of the devices to achieve iso-leakage. In this article, we present inverter static and dynamic characteristics and multiple ring oscillator (RO) structures. The simulation study shows that we can achieve 28% (FO4-RO) – 59% (NAND3-RO) higher performance under iso-V_{DD} scenario and up to 90% improvement in the energy-delay product (EDP) under iso-overdrive scenario at 6 K compared to room temperature.

INDEX TERMS Berkeley Short-channel IGFET Model (BSIM)4, cryogenic CMOS (Cryo-CMOS), ring oscillators (ROs), standard cells, static characteristics, threshold voltage, transient analysis.

I. INTRODUCTION

CRYOGENIC CMOS (Cryo-CMOS) plays a key role in several applications like space electronics, astronomical detectors, metrology, high-performance computing, and interface circuits to quantum computers [1]–[7]. The qubits operate in the deep cryogenic regimes of the order of a few millikelvin. This operating temperature is dictated by both the implementation requirements of qubits (for ion traps, superconducting, spin, etc.) as well as reliability in terms of fidelity. A feasible solution for building a scalable quantum computer with a reasonable number of interconnects is to place the control electronics and memory circuits closer to the qubits at around 4 K rather than at room temperature [8] which will require digital, analog, and RF circuits to operate at low temperatures. CMOS is one of the more reliable technologies that can provide an integrable solution with a higher number of qubits and operate at cryogenic temperature.

With remarkable improvement in the device behavior including ultralow leakage current, higher ON-current, near-ideal subthreshold swing, lower thermal noise, and lower device and interconnect resistance [22], Cryo-CMOS has shown promising results for achieving higher performance and/or obtaining better power efficiency [2], [15]. The design requires well-calibrated transistor models for low-temperature operation that can be used for circuit-level simulations. There have been quite a few attempts to model the behavior of CMOS at low temperatures including but not limited to physics-based semi-empirical models,

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simplified-EKV models, virtual source (VS) models, and so on [9]–[13], [23]–[26]. There is a need for a physics-based, accurate, scalable, and robust MOSFET Berkeley Short-channel IGFET Model (BSIM) compatible model for circuit simulation and technology assessment. Some of the recent publications [16]–[20] demonstrate similar modeling but the devices are on matured technology nodes (e.g., 180 nm).

In this article, we introduce a BSIM4 MOSFET model compatible with cryogenic temperature for more recent 28 nm bulk HKMG CMOS. The key transistor parameters are tuned to accurately model the device characteristics. The models are temperature-dependent meaning the parameters are tuned for each temperature point in order to account for the varying device characteristics across the wide temperature range of 6–300 K. The models are used to tune the transistor's threshold voltage to obtain iso-leakage at all the operating temperatures. The tuned BSIM4 models are then used to analyze the power and performance of digital standard cells with an emphasis on CMOS inverters and a family of ring oscillators (ROs).

The remainder of the article is organized as follows. In Section II, we examine some of the key transistor properties at low temperatures and briefly describe the BSIM4 modeling methodology. In Section III, we analyze the performance and power metrics of digital standard cells followed by conclusions.

II. DEVICE CHARACTERISTICS AT CRYOGENIC TEMPERATURES

The transistor device I_{ds}–V_{gs} and I_{ds}–V_{ds} for 28 nm gate first based high-k metal gate (HKMG) bulk Si NMOS and SiGe PMOS from Global Foundries [27] are measured on a Lakeshore CPX-VF cryogen-free cryogenic probe station from 300 to 4 K. The devices have chemical oxide-based gate oxide (interlayer and hafnium oxide-based high-k) and an equivalent oxide thickness (EOT) of 1.25 nm. The device output characteristics for iso-overdrive voltage ($V_{ov} = |V_{gs}| - |V_{th}|$) of 0.5 V is shown in Fig. 1(a). We choose the iso-overdrive scenario because with a decrease in temperature, the threshold voltage of the devices increases, in order to provide a correct comparison of increase in current, it would be accurate to model the amount of charge accumulated after the device turns ON ($|V_{gs}| > |V_{th}|$) by a constant headroom (we choose a headroom or overdrive of 0.5 V). The device transfer characteristics are shown for the linear region [see Fig. 1(b)] defined by $|V_{ds}| = 50$ mV and saturation region [see Fig. 1(c)] defined by $|V_{ds}| = 1$ V. All the curves indicate an increase in the device ON current from 300 to 4 K. As evidenced by the output characteristics, there is no kink effect for bulk 28 nm CMOS. We also notice that the slope of the transfer characteristics becomes steeper with a decrease in temperature and the device OFF current decreases exponentially [notice the log scale of Fig. 1(b) and (c)]. This means the subthreshold swing of devices decreases linearly with temperature proving more ideal ON–OFF characteristics.

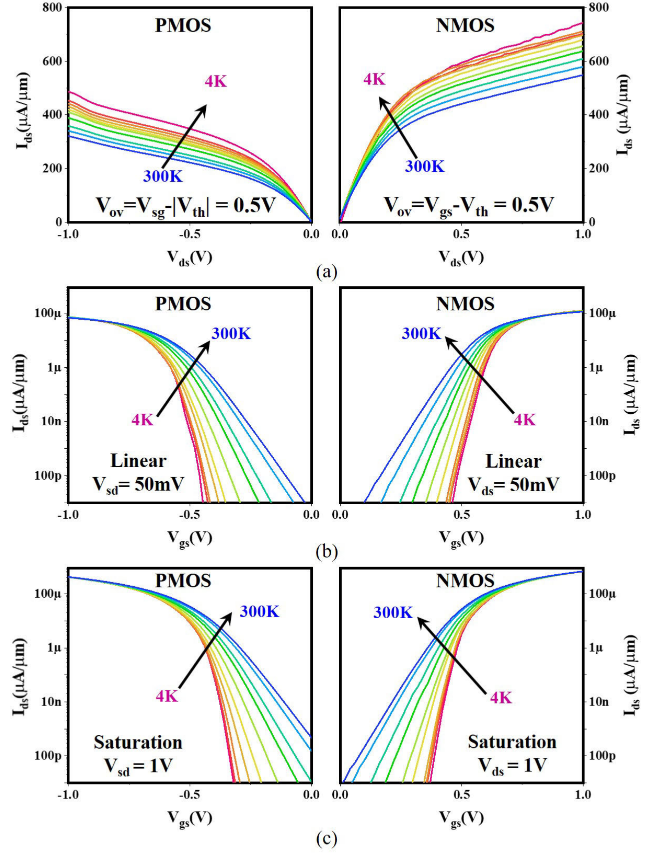

FIGURE 1. Measured device characteristics across temperature showing (a) transistor output characteristics for iso-overdrive of 0.5 V, (b) transistor transfer characteristics in linear region defined by $V_{ds} = 50$ mV (NMOS) and $V_{sd} = 50$ mV (PMOS), and (c) transistor transfer characteristics in saturation region defined by $V_{ds} = 1$ V (NMOS) and $V_{sd} = 1$ V (PMOS).

III. DEVICE MODELING AT CRYOGENIC TEMPERATURE

We use the industry-standard tool BSIMProPlus[1] to calibrate BSIM4 model parameters to the measured data and analyze the fit parameters. The parameters are individually fit five key temperature points (300, 150, 70, 30, and 6 K) so as to obtain a lower error percentage. We tune a minimal number of crucial parameters like V_{th0}, V_{SAT}, U0, K1, ETA0, DSUB, CIT, and RDSW that control the device behavior. Fig. 2 shows the flow of parameter tuning at a given temperature.

A. THRESHOLD VOLTAGE

The increase in the silicon (Si) bandgap along with exponential scaling of Fermi–Dirac occupation function decreases in intrinsic carrier concentration causing increased bulk Fermi potential and incomplete ionization all collectively, which causes the threshold voltage of the MOSFET to increase with a decrease in temperature [21]. In BSIM4, the temperature

[1] Trademarked.

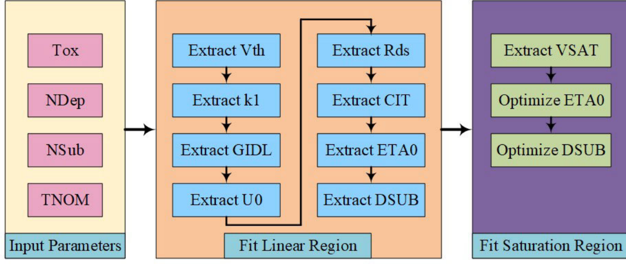

FIGURE 2. Flow diagram for parameter tuning at each temperature point.

dependence of threshold voltage is modeled by

$$V_{\text{th}}(T) = V_{\text{th0}}(\text{TNOM}) + \left(\text{KT1} + \frac{\text{KT1L}}{L_{\text{eff}}} + \text{KT2}\cdot V_{\text{bseff}}\right)\left(\frac{T}{\text{TNOM}} - 1\right). \quad (1)$$

KT1 is the dominant parameter to describe the temperature dependence of V_{th}, KT1L improves the fitting for various channel length sizes, and KT2 models the temperature dependence of the body effect on V_{th0}. In our case, since we are fitting for a constant channel length and not studying the body effect, we retain the default values for KTL1 and KTL2 parameters. The final fit V_{th} is shown in Fig. 3(a) and shows approximately 100 mV shift from 300 to 6 K.

B. MOBILITY AND VELOCITY SATURATION

The mobility of the charge carriers is degraded by the vertical electric fields in scaled nodes and at higher gate voltages, which is further degraded by the phonon/surface roughness and Coulomb scattering. However, at lower temperatures, due to lower lattice vibrations, the phonon scattering largely reduces. On the other hand, the surface roughness under strong transverse electric field increases with a decrease in temperature as low-temperature electrons have lesser kinetic energy making them more vulnerable to surface roughness scattering.

Coulomb scattering due to bulk charge increases with a decrease in temperature since the interaction time between the fast-moving channel carriers and ionized impurity centers becomes longer but is reduced at higher electric fields due to the screening effect. Conversely, Coulomb scattering due to interface charges, though higher, gets masked by the reduced screening effect causing mobility due to Coulomb scattering from interface charge show inverse proportionality to temperature. These phenomena have been captured in the recent modifications to BSIM models [18] and the final effective mobility is given by

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + U_A E_v^{E_U} + \frac{U_D}{\left[\frac{1}{2}\left(1+\frac{U_{\text{DS}}q_s + U_{\text{DD}}q_d}{q_0}\right)\right]^{U_{\text{CS}}}}} \quad (2)$$

where q_s and q_d are normalized source- and drain-side inversion charge densities, q_0 is a temperature-independent constant, E_v is the effective vertical electric field, μ_0, U_A, U_D, U_{CS}, U_{DS}, and U_{DD} are temperature-dependent mobility coefficients, all following linear temperature-dependent power law as:

$$\mu_0(T) = \mu_0(T_{\text{nom}})(T_r)^{U_{01}+U_{02}T_r} \quad (2a)$$
$$U_A(T) = U_A(T_{\text{nom}})(T_r)^{U_{A1}+U_{A2}T_r} \quad (2b)$$
$$U_D(T) = U_D(T_{\text{nom}})(T_r)^{U_{D1}+U_{D2}T_r} \quad (2c)$$
$$U_{\text{CS}}(T) = U_{\text{CS}}(T_{\text{nom}})(T_r)^{U_{\text{CS1}}+U_{\text{CS2}}T_r} \quad (2d)$$

and E_U is the slope of μ_{eff} versus E_v

$$E_U(T) = E_U(T_{\text{nom}}) + E_{U1}(T_r - 1) \quad (2e)$$

U_{01}, U_{02}, U_{A1}, U_{A2}, U_{D1}, U_{D2}, U_{CS1}, U_{CS2}, and E_{U1} are all temperature-independent parameters. In this work, we capture the effects by fitting U_0, and the normalized U_0 as a function of temperature is shown in Fig. 3(b).

A cubic polynomial temperature dependence model of velocity saturation parameter V_{SAT} proposed in [18] to fit the nonlinear data has been used here. The variation of V_{SAT} with temperature is shown in Fig. 3(c)

$$V_{\text{SAT}}(T) = V_{\text{SAT}}(\text{TNOM}) + A_T\Delta T + A_{T1}\Delta T^2 + A_{T2}\Delta T^3 \quad (3)$$

C. SUBTHRESHOLD SLOPE AND DRAIN INDUCED BARRIER LOWERING

The exponential dependence of I_D on temperature seen in (4) causes the subthreshold slope to become steeper with decreasing temperature. I_0 is the saturation current, k_B is the Boltzmann's constant

$$I_D \approx I_0 e^{\frac{q(V_{\text{GS}}-V_{\text{th}})}{nk_BT}} \quad (4)$$

$$\text{SS} = \left[\frac{\partial \log(I_D)}{\partial V_{\text{GS}}}\right]^{-1} = \ln(10)\frac{nk_BT}{q} \quad (5)$$

where n is the non-ideality factor defined by

$$n = 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{C_{\text{it}}}{C_{\text{ox}}} \quad (6)$$

C_{it} is the interface trap capacitance, C_{dep} is the depletion capacitance, and C_{ox} is the oxide capacitance. However, the measured SS deviates from the Boltzmann limit below a critical temperature and then saturates to a value depending on the technology. The inclusion of interface trap capacitance $C_{\text{it}} \propto qN_{\text{it}}$ in the slope factor helps model the behavior up to ≈50 K, but at deep cryogenic temperatures, leads to unreasonably high N_{it} values.

Another explanation is attributed to a more intrinsic mechanism of the presence of localized trap energy states in the band tail in addition to the delocalized states that take part in conduction [28], [29], revising the saturated value of SS when thermal energy becomes smaller than the band-tail extension (W_t) to a temperature-independent $n \cdot \ln(10) \cdot (W_t/q)$ rather than $n \cdot \ln(10) \cdot (k_BT/q)$ below a critical temperature of ≈ 46 K [11]. In this article, the SS trend has been captured and modeled with BSIM4 parameter CIT whose variation with temperature is shown in Fig. 3(d) and agrees with [14].

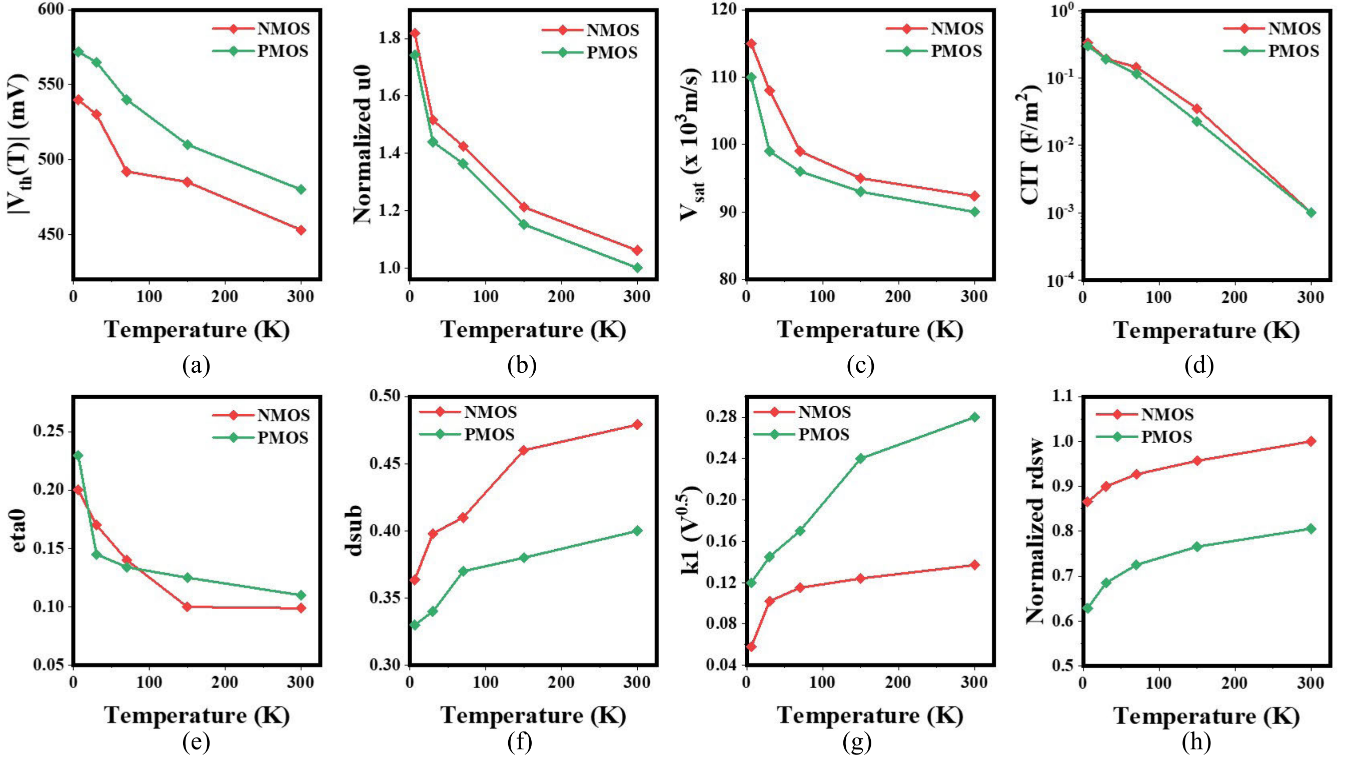

FIGURE 3. Fit BSIM4 parameters. (a) Threshold voltage. (b) Normalized low-field mobility. (c) Saturation velocity. (d) Interface trap charge. (e) DIBL coefficient in subthreshold region. (f) DIBL coefficient exponent in sub-threshold region. (g) First-order body bias coefficient. (h) Zero bias L_{DD} resistance per unit width for RDSMOD = 0 normalized to NMOS at 300 K.

To fit the I_d–V_{gs}, we also tune the DIBL coefficient in the subthreshold regime ETA_0, DIBL coefficient exponent in subthreshold regime DSUB, and first-order body bias coefficient k_1 (see Fig. 3(e)–(g), respectively).

D. Drain–Source PARASITIC RESISTANCE

The drain–source parasitic resistance includes many contributing factors such as contact resistance, diffusion resistance between contact and gate, crowding resistance near the gate, etc. The BSIM4 parameter RDSW is used to characterize temperature dependence along with temperature coefficient PRT. The variation of fit RDSW with temperature is shown in Fig. 3(h)

$$\text{RDSW}\,(T) = \text{RDSW}\,(\text{TNOM}) + \text{PRT}\left(\frac{T}{\text{TNOM}} - 1\right). \tag{7}$$

E. MODEL VALIDATION

All these key parameters provide a closely fit model with a mean rms error of less than 4.24% at all temperature points. Fig. 3 shows the validated models for both NMOS and PMOS at the five temperature points with lines representing fit BSIM4 models and points being experimental data. Fig. 4(a) shows the output characteristics for iso-overdrive voltage of 0.5 V, Fig. 4(b) shows transfer characteristics for the linear region, and Fig. 4(c) shows transfer characteristics for saturation region. Fig. 5 shows the extracted gate capacitance values from the BSIM4 models that will be later used for simulating and predicting the dynamic behavior of the digital standard cells in Section IV.

F. THRESHOLD VOLTAGE TUNING FOR ISO-LEAKAGE MODELS

We use the above developed BSIM4 models to tune the threshold voltage across temperatures so that the devices have the same subthreshold leakage current I_{OFF}. This is done by reducing the V_{th} at a lower temperature so as to maximize the headroom or overdrive ($V_{ov} = V_{gs} - V_{th}$) and increase the ON current. It has been experimentally demonstrated from the foundry process that metal gate work function tuning, metal-oxide cap induced interfacial dipole layers, and lower bandgap channel materials are amongst a few methods to achieve such V_{th} tuning [15]. For the rest of the article, we use the V_{th} engineered BSIM4 models for our analysis and refer to them as "*Iso*-I_{OFF} *models*." The final tuned V_{th} values for NMOS and PMOS devices at the five temperatures for three values of the device OFF currents I_{OFF} is shown in Fig. 6.

IV. POWER AND PERFORMANCE ANALYSIS OF DIGITAL STANDARD CELLS

In this article, we discuss the behavior of INV, NAND2, NAND3, NOR2, and NOR3 gates simulated for industry

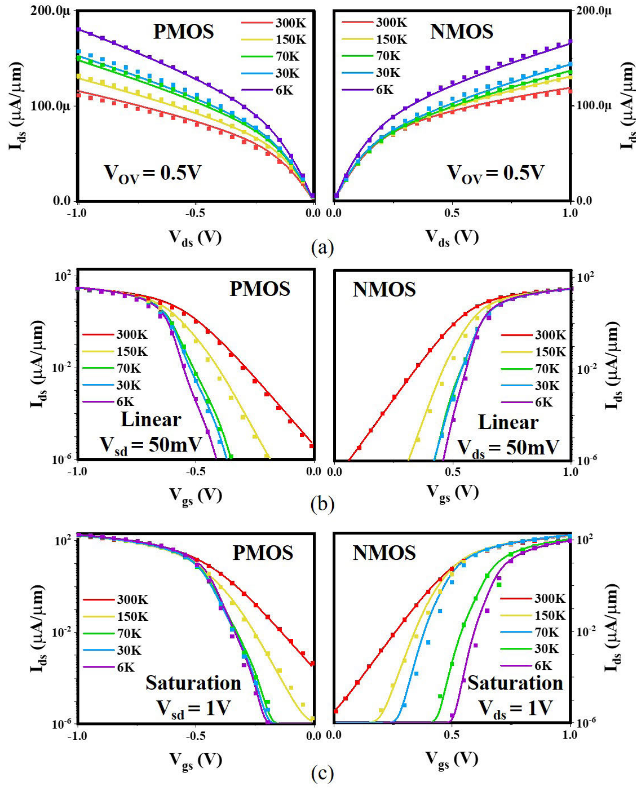

FIGURE 4. Measured device characteristics (points) and fit BSIM4 model (solid lines) after V_{th} tuning for iso-I_{OFF} of 1 nA/μm (lower V_{th} for low-temperature devices as per Fig. 6) as against Fig. 1 which illustrates raw measurements, showing (a) output characteristics for constant overdrive of 0.5 V, transfer characteristics for (b) linear region, and (c) saturation region.

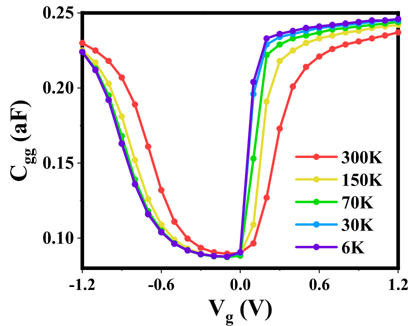

FIGURE 5. Transistor gate capacitance variation with temperature extracted from calibrated BSIM4 models.

standard 28 nm technology node using the above-developed iso-I_{OFF} BSIM4 models. At cryogenic temperatures, many device properties change viz.: 1) increase in threshold voltage; 2) increase in the saturation current; and 3) exponential decrease in sub-threshold leakage current or I_{OFF}. Hence, it becomes difficult to compare the performance and other figures of merits across temperature. Keeping one of the parameters constant will simplify the analyses. The rationale behind choosing iso-I_{OFF} is twofold: 1) this will provide iso-leakage power analysis at low temperatures and 2) tuning devices

I_{OFF}	Type	300K	150K	70K	30K	6K
1nA/µm	NMOS	0.274	0.239	0.215	0.205	0.195
	PMOS	0.410	0.325	0.257	0.195	0.158
0.1nA/µm	NMOS	0.353	0.280	0.244	0.224	0.216
	PMOS	0.507	0.378	0.311	0.301	0.200
0.01nA/µm	NMOS	0.428	0.331	0.289	0.270	0.261
	PMOS	0.605	0.455	0.346	0.280	0.222

FIGURE 6. Final engineered threshold voltage for different values of device-OFF currents (I_{OFF}). (Absolute values shown for PMOS devices.) .

TABLE 1. Standard cells and device sizes (1× drive strength).

Cell	NMOS	PMOS
INV	140nm	170nm
NAND2	140nm	170nm
NOR2	140nm	170nm
NAND3	140nm	170nm
NOR3	140nm	340nm

for I_{OFF} same as that at room temperature will reduce the threshold voltage at cryogenic temperature, providing more overdrive voltage and hence better performance as explained in Section III. All the devices considered in the simulation are of 1× drive strength. The device sizes are shown in Table 1.

A. INVERTER STATIC CHARACTERISTICS

The inverter voltage transfer characteristics (VTCs) are shown in Fig. 7(a). The slope of the curve or the gain of the inverter decreases with a decrease in temperature with peak gain reducing from −4.08 (300 K) to −2.64 (6 K) (35% decrease) due to the lower threshold voltage V_{th} of tuned devices and the increase of the input voltage corresponding to the peak by 4.2% of supply voltage V_{DD} [see Fig. 7(b)]. The plots in Fig. 8(a) show that the inverter trip voltage (V_M) increases with a decrease in temperature. Ignoring the short channel effects, the trip voltage is related to the transconductance parameter $k = \mu CoxW/L$ as

$$V_M \propto \frac{r}{1+r} \tag{8}$$

$r = k_p/k_n$ is the ratio of PMOS and NMOS transconductances. The increase in current for PMOS is higher than that of NMOS (for iso-I_{OFF} devices) indicating a change in mobility for PMOS is higher, thus explaining the upward shift of V_M.

Also, due to the higher strength of PMOS at a lower temperature, the β ratio needed to achieve $V_M = V_{\text{DD}}/2$ increases with a decrease in temperature [see Fig. 8(b) (top)] and the noise margins (NMs) decreases (NM-high by 127 mV and NM-low by 18 mV) with a decrease in temperature [see Fig. 8(b) (bottom)]. In Fig. 9(a) the variation of input pin capacitance with input voltage for 1× inverter for different temperatures is shown. The total switched charge given by

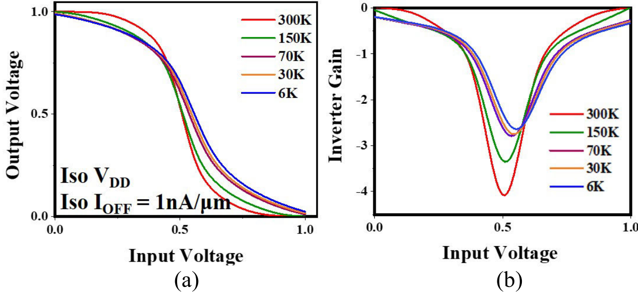

FIGURE 7. Simulated (a) inverter VTCs for iso-I_{OFF} devices at iso-V_{DD} across temperature and (b) resulting voltage gain for 1x inverter. (Device sizes: NMOS: 140/30 nm PMOS: 170/30 nm.)

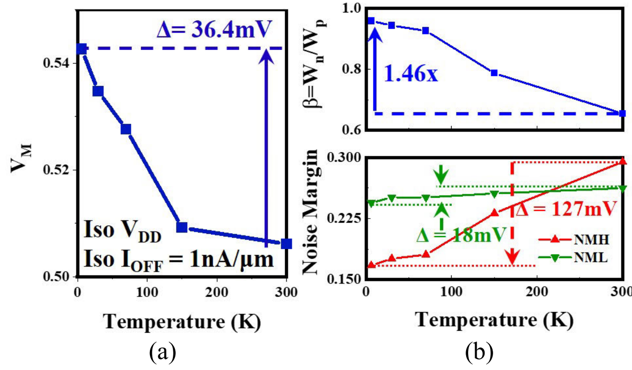

FIGURE 8. (a) Inverter trip voltage V_M for iso-I_{OFF} devices at iso-V_{DD} across temperature showing 36.4 mV shift from 300 to 4 K. (b) β needed to achieve $V_M = V_{DD}/2$ and NMs for 1x inverter.

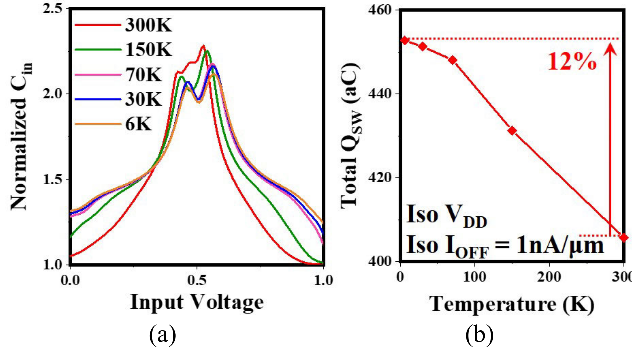

FIGURE 9. (a) Extracted input pin capacitance C_{in} for 1x inverter across temperature showing from simulation. (b) Total switched charge Q_{SW} per input transition for 1x inverter at iso-I_{OFF} and iso-V_{DD} conditions showing 12% increase from 300 to 6 K.

the area under curves Fig. 9(a) increases and at iso-V_{DD}, the input pin cap increases by approximately 12% going from 300 to 6 K which is due to the increased charge inversion at the channel created by the larger overdrive voltage (V_{ov}) created in retargeted V_{th} devices [see Fig. 9(b)]

$$Q_{SW} = \int_0^{V_{DD}} C(V)\, dv. \tag{9}$$

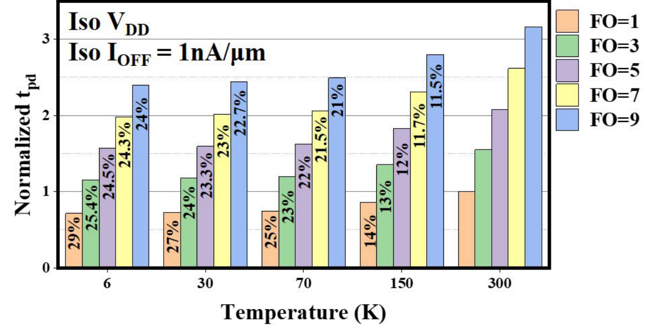

FIGURE 10. Simulated propagation delay of 1x inverter for different fan-out conditions at iso-V_{DD} and iso-I_{OFF} conditions across temperature normalized to FO = 1 at 300 K. t_{pd} defined as time between 50% input and output transitions. The percentage reduction from room temperature is shown for lower temperatures.

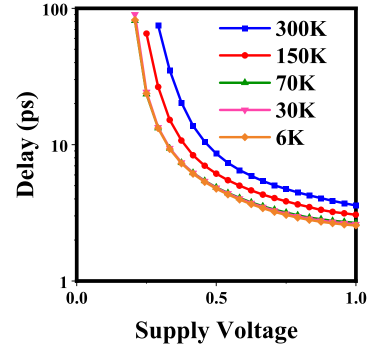

FIGURE 11. Delay versus supply voltage for 1x inverter across temperature.

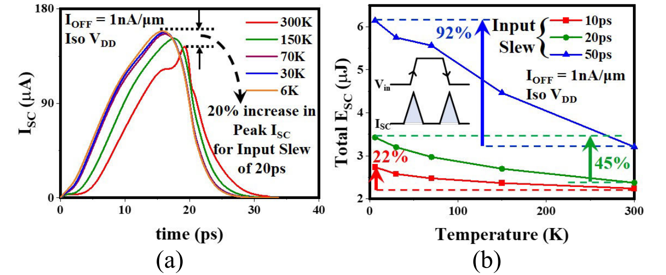

FIGURE 12. (a) Transients of input short circuit current I_{SC} for 1x inverter with input slew of 20 ps across temperature showing peak I_{SC} increase by 20% from 300 to 6 K. (b) Total short circuit energy E_{SC} per transition of input for 1x inverter across temperature at different input slew rates indicating lower increase in E_{SC} for sharper slew conditions at 6 K.

B. INVERTER TRANSIENT CHARACTERISTICS

In the inverter transient characteristics, we see the variation of propagation delay t_{pd} (defined as the time between 50% of input and output transitions) for different fan-out (FO) conditions (see Fig. 10). We observe between ~24% (FO = 9) − 28% (FO = 1) improvements in the same. The switching speed increase is a direct effect of increased ON current at

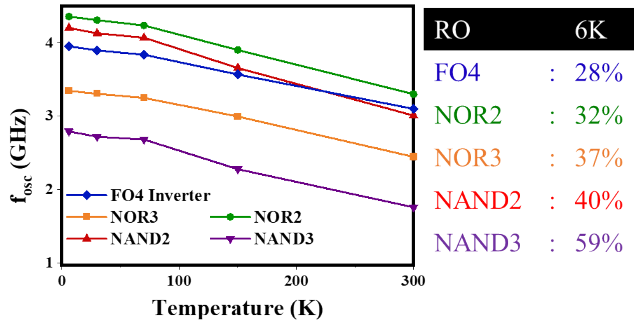

FIGURE 13. Frequency of oscillation from simulation for different ring oscillator structures across temperature at iso-V_{DD} and iso-I_{OFF} conditions and percentage improvement at 6 K compared to 300 K.

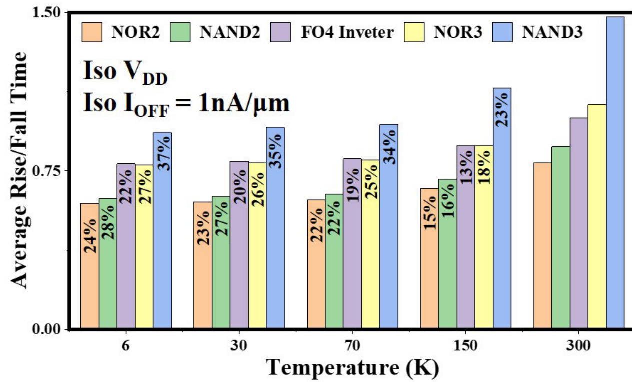

FIGURE 14. Average rise/fall times extracted from ring oscillator frequency across temperature, normalized to 300 K FO4 inverter, at iso-V_{DD} and iso-I_{OFF} conditions.

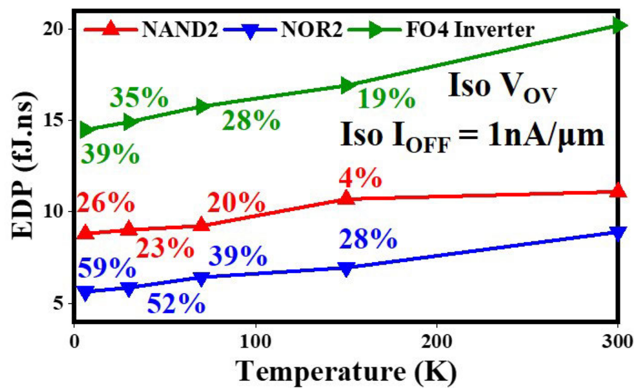

FIGURE 15. Energy-delay product (EDP) improvement for three RO structures across temperature at iso-I_{OFF} and iso-overdrive (V_{OV}) conditions.

lower temperatures with an additional current increase from V_{th} retargeting. The variation of delay with supply voltage across temperature for a 1× inverter is shown in Fig. 11. The transient variation of inverter short circuit current I_{SC} during the switching activity is plotted in Fig. 12(a). One of the key takeaways from [2] was that the internal power of the system increases by 77% going from 300 to 100 K. This can be clearly explained from the BSIM4 models where we notice that I_{SC} increases going from 300 to 6 K due to higher I_{ON} with ∼20% increase in the peak value for input slew of 20 ps

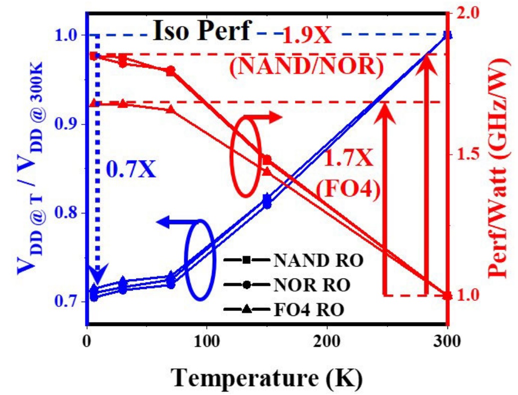

FIGURE 16. Normalized supply voltage needed to achieve oscillation frequency of 300 K RO and corresponding performance per watt improvements.

for a 1× inverter driving a nominal 1 fF load.

The short circuit power which is a function of the input slew increases between 22% for 10 ps slew, 44.5% for 20 ps slew, and 92% for 50 ps slew [see Fig. 12(b)].

C. RING OSCILLATORS

We design multiple RO structures based on NAND2, NOR2, NAND3, NOR3, and FO4 inverters to obtain the frequency of oscillation at the five key temperature points. We see improvements of 28% for FO4, 32% for NOR2, 37% for NOR3, 40% for NAND2, and 59% for NAND3 in the frequency of oscillation compared to their corresponding 300 K values (see Fig. 13) and the rise/fall times normalized to that of FO4 values at 300 K is shown in Fig. 14.

One of the key advantages of operating CMOS at cryogenic temperature is that we can overcome the V_{DD} scaling limits to operate the devices at lower supply voltages, while still achieving better performance compared to room temperature, thus saving power. Fig. 15 shows the EDP improvements at the iso-overdrive (Iso-V_{ov}) scenario. Fig. 16 shows the supply voltage needed at lower temperatures to achieve oscillation frequency observed at 300 K and the corresponding performance/watt. We see between 1.7×–1.9× improvement between 300 and 6 K.

V. CONCLUSION

In this article, we use BSIM4 models with V_{th} tuning for achieving iso-I_{OFF} to characterize primitive standard cells and show through exhaustive simulations that we can achieve up to 90% performance/watt improvement by operating CMOS at 6 K. The analysis of the cost of cooling is beyond the scope of this article and it will add significant overhead. The BSIM4 models provide a pathway for developing a full process design kit (PDK) at cryogenic temperatures which can be used to accurately predict and design cryogenic circuits and systems.

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