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IEEE Journal on Exploratory Solid-State Computational Devices and Circuits—Volume 7, No. 2

WELCOME to the seventh volume, second semiannual issue of the IEEE JOURNAL ON EXPLORATORY SOLID-STATE COMPUTATIONAL DEVICES AND CIRCUITS (JXCDC), a multidisciplinary, open access IEEE journal that is focused on publishing seminal research in the exploration for energy-efficient computing based on physics and materials to enable new devices, circuits, and architecture that will be of great interest to integrated circuit researchers and those working in the IT industry. The articles in the journal are selectively chosen to provide insight into the architectural, circuit, and device implications of emerging quantum nanoelectronic and nanomagnetic device technologies. The discovery of new materials, devices, and circuits for energy-efficient computational circuits will be needed to enable Moore's law to continue for computing beyond the end of the roadmap for CMOS technologies, with significant improvement in energy efficiency and cost per function.

Integrated circuit technology for computing will soon reach an inflection point. The power reduction through device scaling that served the semiconductor industry so well for over 30 years is seeing substantial challenges going forward. Exploratory materials, devices, and circuits that were once considered exotic are now being examined seriously because there may be no other alternatives. At the same time, this new-found freedom of breaking out of "CMOS scaling" introduces many new opportunities to do things completely differently—use a different material, invent a new device that operates on a different physical mechanism, and explore a new circuit function for computing that capitalizes on the unique properties of the new devices.

As such, JXCDC is a multidisciplinary publication that brings together the researchers who are focused toward the exploration of a new device and interconnect, or function for a more energy-efficient integrated circuit for computing. The journal is for the publication of results unifying the areas of solid-state materials, devices, and circuits for novel computation (logic, memory, and communication) toward the exploration of beyond CMOS technology. The publication is not limited to just digital information processing but also encompasses non-Boolean computation, including analog, neuromorphic computing, and novel concepts in computer automata. It is envisioned that these exploratory devices and methods of computing could augment CMOS through their improvement in energy efficiency.

JXCDC is sponsored by the Solid-State Circuits Society, Magnetics Society, Circuits and Systems Society, Council on Electronic Design Automation (as financial sponsors), and by the Electron Devices Society and the Council on Superconductivity (as technical sponsors).

IEEE JXCDC received its first CiteScore in 2019 from Scopus. CiteScore reflects the yearly average number of citations to recent articles published in a journal based on the citations recorded in the Scopus database. The latest CiteScore JXCDC has received is 3.7 for 2020 (three year). In 2017, Clarivate Analytics (formerly Thomson Reuters IP and Science) added the IEEE JXCDC to the Emerging Sources Citation Index (ESCI). The ESCI is a new edition of the Web of Science and includes important journals not yet selected for the science citation index (SCI). However, this is seen as the first step in the process toward having an SCI and an Impact Factor.

There are four regular articles that are in Part I of this Special Topic, our second of the two semiannual issues of the 2021 JXCDC. Part II contains articles on the Special Topic "Emerging Hardware for Cognitive Computing" with Professor Jean Anne C. Incorvia as the Guest Editor. Part III contains articles on the Special Topics "Cryogenic Semiconductor Devices and Circuits for Computing," with Dr. Victor Zhirnov as the Guest Editor.

First, I will introduce the regular articles in Part I, and then in Parts II and III Prof. Incorvia and Dr. Zhirnov will introduce the Special Topic articles, respectively.

For the regular articles in this issue, first, we have an article by M. Zabihi *et al.* [A1], where the authors present and evaluate thresholded matrix-vector multiplication (TMVM), neural networks (NNs), and 2-D convolution on 3-D XPoint. The authors highlight the importance of interconnect parasitics and present guidelines for 3-D XPoint Subarray size and configurations.

In the second article by S. Barve *et al.* [A2], the authors propose a neuromorphic SOFM architecture, based on emerging FeFET and gated-RRAM memory devices, and utilize the underlying device physics of the device technologies to lower power consumption and circuit overhead for learning simple benchmark datasets such as RGB colors to more complex application-specific datasets such as the COVID-19 chest X-rays. An important feature of the architecture

is that its unsupervised; hence, requires no labeled data.

In the third article by D. Kim *et al*. [A3], the authors present an SRAM memory complier for monolithic 3-D carbon nanotube technology. The authors also demonstrate the feasibility of using their memory compiler to generate a monolithic 3-D stack of logic and memory.

In the last paper by N. Jao *et al.* [A4], the authors highlight the need for optimization of the ferroelectric thickness and the read/write voltages for proper functionality.

Some of the articles have supplementary material which is found under the ''multimedia'' section of the article on IEEE Xplore.

I hope you enjoy the articles in this 2020 second half-year issue of JXCDC.

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APPENDIX: RELATED ARTICLES

[A1] M. Zabihi *et al.*, ''Exploring the feasibility of using 3-D XPoint as an in-memory computing accelerator,'' *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 7, no. 2, pp. 88–96, Dec. 2021.

[A2] S. Barve *et al.*, ''NeuroSOFM: A neuromorphic self-organizing feature map heterogeneously integrating RRAM and FeFET,'' *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 7, no. 2, pp. 97–105, Dec. 2021.

[A3] D. Kim, E. Lee, J. Seo, J. Kim, S. K. Lim, and S. Mukhopadhyay, ''An SRAM compiler for monolithic-3-D integrated circuit with carbon nanotube transistors,'' *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 7, no. 2, pp. 106–114, Dec. 2021.

[A4] N. Jao, Y. Xiao, A. K. Saha, S. K. Gupta, and V. Narayanan, ''Design space exploration of ferroelectric tunnel junction toward crossbar memories,'' *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 7, no. 2, pp. 115–122, Dec. 2021.

AZAD NAEEMI (Senior Member, IEEE) received the B.S. degree in electrical engineering from Sharif University, Tehran, Iran, in 1994, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2001 and 2003, respectively.

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Dr. Naeemi was a recipient of the IEEE Electron Devices Society (EDS) Paul Rappaport Award, the NSF CAREER Award, and the SRC Inventor Recognition Award.