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Differential Electrically Insulated Magnetoelectric Spin-Orbit Logic Circuits

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ABSTRACT Beyond complementary metal–oxide–semiconductor (CMOS) devices have functionalities different from CMOS transistors, and therefore, the development of novel circuits that leverage their properties is necessary for their practical application to computing. The magnetoelectric spin-orbit (MESO) device has been proposed as one of the promising energy-efficient beyond CMOS device candidates, and several basic circuit blocks have been demonstrated with MESO. In this work, we propose a new differential MESO device that enables differential logic circuit design with better interstage isolation. This improves the output voltage of MESO circuits, provides signal common-mode noise rejection, and eliminates any sneak current path. We demonstrate the functionality of multiple essential logic circuit blocks implemented with MESO devices.

INDEX TERMS Beyond complementary metal–oxide–semiconductor (CMOS) logic, magnetoelectric (ME), SPICE, spin-orbit (SO), spintronic devices.

I. INTRODUCTION—CIRCUITS BEYOND CMOS

THE progress of computing in the past four decades was mostly enabled by the scaling of complementary metal–oxide–semiconductor (CMOS) transistors according to Moore's law [1]. Despite success in shrinking the size of CMOS transistors, voltage and frequency scaling has slowed down and has led to computing performance being limited by power [2], [3], instead of the number of transistors. To satisfy the ever-increasing demand for computing capability, it becomes natural to explore various energy-efficient beyond-CMOS alternatives. Systematic benchmarking of beyond-CMOS devices and circuits was performed [4], [5]. It demonstrated that magnetoelectric spintronics-based devices, especially magnetoelectric spin-orbit (MESO) logic [6], promise ultralow switching power due to utilization of magnetoelectric (ME) material, while it is critical to demonstrate MESO device feasibility to develop practical logic circuits with it is not trivial at all. Several essential circuit characteristics for logic applications have been pursued in efforts for all-spin logic circuits [7] and exploration of SOTFET [8] and CoMET [9] circuits. For MESO, the fundamental building blocks, such as sequential and combinatorial circuits, have been shown [10] using its original device structure. Here, we propose a new MESO device design, where we transform the single-ended input/output signal to a differential one and eliminate any feedback signal propagation [11] by insertion of an insulating layer.

II. PROBLEMS AND SOLUTIONS FOR SPINTRONIC CIRCUITS

In the original MESO concept, as shown in the top scheme of Fig. 1(a), each MESO device consists of two critical modules: the ME capacitor at its input and the spin-orbit (SO) magnetism-to-charge conversion module, which provides an electric current as of the signal output. Specifically, the ME module can be made of multiferroic material $BiFeO_3$ (which is both ferroelectric and antiferromagnetic, FE+AFM), sandwiched between a metallic ferromagnetic layer (FM) and metallic interconnect (IC) layer for the top and bottom electrodes, respectively. By switching the ferroelectric (FE) polarization of the ME material, the computing state is written and stored due to its nonvolatility. The SO module comprises the ferromagnet (FM) as the source of spin-polarized carriers, a spin-coherent layer, and the SO

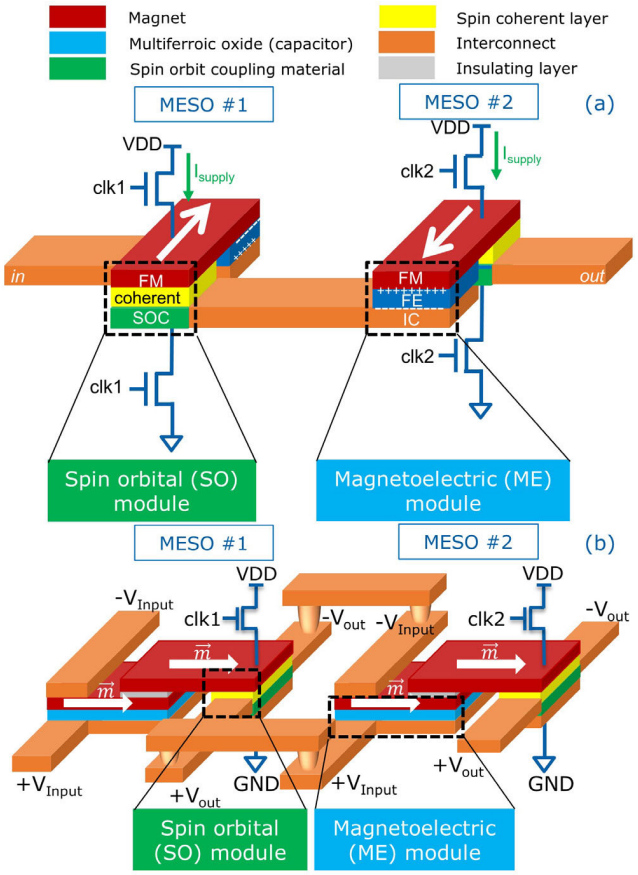


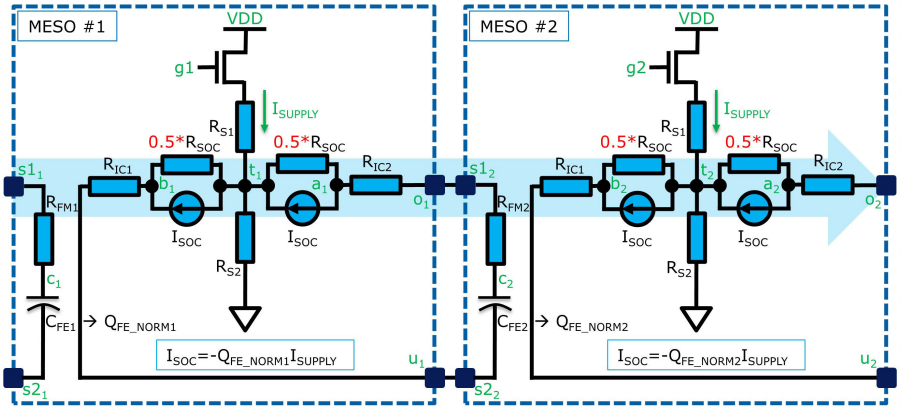
FIGURE 1. Two cascaded MESO devices. (a) Original scheme of MESO logic [10], which uses the output from one side of the SO module. Each device needs two MOSFET transistors for clocking control. (b) Improved scheme of MESO logic, which uses the differential outputs from both sides of the SO module. Only one MOSFET transistor is needed for each MESO. An insulating layer has been inserted into the previously homogeneous FM to electrically isolate the ME input module from the SO output module. The FM (red)-insulating (gray)-FM (red) layered structure couples together to function as one FM that switches coherently.

coupling (SOC) layer, respectively, going from the top to bottom in Fig. 1(a). The vertical charge flow is polarized into spin current by the FM layer. Then, the spin orientation of the vertical flow is mostly preserved in the spin-coherent layer, and the spin current is converted to a horizontal charge current by the SOC layer. The FM state is converted by magnetic exchange coupling at the interface of the multiferroic oxide and the FM, using the ME effect in $BiFeO_3$. Conversely, the output current, whose direction is determined by the FM's magnetization state, will charge/discharge the ME capacitor of the next MESO device and switch its FE polarization. In conventional CMOS technology, logic circuit leakage is shut off in steady state by controlling it with power gating or clocking transistors. Similarly, header and footer transistors are used to control the vertical current flow through the SO stack from the power supply (VDD) to the ground (GND).

The gates of the header and footer transistors are controlled by clocking signals (clk1 and clk2). They are ON for a short time necessary to switch the ME, and then, they are OFF for the time required for FM to complete switching its state. A two-phased clock (clk1 and clk2) can be applied to consecutive stages of the MESO logic. At time intervals when both clocks are ON, SO of MESO #1 will be enabled to conduct vertical current. The generated spin-to-charge current will flow horizontally to reach the bottom electrode of the ME in MESO #2. Simultaneously, the conduction path from the top electrode of the ME to the ground in MESO #2 will be enabled as well. The resulting voltage across ME in MESO #2 would switch its FE polarization. Once the FE polarization (P) in MESO #2 switches, its antiferromagnetic (AFM) order will follow to switch and couple with the FM layer on the top. After the FM layer changes its magnetization direction, the spin polarization in the SO module of the next MESO stage will also change its sign. As a result, the charge current generated by this spin current in the next MESO will flip its direction. From here, we can see that the states of P, AFM, FM, spin polarization, and charge current are coupled together, where each variable has two states. With two cascaded MESO devices, the state of the first MESO will drive the next MESO to have the opposite state.

In the original design [10], only one side of the SO current output is used to control ME and, thus, is not fully utilizing its driving potential capability. Also, when more stages of MESO are cascaded with just two-phase clocking, there will be a conductive path leading to backward signal propagation, similar to the sneak path discussed in [11]. This can cause disturbance of previously switched ME capacitors and, thus, cause logic functionality errors. As shown in the graph in Fig. 1(a), the use of multiphase clocking to eliminate this effect was, therefore, necessary.

To address these two issues, a differential MESO is proposed and shown in Fig. 1(b). There are two major changes in the differential MESO device architecture as follows. First, in the SO module, both sides of the SOC layer are connected to the two electrodes of the ME in the next MESO stage. Second, the previous single homogeneous FM layer is replaced by a composite layer comprising two conducting FM layers (red) sandwiching an insulating layer (gray). The FM layers are expected to have strong exchange coupling via the insulating layer. More rigorous micromagnetic simulation can be done to understand its switching dynamics for better optimization, but the goal here is to have coherent switching of this composite structure. With this change, both the input and the output of each MESO device now have become differential, which also provides the benefit of suppressing the common-mode signal noise. In the original single-ended MESO version, the ME capacitor in the next cascaded MESO stage can only be charged during the overlapping time of its clock enable phase with the previous MESO stage's clock enable phase. In the new differential MESO, the SO of MESO #1, the two interconnects, and the ME capacitor of MESO #2 are electrically isolated from the other stages.



Parameter	Description	Values
VDD	Supply voltage	100mV
VG	gate voltage for power switch	0.8V
R_{S1}, R_{S2}	SO stack vertical resistance	100 Ω
R_{FM}	Ferromagnet film resistance	1 Ω
R_{SOC}	Lateral SOC channel resistance	5 kΩ
R_{IC}	Interconnect resistance	1 kΩ
$V_{coercive}$	ME coercive voltage [10]	~68mV

FIGURE 2. Circuit schematics of an MESO inverter. The light blue arrow indicates the direction of information/signal propagation. After switching, the bit stored in the second MESO device will be the inverse of that of the first MESO device. Here, Q_{FE_NORM} is the normalized charge for C_{FE}, whose polarization direction determines the FM polarization and, thus, the spin-to-charge current direction. For R_{FM}, R_{S1}, R_{S2}, and R_{SOC}, they highly depend on the material choice. Here, we can use the size of 20 nm × 20 nm for the SO module as an example. FM: with the resistivity of 4e-7 Ω*m and thickness of 1 nm, R_{FM} is 1 Ω. Vertical layer stack: with the resistivity of 4e-6 Ω*m (~average of FM/coherent/SOC/interface) and thickness of 10 nm for the SO layer stack, R_{S1} or R_{S2} would be 100 Ω. SOC: with the resistivity of 1e-5 Ω*m and thickness of 2 nm, R_{SOC} would be 5 kΩ. Different interconnect layer stacks, the material choice and fabrication could vary these estimated values significantly, but the benefit of the differential design should still remain.

Therefore, whenever the clk1 is high, the SO in MESO #1 will generate spin-to-charge current to flow in its output driving current loop and will charge/discharge the ME in MESO #2. In other words, only one clock ON is required to drive the next MESO stage instead of two overlapping clocks. This greatly simplifies the control and clocking scheme. In addition, the electrical isolation of the differential MESO device input eliminates disturbance of previous stages. Another subtle difference is where the interconnect is connected. In the original design, the signal output wire connects to the green layer, which suggests the utilization of the bulk SO material. In the new design, this wire connects to the interface between the green and yellow layers, which is an alternative SO technique that utilizes the 2-D electron gas (2DEG) [12] because of its potentially higher conversion efficiency. Both technology options (bulk or 2-DEG) would work for the MESO SO output.

It should be mentioned that several factors, such as R_{FM} and parasitic variation, can practically make potential values at o_1/u_1 asymmetric with respect to t_1 in the transient response. As long as the potential difference between o_1 and u_1 is higher than the coercive voltage of C_{FE}, MESO #1 can switch MESO #2. For the transient state, there will be identical nonzero currents in R_{IC1} and R_{IC2}. According to Kirchoff's law for current, at the b1 node, we have $I(R_{IC1}) + I_{SOC} + I(0.5^*R_{SOC}) = 0$. Similarly, at a1 node, there is $I(R_{IC2}) + I_{SOC} + I(0.5^*R_{SOC}) = 0$. Therefore, the currents in 0.5^*R_{SOC} of each differential branch should be identical. The IR drops for $b_1 - t_1$ and $t_1 - a_1$ are the same. However, if the IR drop on R_{IC1}/R_{IC2} is different, the potential of o_1/u_1 will be asymmetric to t_1. In the steady state, because charging/discharging of C_{FE} is complete, no current will flow through $C_{FE}/R_{IC1}/R_{IC2}/R_{FM}$. The IR drops for $u_1 - t_1$ and $o_1 - t_1$ are both $I(0.5^*R_{SOC})^*0.5^*R_{SOC}$. Therefore, the potential values of $(a1, b1)$ and $(o1, u2)$ should be symmetric with respect to t_1. A few cases with unbalanced interconnect are discussed in the Supplementary Material.

III. MESO INVERTER

In this section, the new MESO device design is used to construct the inverter and simulate its switching behavior.

With fully differential input and output signals, two connected MESO devices have equivalent circuit models, as shown in Fig. 2. In each MESO device, there are two differential half-circuit blocks for input and output, respectively. For output (MESO #1, for instance), there is a vertical circuit path of VDD → nMOS transistor → R_{S1} → t_1 → R_{S2} → GND. Here, R_{S1} and R_{S2} approximate the through layer resistance for the SO module. There is also a horizontal (differential) circuit loop of t_1 → 0.5^*R_{SOC} → R_{IC2} → o_1 → $S1_2$ → R_{FM2} → c_2 → C_{FE2} → $s2_2$ → u_1 → R_{IC1} → 0.5^*R_{SOC} → t_1, within which the spin-to-charge current is flowing when the device is active. The original single R_{SOC}, representing the total resistance of the SOC layer, is split into two halves and connected at node t_1, which is the midpoint of the differential SOC layer. The ideal current-controlled current source is in parallel with each half of $R_{SOC} = 5$ kΩ and embodies the converted charge current $I_{SOC} = -Q_{FE\_NORM} \times I_{SUPPLY}$. Here, Q_{FE_NORM} refers to the normalized FE charge of ME, and I_{SUPPLY} refers to the vertical current from VDD to the ground. R_{IC1} and R_{IC2} (=1 kΩ, the same as [10]) represent the resistance value of each of the differential signal interconnect lines, vias, and the resistive interface between wire/via and SO output terminals. Meanwhile, due to the large R_{SOC}, even longer wire lengths do not significantly affect the device/circuit functionality. For the input, the magnet's "through-layer" resistance R_{FM} of ~1 Ω in series with C_{FE}, form a circuit branch isolated from the output part. C_{FE} is modeled using a Verilog-A file to mimic the FE polarization versus voltage hysteretic behavior. A specification similar to

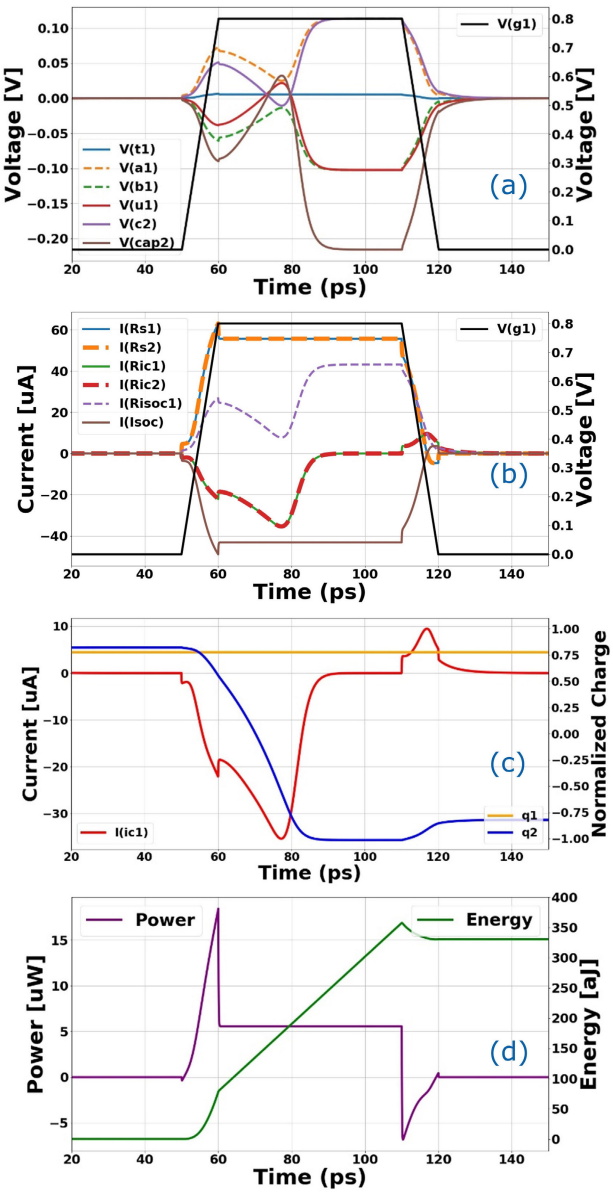


FIGURE 3. Simulated switching characteristics of an MESO inverter: (a) voltage, (b) current, (c) normalized charge, and (d) power and energy.

[10] is used, and the coercive voltage is ∼68 mV. The main simulation parameters are listed in the table in Fig. 2. Here, the parameters are estimated from a few representative measurements [13]–[15]. With a different layer stack, material, or fabrication method, and so on, the parameters could change significantly, but the benefits from differential design should still remain.

Using the equivalent circuit model above, transient simulation is performed with the Cadence Virtuoso Spectre [16] simulator. Fig. 3 shows detailed transient switching characteristics. In Fig. 3(a), the black curve is the single clock signal fed to nMOS of MESO #1 and could be used as a reference. The pulsewidth is 50 ps, and the rise/fall time is 10 ps. Node t_1 is only a few mV above ground voltage since R_{S2} is low. With respect to t_1, the potentials of a_1 and b_1 are symmetric due to the balanced differential circuit with the capacitive load. The potential at b_1 is different from u_1 during the transient time because of the IR drop of R_{IC}. Similarly, the potential at c_2 is lower than that of a_1. By subtracting $V(c_2)$ from $V(u_1)$, the voltage across the C_{FE2} capacitor in MESO #2, $V(\text{cap}_2)$, can be obtained. Because of the transient negative capacitance effect in the FE [17], the absolute value of $V(\text{cap}_2)$ increases, decreases, and again increases versus time during the FE switching. The voltage across the FE goes through the S-shaped polarization charge versus the voltage curve of the ME material in this transient manner. In Fig. 3(b), several critical current variables are plotted with the clock signal as a reference. Once the clock signal becomes larger than the threshold voltage, Vth, in the MOSFET, the current starts to flow vertically through R_{S1} and R_{S2}. The I_{SOC} current source controlled by this vertical current will then generate a spin-to-charge current with a direction based on the FM's magnetization. This current flows from I_{SOC} through R_{SOC} and R_{IC}, but the differential output voltages a_1 and b_1 eventually reach equal (but opposite sign) steady-state voltages of $I_{SOC} \times 0.5R_{SOC}$, and no current flows out through R_{IC} into C_{FE}. When the voltage across C_{FE} in MESO #2 exceeds its coercive voltage, C_{FE} in MESO #2 switches its polarization. Approximately 40 ps after the rising edge of the clock signal, the current in R_{IC1}/R_{IC2} becomes zero. This is because C_{FE} already completed its switching, and now, the spin-to-charge current only flows in R_{SOC}. In a further optimization of the design, the clock pulsewidth could be even narrower to avoid wasting energy. In Fig. 3(c), the normalized C_{FE} charge of each MESO is plotted with a charging current flowing in R_{IC1} as the reference. For MESO #1, since C_{FE} is not disturbed, its charge remains constant. For MESO #2, C_{FE} charge has been initialized in the simulation as positive. From 50 to 90 ps, the current in R_{IC1} spikes up to switch the C_{FE} polarization in MESO #2 to negative. Here, only while the FE charged polarization is at its saturated maximum, the normalized charge is about 1, in the unit of $C/\mu m^2$. Once the driving voltage is removed (i.e., the clock signal turns off the supply current), the C_{FE} polarization goes from the saturation (~ -1) back to the remnant value (~ -0.8). In Fig. 3(d), the current and voltage at VDD and the clock signal swing on the gate node of the nMOS transistor are used to calculate the total power and energy. The power curve shows transient spikes during the rise and fall times of the clock signal, which are due to the charging/discharging occurring when the nMOS transistor is turning on/off. During the switching of C_{FE}, the power stays ∼6 μW. At around 90 ps, the switching has just been completed, and the corresponding energy is ∼250 aJ.

We then sweep the bias voltage on the gate and drain terminals of the nMOS transistor to explore the parameter space. As shown in Fig. 4, the VDD increases from 5 to 100 mV, and the gate voltage (VG) increases from 0.1 to 0.8 V. In each simulation run, the final charged state of MESO #2 C_{FE} is checked. Both MESOs were initialized with a charge state $-$Q, so it would be considered functional if MESO #2

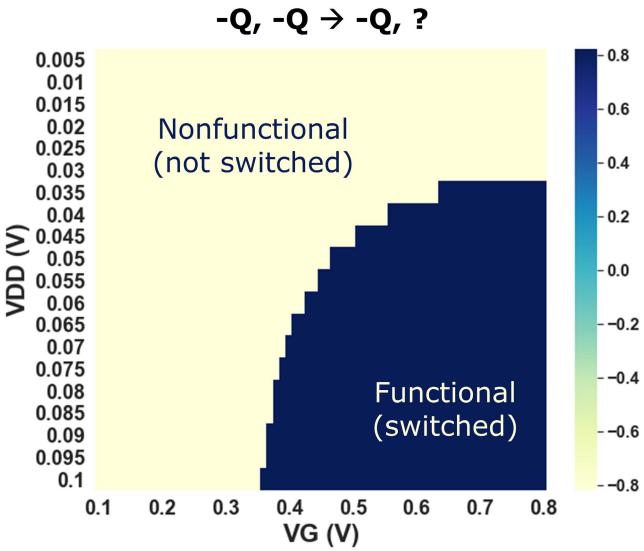


FIGURE 4. Switching diagram of two cascaded MESO gates with a range of VDD and VG values. With the two MESO gates initialized with −Q, the circuit is considered functional if the second MESO gate switches to +Q.

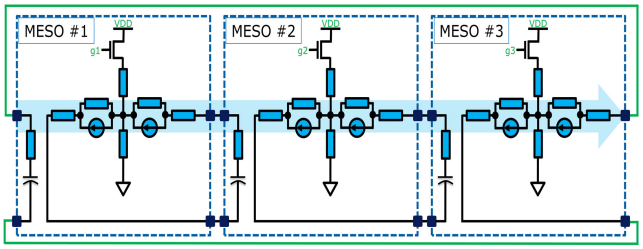


FIGURE 5. Circuit schematic of the three-stage ring oscillator with stage insulation.

switches to +Q. From the map, the data indicate that the switching is still possible even if VDD is as low as ∼35 mV or VG is as low as ∼0.4 V. Even though the switching dynamics or speed is affected, these results show the possible range of bias conditions that could achieve ultralow-power consumption in an MESO gate. Here, we only show initial conditions of −Q/−Q, but symmetric behaviors are shown for the other initialization states.

IV. CASCADED INVERTERS

In this section, the inverter of MESO is cascaded to show sequential logic and combinatorial logic, which are essential logic circuits for computation.

By adding another stage to the two-stage MESO circuit and connecting the output of the third to the input of the first stage, we make a three-stage synchronous ring oscillator, as shown in Fig. 5. To switch these three stages and propagate the state, three clock signals with a period of 5 ns and pulsewidth of 1 ns control the nMOS gate terminal of each MESO, as shown in Fig. 6. The three clock signals are shifted with 1.5 ns to avoid any overlap. In the right part of Fig. 6, the normalized charge of each MESO is plotted along with its control clock. When g1 is at a high level, the SO

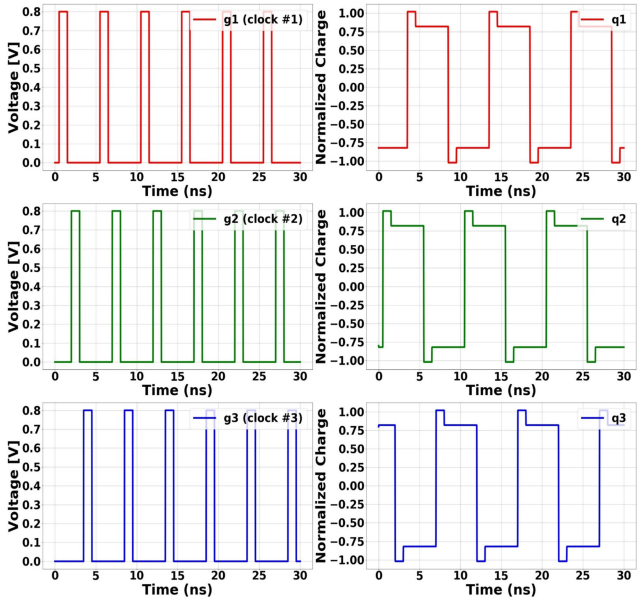


FIGURE 6. Waveforms in the three-stage ring oscillator. The left columns are the three-phase clock signal applied to each stage. The right columns are the normalized charge for each MESO device.

of MESO #1 will be enabled to switch ME of MESO #2, which corresponds to the q2 switching. Similar switching happens for adjacent stages. Hence, clear oscillation of the charge in q1/q2/q3 signals can be observed, having a period of 10 ns. The fact that the state remains after switching OFF the driving transistors and confirms the sequential logic property. By using a faster clock frequency, this oscillation frequency could be further increased. After each FE switching event, the absolute amount of polarization remains ∼1 in the first ∼1 ns and then reduces to ∼0.8. This is because, during the first 1 ns, the driving current drives the capacitor C_{FE} close to C_{FE} saturated polarization. Once the driving force is OFF, Q_{FE_NORM} goes back to the C_{FE} remnant polarization.

Another critical operation required in logic circuits is combinatorial logic. This can also be realized with this new differential MESO. Since the supply current-access enabling nMOS transistor can be shared across multiple MESO stages that switch only once, efficient power gating of combinatorial MESO gates can be achieved.

In Fig. 7, seven MESO devices (representing the simple form of cascaded combinatorial gates) are cascaded and share the same power gating nMOS transistor, whose gate terminal is controlled by clock g1. The supply current input nodes of each of the MESO devices are merged together and highlighted in red. From MESOs #1 to #7, the initial and final charges of the capacitor C_{FE} are labeled +/−Q below the corresponding MESO device. To see the switching of each device, the seven devices are set up with initial conditions of −Q/−Q/+Q/−Q/+Q/−Q/+Q. The circuit is expected to carry the state from left to right.

In Fig. 8, the simulation data of the seven-stage MESO, which shares the nMOS power gating transistor, are shown.

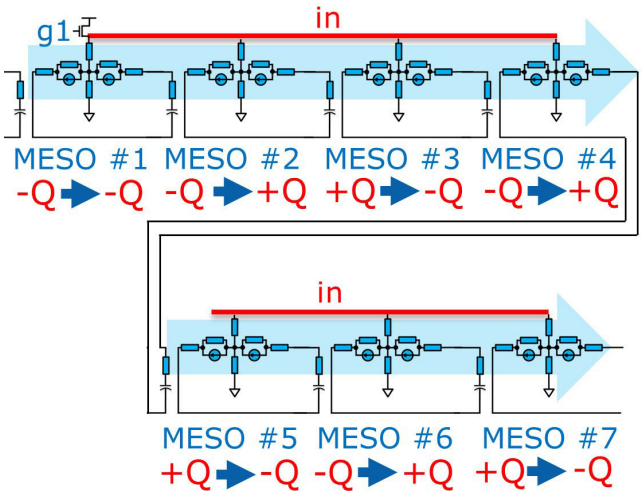


FIGURE 7. **Circuit schematics of seven cascaded inverter stages representing how a signal would propagate/ripple through seven combinatorial logic gates.**

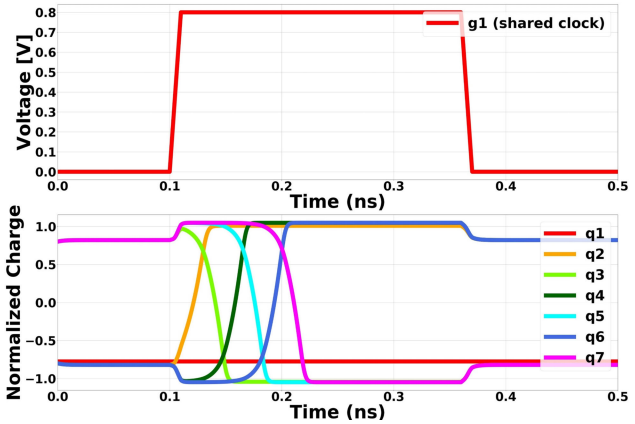


FIGURE 8. **Simulation of the switching transients of seven cascaded inverter stages, where a shared enabled power gating nMOS transistor allows state switching propagation consecutively for all stages of MESO.**

During operation, the g1 clock provides a single pulse of 0.25 ns with a rise or fall time of 0.01 ns. Once g1 rises to the high level, the current starts to flow from VDD down to the ground through all seven MESO devices. Without any disturbance, the charge state of MESO #1 will remain constant for the entire operation. MESO #2 will start to switch during the g1 high pulse. Before MESO #2 completes switching, MESO #3 will start to flip with a small lag. A similar state propagation continues for the following stages. For the state to pass all seven stages, it only takes 0.12 ns, which is determined by the intrinsic switching speed of the MESO device's ME and ferromagnetic materials.

V. SEQUENTIAL-COMBINATORIAL MESO LOGIC

With the sequential and combinatorial logic types validated, a circuit scheme combining both is set up, as shown in Fig. 9. Here, four latches, each implemented with just one MESO device, sequentially pipeline three combinatorial logic sections between them. The three combinatorial sections have 15, 15, and 10 MESO stages, respectively. The

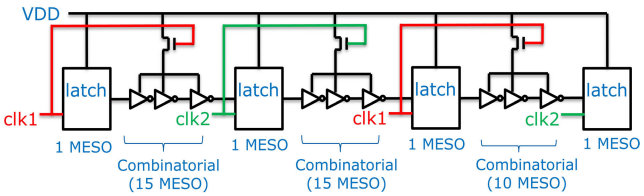


FIGURE 9. **Illustration of a circuit implementing the combination of sequential and combinatorial logic. Each latch is one MESO device, and there are three combinatorial logic paths with 15, 15, and ten MESO gates, respectively, between latches. Only two clock control signals are needed for fully functional sequential control of the entire circuit.**

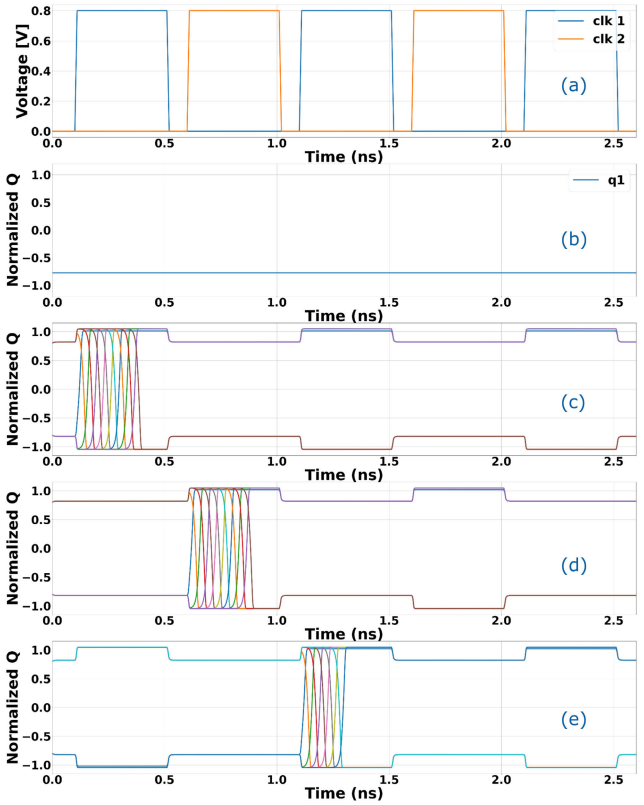


FIGURE 10. **Simulated switching characteristics for a combination of sequential and combinatorial logic. A two-phase clock with a frequency of 1 GHz is used to control the switching of each pipeline section in turns. (a) Clock signals, (b) normalized charge for MESO #1, (c) switching of first combinatorial section and the second latch, (d) switching of the second combinatorial section and the third latch, and (e) switching of the third combinatorial section and the fourth latch.**

devices in each combinatorial section share the same power gating nMOS. This nMOS gate terminal is controlled by a clock signal, which is also connected to the enable of this section's driving latch.

The switching behavior of this combined circuit is shown in Fig. 10. During operation, only two clock signals are needed for control, as shown in Fig. 10(a). Here, the clock period is 1 ns, and the phase shift between two clock signals is 0.5 ns. Since no driving force is applied to it, the first latch (MESO #1) will remain in the $-Q$ state, as shown in Fig. 10(b). When clk1 rises and reaches 0.8 V, both the

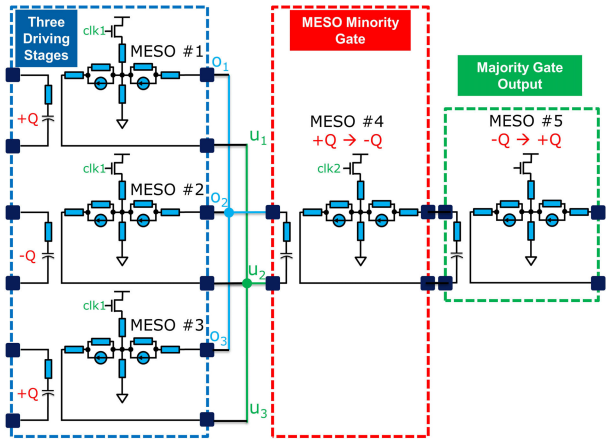


FIGURE 11. Circuit schematic of an MESO majority gate with the electrically insulated FM.

first latch and the first section of 15 combinatorial gates are enabled. The switching of state will propagate from MESO #2 → #3 → #4 and so on and stop after the second latch (at MESO #17) is switched. Similarly, when clk2 rises and reaches 0.8 V, the second latch and the second section of 15 combinatorial gates are enabled. The switching will propagate from MESO #18 → #19 → #20 and so on and stop after the third latch (MESO #33) is switched. When the clk1 becomes high for the second time, the ten combinatorial gates in the third section and the fourth latch will complete their switching. In summary, the three sections are switched within one and half periods of the clock signal. Within each pipeline section, the logic signal propagates through the cascade of combinatorial logic gates, switching in turns based upon the final logic state presented on their inputs.

VI. MAJORITY GATE

Another key feature that the MESO device promises are to enable the majority-gate circuit function with far fewer devices compared to a CMOS implementation [6]. This greatly increases the MESO logic functional density and power efficiency over CMOS.

As shown in Fig. 11, a three-input majority gate is implemented with the differential MESO devices. From left to right, we have: 1) the input signal driving stage; 2) the minority gate stage; and 3) the inverting gate stage (with the majority output), respectively. Each input/output node is labeled with a pin having a dark blue square. The output signals ($o1$–$u1$)/($o2$–$u2$)/($o3$–$u3$) of MESO drivers #1/2/3 are merged and connect to the input of MESO #4. During operation, the input signals from the input driver MESO #1/#2/#3 devices hold their input FM state. The minority gate MESO #4 will switch to the state, which is the minority state of the three MESO inputs. If required, MESO #5 will invert the output of MESO #4 so that the final output is behaving with the majority gate function.

Fig. 12 shows the simulation results of this three-input majority gate circuit. As shown in Fig. 12(a), two clock signals have pulse widths of 0.1 ns and rise/fall times of 0.01 ns. The nonoverlapping phase delay between clk1/clk2

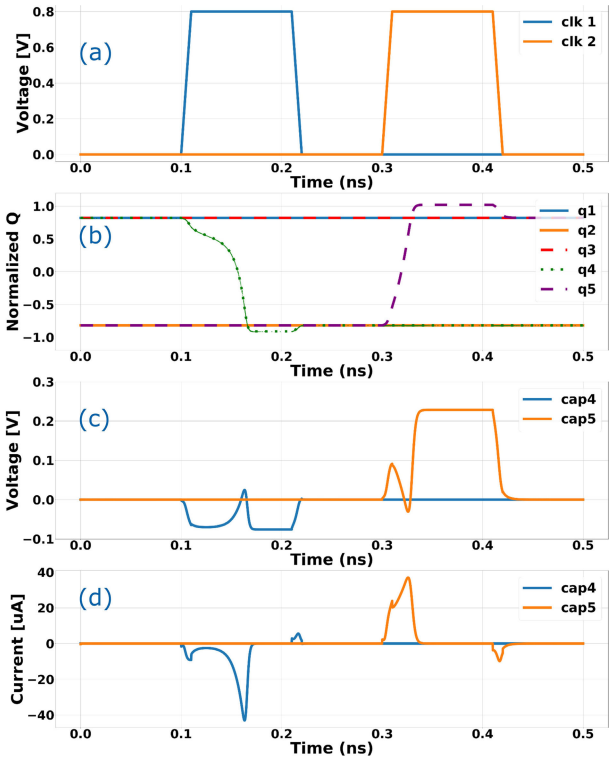


FIGURE 12. Simulation results of three-input majority gate circuits. (a) Two-phase clock, (b) normalized charge state of each MESO device, (c) voltage across C_{FE} in MESO #4/#5, and (d) charging current for C_{FE} in MESO #4/#5.

is 0.2 ns. In Fig. 12(b), the normalized charges are plotted for all five MESO devices. The q1/q2/q3 of the input devices are set as +Q/−Q/+Q, where the minority state is −Q. q4 and q5 are set as +Q and −Q. When clk1 becomes active, MESO #1/#2/#3 will be enabled and generate a voltage across C_{FE} of MESO #4. This makes q4 switch from +Q to −Q (minority state). Until clk2 becomes active, switched MESO #4 will then drive MESO #5, and it is changed from −Q to +Q, which is the final output and the correct majority state of the input driving devices. In Fig. 12(c), the voltages of C_{FE} for MESO #4/#5 (cap4/cap5) are plotted. It can be noted that the maximum absolute input voltages for MESO #4/#5 are approximately 80 and 230 mV, respectively. Meanwhile, the dip in the absolute voltage happens earlier for MESO #5 with respect to the trigger of its corresponding clk. For MESO #5, it is like the two-stage inverter case. When the MESO circuit reaches its stable state, there will be no current flowing in R_{IC}. The differential output voltage is determined by the product of R_{SOC} and I_{SOC}. For MESO #4, the input comes from joint nodes of MESO #1/#2/#3. Even when the circuit reaches its stable state, the potential at node "a" in MESO #1/#2/#3 will be different since I_{SOC} has different directions in MESO #1/#2/#3 due to the C_{FE} state (+Q/−Q/+Q here). Then, there will be constant current flowing in R_{IC}, which causes IR drop from the product of R_{SOC} and I_{SOC}. Eventually, the three-input driving devices will generate a lower output voltage (input to MESO #4) compared to the two-stage inverter case. In Fig. 12(d), the currents charging C_{FE} of

MESO #4/#5 are plotted. Like in Fig. 12(c), the charging current for MESO #4 takes a longer time than that for MESO #5 due to the IR drop in the interconnect.

The exercise above was also repeated for cases with all different initial conditions of MESOs #1/#2/#3/#4/#5. The simulation data are postprocessed with a python script and validated with the ideal logic truth table. The output voltages from MESO #1/#2/#3 input drivers have two different absolute values, ∼80 and ∼230 mV. These two voltage values depend on the states of the three input MESO devices. The voltage ∼80 mV/∼230 mV corresponds to the pattern of "ABB"/"AAA," where A/B refers to the state of +Q/−Q or −Q/+Q. The case in Fig. 12 is initialized as +Q/−Q/+Q, which follows the "ABB" pattern and gives a lower output voltage ∼80 mV. As discussed in [11], the single-sided MESO majority-gate can have four different output voltage levels, which are not symmetric with respect to ground. Among them, the minimum voltage can be as low as sub-10 mV. Here, with the differential design, the minimum output voltage is greatly enhanced, and output voltage levels become symmetric to the potential of the "t" node. These changes help further relax the requirement for increasing the SO output voltage and lowering the ME coercive voltage of the MESO device.

Based on the three-input majority circuit, a five-input majority circuit was also constructed. It turned out that the voltage across C_{FE} of the minority gate will sometimes be below its coercive voltage. Relating to the input voltage decrease from an MESO two-stage inverter to an MESO three-input majority gate circuit, all these results indicate the same input scaling penalty. In other words, the number of input devices for a majority gate can be increased but at the cost of reducing the maximum input differential signal across C_{FE}. In the five-input majority-gate case, there are several options to solve the issue. The VDD could be increased to enable a larger output signal voltage, but this also increases power consumption. Alternatively, C_{FE} needs to be further optimized in order to have a lower coercive voltage. With novel materials [14], the SOC efficiency is also expected to further increase, which could lead to a better output signal drivability.

VII. CONCLUSION—BENEFITS OF NEW CIRCUITS

In this work, a novel differential MESO device design with its FM having an insulating layer is proposed. This new design takes full use of the dual electrical signal output of the SO module to enhance its drivability. In addition, the feedthrough interference in the original (first generation) of MESO is eliminated by way of inserting an insulating layer in the FM so that the robustness of the entire circuit is improved. The good isolation between stages allows simplification of clock signals and needs only the half number of nMOS transistors for sequential logic control. Using the new design, essential circuit building blocks, such as inverter, ring oscillator, sequential-combinatorial logic, and majority-gate circuits, are constructed, and their functionalities are validated with simulation. Under the power supply operation of 100 mV, these circuit blocks have been modeled in SPICE simulation for their functionalities, bias conditions, scalability, and power consumption. The device-circuit co-optimization work described in this article provided insight that deepened the understanding of the design tradeoffs and resulted in a set of device/logic circuits. Those circuits also make the MESO logic design techniques more complete for the implementation of full compute engines.

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