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Special Topic on Tunnel Field-Effect Transistors

THE tunneling field-effect transistor (T-FET) is considered a future transistor option due to its steep-slope prospects and the resulting advantages in operating at low supply voltage (V_{DD}). Reducing supply voltage while keeping a low leakage current and a reasonably high on-current is critical for minimizing energy consumption and continue Moore's law by helping with energy efficiency of computing. The thermal limit of the MOSFET transistor subthreshold swing (SS) restricts lowering its threshold voltage (V_t), causing significant performance degradation at low V_{DD}. A T-FET's SS is not limited by this thermal tail and may perform better at low V_{DD}.

Since the first experimental proof of SS $<$ 60 mV/decade, T-FET's prospects have attracted interest. Due to the large bandgap and larger carrier mass, Si T-FET has limited TFET performance. SiGe, Ge, and III–V materials for T-FETs attracted attention because of their low bandgap and carrier mass. While more challenging to fabricate, the broken bandgap hetero-junctions T-FETs eventually showed the highest T-FET on-current. Beyond III–V materials, transition metal dichalcogenide and other 2-D materials may provide a path in the future. Further progress in the T-FET fabrication process is needed for implementation in future semiconductor products.

This Special Topic of the IEEE JOURNAL ON EXPLORATORY SOLID-STATE COMPUTATIONAL DEVICES AND CIRCUITS (JXCDC) called for the most recent developments for recent T-FET device innovations and new ways of implementing its circuits for better energy-efficient computing. Here are the three articles that were accepted after the peer-review process.

1) Jo-Han Hung and coauthors from the National Chiao Tung University and National Taiwan University contributed an article titled "Digital Logic and Asynchronous Datapath With Heterogeneous TFET-MOSFET Structure for Ultralow-Energy Electronics," in which they investigate the use of SiGe low-bandgap epitaxial tunnel layer (ETL) TFET in circuits. They propose an optimum design of heterogeneous pMOS–NTFET dynamic logic gates and show how it may achieve lower power than CMOS during low-voltage operation.
2) Daniel Truesdell and coauthors from the University of Virginia contributed the article titled "Minimum-Energy Digital Computing With Steep Subthreshold Swing Tunnel FETs," in which they show that the optimal supply voltage for energy minimization and minimum energy is proportional to SS. They explore how device knobs and T-FET nonidealities affect the energy efficiency.
3) Shelly Garg and Sneh Saurabh from Indraprastha Institute of Information Technology (IIIT) Delhi contributed an article titled "Implementation of Boolean Functions Using Tunnel Field-Effect Transistors," in which they examine a novel way of implementing logic circuits using T-FET. With simulations, they show that a single T-FET device, in which two terminals are biased independently, can realize all primary two-input Boolean functions.

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UYGAR E. AVCI received the B.S. degree in physics and electrical engineering from Boğaziçi University, Istanbul, Turkey, in 1999, and the Ph.D. degree in applied physics from Cornell University, Ithaca, NY, USA, in 2005.

He is currently leading Advanced Device Research at Intel's Components Research. He has coauthored more than 40 journal papers and conference proceedings and has filed 100 patents. Currently, his group is responsible for delivering new transistor and memory device technologies with an eye toward bridging device-physics-based understanding, testing, and experimental realities to improve circuit power, performance, and scaling of semiconductor technology.

Dr. Avci was an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES. He is also the Committee Chair for IEDM Emerging Device and Compute Technology.

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