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Implementation of Boolean Functions Using Tunnel Field-Effect Transistors

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ABSTRACT Tunnel field-effect transistors (TFETs) are being examined as a possible replacement of MOSFETs for digital applications. However, TFETs have small ON-state current and, typically, exhibit reduced speed compared with conventional MOSFETs. Nevertheless, TFETs have some distinct characteristics that can be exploited for digital applications. In this article, using simulations, we show that a single device, in which two terminals are biased independently, can realize all primary two-input Boolean functions, such as AND, OR, NAND, NOR, XOR, and XNOR. By modifying the architecture of double-gate TFET (DGTFET) slightly and appropriately choosing device parameters, the Boolean functions AND, OR, NAND, NOR, and XNOR can be implemented. In addition, we propose a twin double-gate (TDG) TFET architecture, which can implement the inhibition functions $A'B$ and AB'. By suitably combining the inhibition functions, an XOR functionality can be obtained in a single device. These implementations demonstrate that the unique characteristics of TFET, such as ambipolar conduction and dependence of tunneling on the gate–source/drain overlaps, can be exploited to realize logic functions compactly.

INDEX TERMS Double-gate tunnel field-effect transistor (FET), independent gate control, ON-state current to OFF-state current ratio, twin double-gate (TDG) structure, two-variable Boolean functions.

I. INTRODUCTION

COMPLEMENTARY metal–oxide–semiconductor (CMOS) technology has been used over the past four decades to realize digital circuits since it provides excellent performance, extremely small standby power consumption, low cost, and good reliability characteristics [1]–[3]. However, the continued downscaling of device dimensions has caused the conventional metal–oxide–semiconductor field-effect transistor (MOSFET)-based devices to exhibit undesirable characteristics, such as high leakage current [4]–[6]. Consequently, the threshold voltage of the transistors and the supply voltage of the digital circuits cannot be further reduced in MOSFETs without degrading the performance and the energy efficiency. This is due to the limitation of the subthreshold swing of the MOSFET, which cannot be lower than 60 mV/decade at room temperature [6]–[8]. Therefore, researchers have been exploring devices based on different operating principles and exhibiting sub-60-mV/decade subthreshold swing [8]–[10]. Among these exploratory devices, tunnel FETs (TFETs) have attracted a great deal of attention [2], [8], [11]–[14]. Although the application of a TFET in digital circuits is challenging due to low ON-state current and a high ambipolar current, certain digital circuits, such as inverters, and arithmetic circuits have been demonstrated in the literature [6], [8], [14]–[17].

In this article, the implementation of Boolean functions, such as AND, OR, NAND, NOR, and XNOR, have been shown to be realized using a single double-gate TFET (DGTFET) requiring fewer transistors in comparison to the conventional CMOS-based implementations [18], [19]. It is shown that, when the architecture of a DGTFET is slightly modified, and the device parameters are appropriately chosen, the DGTFET can implement the required two-input Boolean functions. Furthermore, a twin DGTFET (TDG-TFET) structure has been shown to realize the inhibition functions $A'B$ and AB'. Using these inhibition functions, the implementation of the DGTFET-based XOR function is demonstrated.

The rest of this article is organized as follows. Section II explains the basic terminology related to this work and the simulation model. Section III describes how a DGTFET can realize the OR and NAND Boolean functions. Section IV describes how the gate–source overlap can help in minimizing I_{OFF} and obtaining AND and NOR Boolean functions. In Section V, the realization of the XNOR function is discussed. Section VI demonstrates how the proposed TDG-TFET can implement inhibition functions and be combined to obtain the XOR function. Section VII explains how transistors that exhibit complementary functions are combined to realize CMOS-type logic gates.

II. BASIC TERMINOLOGY AND SIMULATION MODEL

In this work, we treat the voltage V_{DD} (=0.5 V) and ground (=0 V) as logic "1" and logic "0," respectively. When the gates of the DGTFET are biased at logic A and B, respectively, the input to the function can be represented as "AB." Therefore, four possible inputs are "00," "01," "10," and "11." The drain current flowing through the device corresponding to the input "AB" is denoted as I_{AB}. In these logic function realizations, the magnitude of drain current I_{AB} flowing through the device depends on the input to the function ("AB") and is modulated in accordance with the intended functionality. Table S.1 shows the input to the functions and the corresponding current flowing through the device, I_{AB} in the Supplementary Material. When the expected output is logic "0" for the function, a low current flows through the DGTFET and is termed I_{OFF}, and when expected output is logic "1" for the function, a high current flows through the DGTFET and is termed I_{ON}. For DGTFET-based logic function realizations, it is desirable to achieve a sufficient I_{ON}/I_{OFF} ratio to differentiate between logic "0" and logic "1."

In this article, all simulations have been carried out using Atlas version 5.22.1.R [20]. A nonlocal band-to-band tunneling (BTBT) model has been used to compute the tunneling current [21]–[26]. We have considered the Fermi–Dirac statistics and bandgap narrowing effects (for highly doped regions). Furthermore, we have considered the Shockley–Read–Hall recombination model and the Lombardi mobility models in our simulations. We have calibrated the simulation model using [27], and the same simulation setup has been used in [18] and [28]. More detail of the simulation framework is given in the Supplementary Material.

III. REALIZING OR AND NAND BOOLEAN FUNCTIONS USING DGTFET

Fig. 1(a) shows the cross-sectional view of an n-type DGTFET. The top gate is called G_1, and the bottom gate is called G_2. Conventionally, the two gates are tied together to boost the ON-state current [6], [28]. However, in the DGTFET-based Boolean function implementation, the two gates are biased independently at the voltages: V_A and V_B.

In an OR function implementation, the BTBT should occur when one or both the inputs are at logic "1" (refer Table S.1 in the Supplementary Material). Therefore, a conventional n-type DGTFET with independent gate-control performs the OR Boolean function. Similarly, in a NAND function implementation, the BTBT should occur when one or both the inputs are at logic "0." Therefore, it can be realized using p-type DGTFET with independent gate control, as shown in Fig. 1(b). The device parameters used in the simulations for the DGTFET-based functions are listed in Table S.2 in the Supplementary Material.

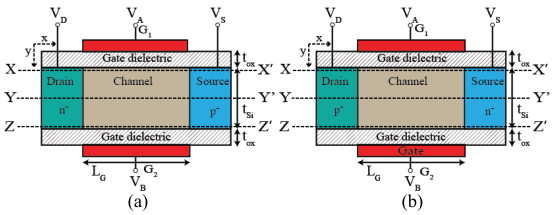

FIGURE 1. Cross-sectional view of (a) n-type DGTFET realizing OR Boolean function and (b) p-type DGTFET realizing NAND Boolean function.

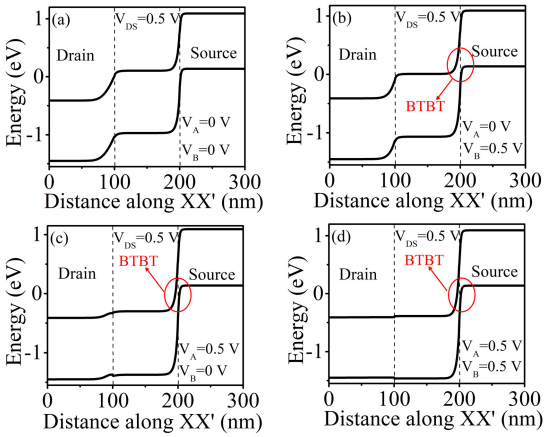

FIGURE 2. Band diagram of a DGTFET realizing OR Boolean function, along X-axis $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

Fig. 2 illustrates the band diagrams across the length of the device for DGTFET realizing OR Boolean function for different input combinations, showing that the BTBT is enabled in the "01," "10," and "11" cases. Fig. 3 illustrates the band diagrams across the length of the device for DGTFET realizing NAND Boolean function for different input combinations, showing that the BTBT is enabled in "00," "01," and "10" cases. Furthermore, the transfer characteristics of the DGTFET realizing OR function are shown in Fig. 4(a). The transfer characteristics of the DGTFET realizing NAND function are shown in Fig. 4(b). These realizations provide an I_{ON}/I_{OFF} ratio of $\sim 10^8$ at $V_{DD} = 0.5$ V.

It is worth pointing out that the I_{ON}/I_{OFF} ratio is sensitive to process-induced variations. For example, due to process-induced variations, the gates can shift creating underlap or overlap with the source. Using simulations, it is found that, when both the gates shift by 5 nm creating underlap with the

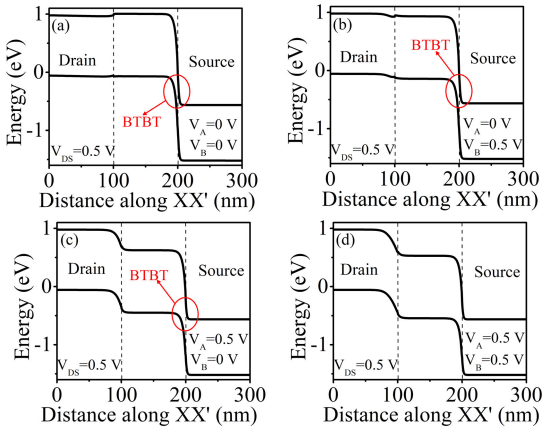

FIGURE 3. Band diagram of a DGTFET realizing NAND Boolean function, along *X*-axis $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

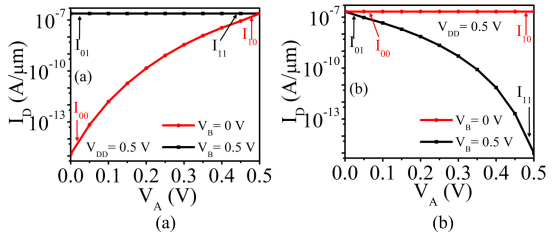

FIGURE 4. Transfer characteristics of DGTFET realizing (a) OR and (b) NAND Boolean functions.

source, the I_{ON}/I_{OFF} ratio reduces from 1×10^8 to 6×10^7. Similarly, when both the gates shift by 5 nm, creating overlap with the source, the I_{ON}/I_{OFF} ratio reduces from 1×10^8 to 1×10^7.

Moreover, it is important to examine the effect of change in gate length on the I_{ON}/I_{OFF} ratio. We notice that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 30$ nm and then decreases. However, the functionality remains intact for $L_G \geq 20$ nm though the I_{ON}/I_{OFF} ratio decreases to 1×10^7.

IV. REALIZING AND AND NOR BOOLEAN FUNCTIONS USING DGTFET

The AND function requires the BTBT to occur only when the input is "11." The DGTFET realizing OR conducts in the "01," "10," and "11" cases. Therefore, to obtain a DGTFET realizing AND function, there is a need to stop the conduction in "01" and "10" cases. For this, employing gate–source overlap has been suggested in [18]. Fig. 5 shows the band diagram of the DGTFET without gate–source overlap. It can be observed that tunneling is enabled near the gates (across the cutlines XX' and ZZ') at all bias conditions. We refer to the tunneling near the silicon–dielectric interface as the surface tunneling. However, tunneling occurs in the middle of the silicon body (across the cutline YY') when the input at both the gates (top gate and bottom gate) is high [see Fig. 5(d)]. We refer to the tunneling deep inside the silicon body as body

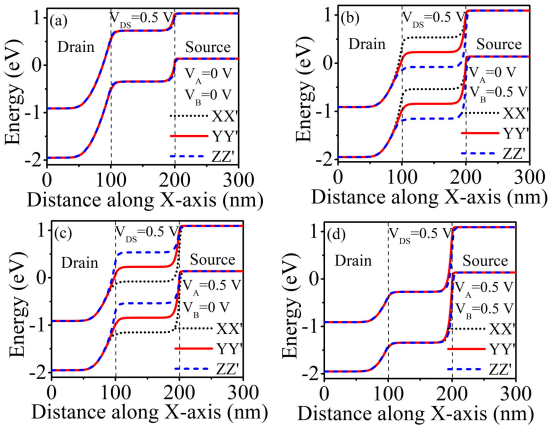

FIGURE 5. Band diagram along the *X*-axis for different cut lines, *XX′*, *YY′*, and *ZZ′*, at $V_{DS} = 0.5$ V without gate–source overlap, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

tunneling. These band diagrams suggest that, if we can inhibit the surface tunneling, then the tunneling current in the "01" and "10" cases will be negligible (since the body tunneling is not occurring at these bias conditions).

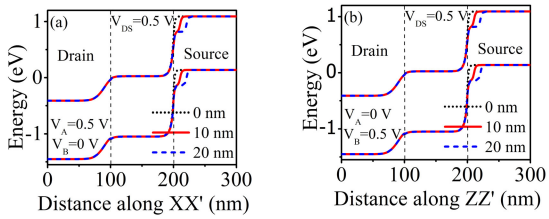

FIGURE 6. Band diagram of a DGTFET realizing AND Boolean function, along the *X*-axis at $V_{DS} = 0.5$ V with varying gate–source overlap from 0 to 20 nm, for input combinations: (a) "10" and (b) "01."

Fig. 6 shows that the addition of the gate–source overlap affects the band alignment of the device such that the surface tunneling (along the cutline XX' and ZZ') is inhibited. When $L_{ov} = 0$, the tunneling barrier width is low at the tunneling junction, as shown in Fig. 6. Therefore, a high I_{OFF} ($\sim 10^{-9}$ A/μm) flows through the device. As L_{ov} increases, the tunneling barrier width increases, and BTBT decreases, as shown in Fig. 6. However, when L_{ov} is increased beyond 20 nm, no further decrease in the drain current is observed. Therefore, $L_{ov} = 20$ nm is chosen to minimize the OFF-state current for the inputs "01" or "10." The cross-sectional view of the DGTFET performing the AND function is shown in Fig. 7. The device parameters used in the simulations for the DGTFET-based AND function are listed in Table S.2 in the Supplementary Material. The band diagrams for DGTFET realizing AND Boolean function across the length of the device for different input combinations are shown in Fig. 8, illustrating that the BTBT is enabled for the "11" case.

The transfer characteristics of the DGTFET performing AND function is shown in Fig. 9. The I_{ON}/I_{OFF} ratio of orders $\sim 10^7$ at $V_{DD} = 0.5$ V is observed. Furthermore, it is important to analyze the impact of silicon body thickness (t_{si}) on

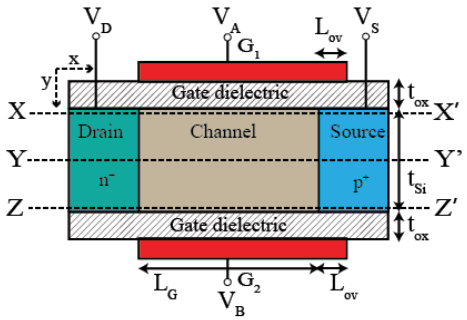

FIGURE 7. Cross-sectional view of DGTFET realizing AND Boolean function [18].

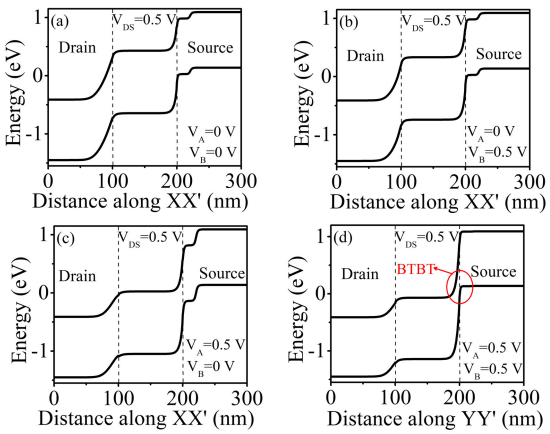

FIGURE 8. Band diagram of a DGTFET realizing AND Boolean function, along the *X*-axis at $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

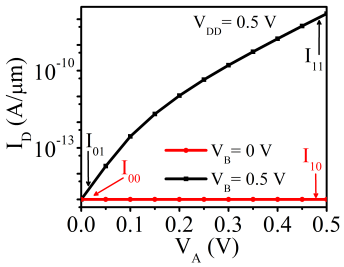

FIGURE 9. Transfer characteristics of DGTFET realizing AND Boolean function.

the electrical characteristics of the DGTFET that realizes the AND logic function. It is found that, as t_{si} increases, the body tunneling decreases since the impact of the gate bias inside the silicon body becomes weak. This leads to an increase in the tunneling barrier width, as shown in Fig. 10. Since the tunneling barrier width increases, the BTBT and I_{ON} decreases. This, leads to undesirable degradation in the I_{ON}/I_{OFF} ratio. Therefore, a high t_{si} is not preferred for a DGTFET that realizes the AND function. Nevertheless, t_{si} cannot be too low since the gate–source overlap inhibits BTBT throughout the silicon body. Therefore, for a reasonable I_{ON}/I_{OFF} ratio, a $t_{si} \sim 10$ nm is chosen.

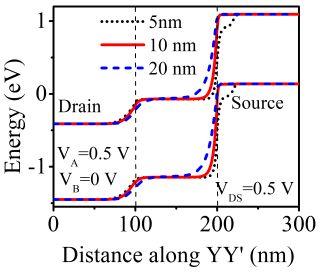

FIGURE 10. Band diagram of a DGTFET realizing AND Boolean function, along the *X*-axis at $V_{DS} = 0.5$ V, for input combinations "11" with varying t_{si}.

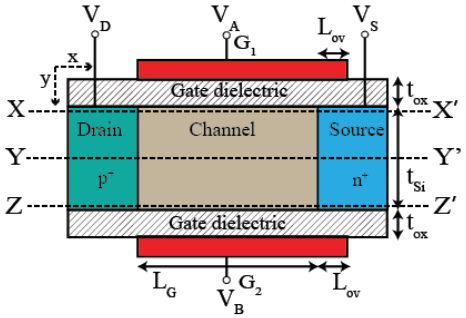

FIGURE 11. Cross-sectional view of DGTFET realizing NOR Boolean function.

The NOR Boolean function requires the BTBT to occur only when the input is "00." The DGTFET realizing OR conducts in the "00," "01," and "10" cases. Therefore, to obtain a DGTFET realizing NOR function, there is a need to stop the conduction in the "01" and "10" cases. For this, the technique of gate–source overlap can be used, as described earlier. Therefore, the gate–source overlap is added to the DGTFET to obtain NOR function, as shown in Fig. 11. The device parameters used in the simulations for the DGTFET-based NOR function are listed in Table S.2 in the Supplementary Material. The band diagrams of the DGTFET realizing NOR Boolean function are shown in Fig. 12, showing that the BTBT is enabled only in the "00" case. The transfer characteristics of the DGTFET performing NOR function are shown in Fig. 13. The I_{ON}/I_{OFF} ratio of $\sim 10^7$ at $V_{DD} = 0.5$ V is observed.

We also studied the effect of change in the gate–source overlap due to process-induced variations. We found that, when the gate–source overlap changes by ± 5 nm, the I_{ON}/I_{OFF} ratio is not significantly impacted.

We also examine the effect of the change in the gate length on the I_{ON}/I_{OFF} ratio. We noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 30$ nm and then decreases. However, the functionality remains intact for $L_G \geq 20$ nm though the I_{ON}/I_{OFF} ratio decreases to 5×10^5. Furthermore, the functionality remains intact till $L_{ov} = 10$ nm with an I_{ON}/I_{OFF} ratio of 5×10^6 at $L_G = 30$ nm. When $L_{ov} < 10$ nm, the I_{ON}/I_{OFF} ratio starts decreasing sharply, and the functionality is lost.

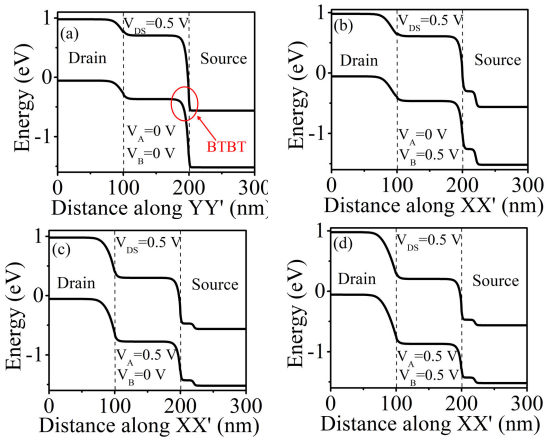

FIGURE 12. Band diagram of a DGTFET realizing NOR Boolean function, along the X-axis $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

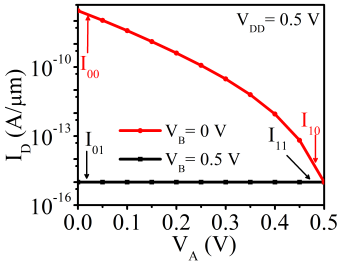

FIGURE 13. Transfer characteristics of DGTFET realizing NOR Boolean function.

V. REALIZING XNOR BOOLEAN FUNCTION USING DGTFET

The XNOR Boolean function requires the BTBT to occur when the input is either "00" or "11" and to be inhibited when the input is either "01" or "10." The inhibition of the BTBT in the device can be achieved by using the gate-overlap technique. When the input is "00," BTBT can be enabled using p-type DGTFET as in the NOR function realization. Similarly, when the input is "11," BTBT can be enabled using n-type DGTFET as in the AND function realization. Therefore, to obtain an XNOR function, a p-TFET and an n-TFET are required. However, to avoid using two devices, we propose to exploit the ambipolar conduction of the TFET. By using dual-material gate (DMG) and suitable work functions ϕ_1 and ϕ_2, tunneling occurs at the source–channel junction in the "11" case (as in the AND function) and the drain–channel junction (due to ambipolar conduction) in the "00" case (as in the NOR function). Moreover, since tunneling is occurring at the source–channel junction and the drain–channel junction, in addition to the gate–source overlap, we employ the gate–drain overlap to inhibit the surface tunneling in the "01" and "10" cases.

The DGTFET realizing the XNOR function is shown in Fig. 14. The device parameters used in the simulations for the DGTFET-based XNOR function are listed in Table S.2 in the Supplementary Material. Fig. 15 illustrates the band diagrams across the length of the device for different input combinations, showing that the BTBT is enabled in the "00" and "11" cases. The transfer characteristics of the DGTFET realizing the XNOR function are shown in Fig. 16. The I_{ON}/I_{OFF} ratio for this implementation is $\sim 10^7$ at $V_{DD} = 0.5$ V.

For the proposed XNOR function, the gate–source and gate–drain overlaps can change due to process-induced variations. We found that, when the gate–source and gate–drain overlaps are changed by ± 5 nm, the I_{ON}/I_{OFF} ratio is not significantly impacted. Moreover, the functionality remains intact till $L_{ov} = 10$ nm with an I_{ON}/I_{OFF} ratio of 5×10^6.

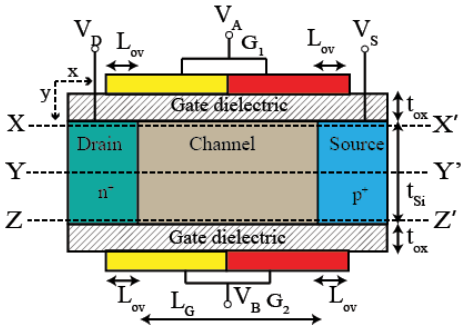

FIGURE 14. Cross-sectional view of DGTFET realizing XNOR Boolean function.

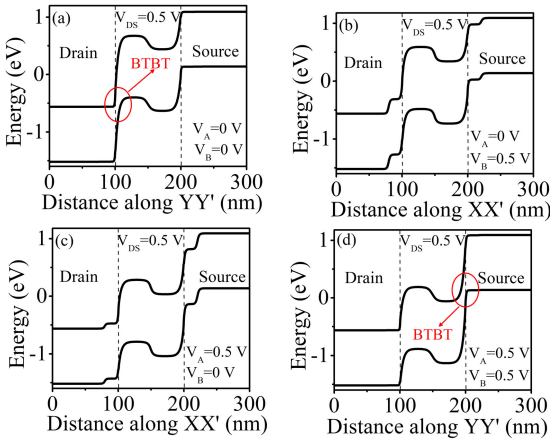

FIGURE 15. Band diagram of a DGTFET realizing XNOR Boolean function, along the X-axis $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11."

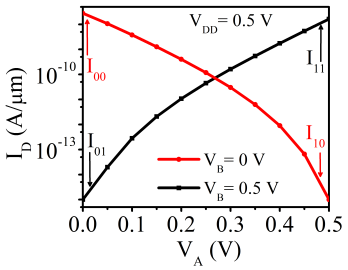

FIGURE 16. Transfer characteristics of DGTFET realizing XNOR Boolean function.

For $L_{ov} < 10$ nm, the I_{ON}/I_{OFF} ratio decreases sharply, and the functionality is lost.

Moreover, we examine the effect of change in the gate length on the I_{ON}/I_{OFF} ratio. It is noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 40$ nm and then decreases. However, the functionality remains intact for $L_G \geq 30$ nm though the I_{ON}/I_{OFF} ratio decreases to 1×10^6.

VI. REALIZING XOR BOOLEAN FUNCTION USING DGTFET

The XOR Boolean function requires that BTBT occurs when the input is "01" or "10" and be inhibited when input is "00" or "11"'. In all the abovementioned implementations, we have inhibited tunneling in the "01" and "10" cases using the gate–source or gate–drain overlaps. However, for XOR function, the tunneling needs to be maximized in the "01" and "10" cases. This requirement is opposite to the functions realized earlier. Therefore, the XOR function cannot be realized using earlier described techniques. We propose to realize the XOR function ($A \oplus B = A'B + AB'$) as the combination of inhibition functions $A'B$ and AB' [1], [3].

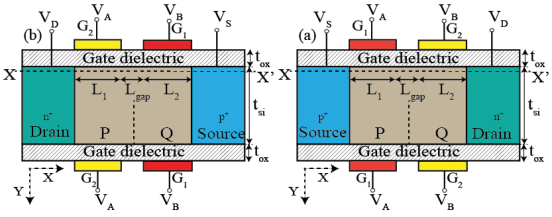

FIGURE 17. Cross-sectional view of a TDG-TFET that realizes inhibition function. (a) $A'B$. (b) AB'.

A. REALIZING INHIBITION FUNCTIONS USING DGTFET

Fig. 17(a) shows the cross-sectional view of the proposed TDG-TFET in which there are two gates at the top called G_1 and G_2, separated by a gap L_{gap}. Similarly, there are two gates at the bottom corresponding to the top gates G_1 and G_2. Thus, a twin double-gate (TDG) structure is formed. The gates G_1 and G_2 are made up of different materials, with workfunctions ϕ_1 and ϕ_2, respectively. The key aspect of a TDG-TFET is that the twin gates are able to modulate the BTBT at their interfaces as per the required functionality. The structure can be fabricated using the techniques reported in [28], [33], and [34].

First, we explain the function of a TDG-TFET realizing $A'B$, as shown in Fig. 17(a). For easier explanation, the channel is divided into two regions: P and Q. The workfunction ϕ_1 is chosen such that the region P becomes p-type (rich in holes) when $V_A = 0$ and is depleted when $V_A = V_{DD}$. Similarly, the workfunction ϕ_2 is chosen such that the region Q becomes n-type (rich in electrons) when $V_B = V_{DD}$ and is depleted when $V_B = 0$. The electron and the hole concentrations for different input combinations are shown in Fig. 18. For the input combination "01," the region P is rich in holes, and

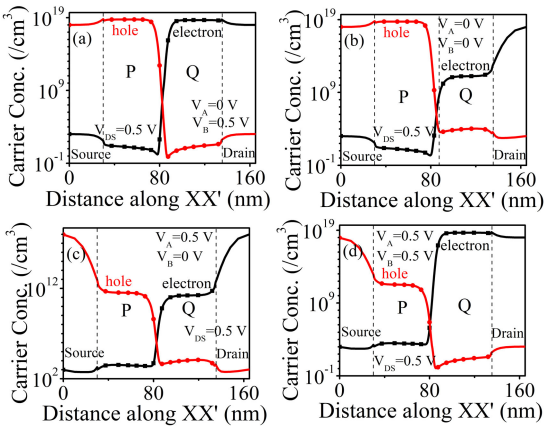

FIGURE 18. Carrier Concentrations of a DGTFET realizing "$A'B$" Boolean function, along the X-axis at $V_{DS} = 0.5$ V, for input combinations: (a) "01," (b) "00," (c) "10," and (d) "11."

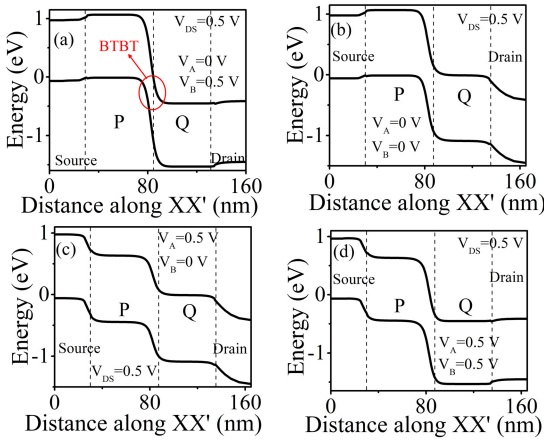

FIGURE 19. Band diagram of a DGTFET realizing "$A'B$" Boolean function, along the X-axis at $V_{DS} = 0.5$ V, for input combinations: (a) "01," (b) "00," (c) "10," and (d) "11."

the region Q is rich in electrons, as shown in Fig. 18(a). Therefore, the conduction and the valence bands get aligned, and the BTBT is enabled at the boundary of regions P and Q, as shown in Fig. 19(a). For the other three input conditions, either region P or Q or both remain depleted, as shown in Fig. 18(b)–(d). Thus, BTBT is inhibited under the other three input conditions, as illustrated in Fig. 19(b)–(d).

The transfer characteristics of a TDG-TFET realizing $A'B$ is shown in Fig. 20(a). Furthermore, the other inhibition function AB' can be realized just by interchanging the inputs at the gates G_1 and G_2, as shown in Fig. 17(b). The transfer characteristics of a TDG-TFET realizing AB' is shown in Fig. 20(b).

By combining TDG-TFETs that realize $A'B$ and AB', XOR can be implemented, as shown in Fig. 21. For compactness, the source of the TDG-TFETs is shared. The device parameters used in the simulations for the DGTFET-based XOR function are listed in Table S.2 in the Supplementary Material. Fig. 22 illustrates the band diagrams across the length of the device for different input combinations, showing

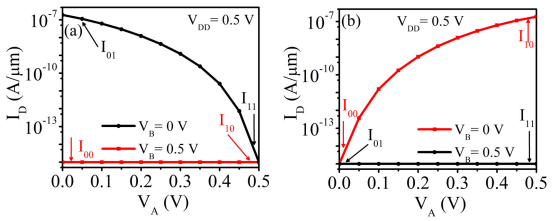

FIGURE 20. Transfer characteristics of a TDG-TFET realizing (a) $A'B$ and (b) AB'.

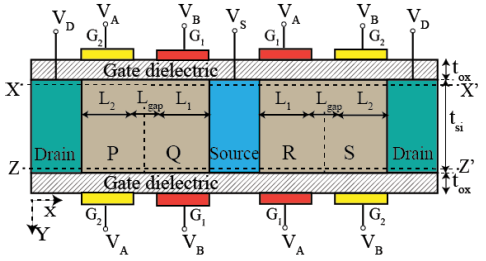

FIGURE 21. Cross-sectional view of TDG-TFET realizing XOR Boolean function.

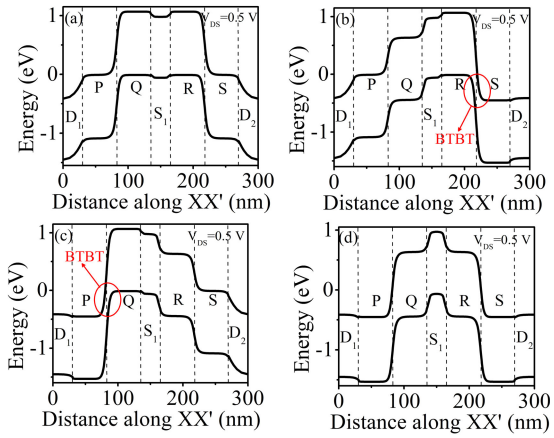

FIGURE 22. Band diagram of a DGTFET realizing XOR Boolean function, along the X-axis at $V_{DS} = 0.5$ V, for input combinations: (a) "00," (b) "01," (c) "10," and (d) "11" (drain1, source, and drain2 have been indicated as D_1, S_2, and D_2, respectively, in these figures.).

that the BTBT is enabled in the "01" and "10" cases. The transfer characteristics of the proposed XOR function is shown in Fig. 23. The I_{ON}/I_{OFF} ratio is observed to be 2×10^8 at $V_{DD} = 0.5$ V.

Furthermore, it is important to note that the process-induced variations can change the gap L_{gap} between the gate electrodes G_1 and G_2 in the device. When L_{gap} increases to 10 nm, the I_{ON}/I_{OFF} ratio reduces from 2×10^8 to 5×10^6. This decrease is due to the decrease in the sharpness of the band diagram profiles at the tunneling junctions.

Moreover, we examine the change in the I_{ON}/I_{OFF} due to the change in the gate length. We notice that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 30$ nm and then decreases. However, the functionality remains intact for $L_G \geq 20$ nm though the I_{ON}/I_{OFF} ratio decreases to 1×10^7.

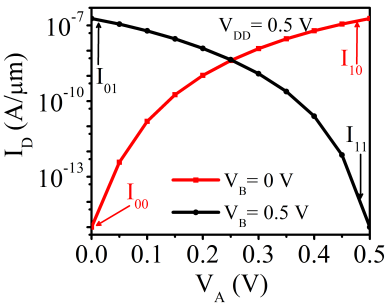

FIGURE 23. Transfer characteristics of DGTFET realizing XOR Boolean function.

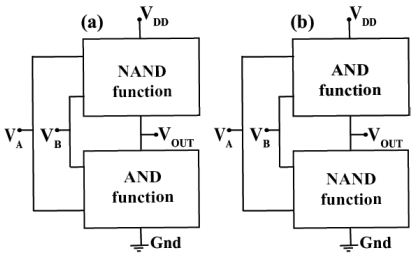

FIGURE 24. Schematic of DGTFET-based (a) NAND gate, (b) AND gate.

VII. IMPLEMENTING LOGIC GATES

Using the Boolean function implementations proposed in Sections III–VI, we demonstrate that CMOS-type two-input logic gates can be implemented in a compact manner. It can be noted that the six Boolean functions proposed in the previous sections form three complementary pairs: AND–NAND, OR–NOR, and XOR–XNOR. These complementary Boolean functions can be used in the pull-up and pull-down configurations to realize CMOS-type two-input logic gates, as shown in Fig. 24. For instance, when the pull-up configuration is the NAND function and the pull-down configuration is the AND function, the circuit works as a CMOS-type NAND gate. When either of the two inputs is at logic "0," then the current flows through the NAND function (a low-resistance path exists between V_{DD} and the output node), and the output is pulled up to logic "1." However, when both the inputs are at logic "1," the current flows through the AND function (a low-resistance path exists between Gnd and the output node), and the output is pulled down to logic "0." Note that, due to the complementary functionality, when the pull-up transistor is switched on, the pull-down transistor is switched off, and vice versa. Thus, the outputs of the proposed two-input gates are always connected to V_{DD} or Gnd through a low-resistance path, similar to CMOS logic gates. The static characteristics of the NAND gate are shown in Fig. 25. Similarly, all other two-input logic gates can be obtained using these Boolean function implementations. These implementations employ fewer transistors than the conventional CMOS implementation of logic gates. Therefore, the proposed implementations are more compact and are expected to reduce equivalent load capacitance.

The performance metrics of the proposed implementations are listed in Table 1. We have used the effective drive current

TABLE 1. Performance metrics of the DGTFET-based Boolean functions.

Function	V_{DD} (V)	I_{ON} $(A/\mu m)$	I_{ON}/I_{OFF}	C_{GG} $(fF/\mu m^2)$	Delay (ns)
OR	0.5	2.4×10^{-7}	10^8	3.5	12
NAND	0.5	2.0×10^{-7}	10^8	1.5	4
AND	0.5	1.6×10^{-8}	10^7	1.5	50
NOR	0.5	2.8×10^{-8}	10^7	1.5	25
XNOR	0.5	2.0×10^{-8}	10^7	1.5	45
XOR	0.5	1.8×10^{-7}	10^8	2.5	10

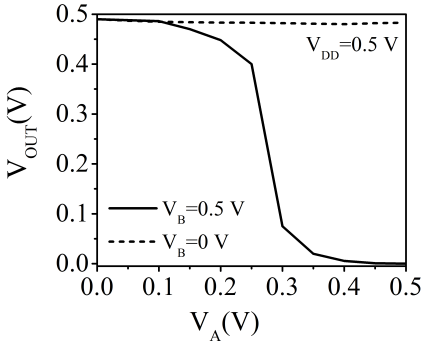

FIGURE 25. Static characteristics of DGTFET realizing NAND gate.

method proposed in [35] to estimate the delay of these implementations. However, to accurately compute and compare the performance of the proposed implementation with the CMOS-based implementations, more rigorous analysis based on transient simulations is required [18], [19]. The delays of the proposed implementations presented in Table 1 are very high compared with the state-of-the-art CMOS logic gates. This is expected since the abovementioned implementations are obtained using Si-based TFETs, and it is well known that Si-based TFET circuits exhibit higher delay due to low I_{ON} and high C_{GD} [13], [18], [19], [36], [37]. Nevertheless, it is important to mention that this article does not claim that the proposed realizations can outperform the state-of-the-art CMOS logic gates in terms of performance. However, in the future, the techniques demonstrated in this work can possibly be adapted to TFETs that exhibit higher I_{ON} and that compete with CMOS.

It is worth pointing out that, in this work, we have only considered two-input logic gates. However, for practical applications, implementing Boolean functions of more input variables is necessary. Using the devices proposed in this work, stacked and cascaded implementations of the Boolean functions are possible.

Fig. 26(a) illustrates how a four-input AND gate can be implemented by stacking four transistors. Though the abovementioned implementation is functionally correct, there are several challenges in the stacked implementation. For a large number of inputs, the delay will significantly increase due to the resistances of the series transistors, the capacitance of the internal nodes, increased input capacitance, and self-loading effects. In TFET implementations, we need to additionally consider the impact of increased C_{GD}, including Miller effects and low ON-state current [37],

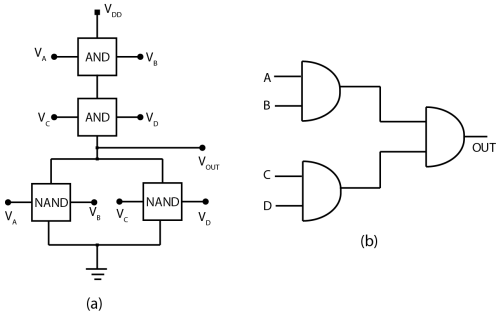

FIGURE 26. Four-input AND gate. (a) Stacked implementation. (b) Cascaded implementation.

[38]. Fig. 26(b) illustrates how a four-input AND gate can be implemented by cascading two-input AND gates. This implementation will require six transistors (two transistors for each AND gate), which is still less than the traditional CMOS implementation that requires ten transistors. Though the proposed implementations consume fewer transistors, there are several nontrivial challenges in these implementations. We can observe from Table 1 that the transistors providing complementary functions are not fully balanced. This can result in noise margin reduction, asymmetric rise/fall delays, output logic levels degradation, and increased power consumption in the subsequent logic gates [39]. Balancing the complementary devices is challenging due to the dependence of subthreshold swing on the gate voltage [38]. It can incur additional area, increase input capacitance, and impact the delay of the preceding gate. In addition, when TFETs are cascaded, high settling time, output voltage degradation, and susceptibility to crosstalk become important due to superlinear onset of saturation in the output characteristics, ambipolar conduction, dominant C_{GD}, and high ON-state resistance [17], [37], [40]. We need to address these problems in the proposed implementation also.

VIII. CONCLUSION

In this article, we have demonstrated that the unique characteristics of TFET, such as ambipolar conduction and dependence of BTBT on the gate–source/drain overlaps, can be exploited to realize logic functions compactly. It is worth pointing out that many researchers have proposed to eliminate ambipolar current and make TFETs similar to MOSFETs for digital applications. However, in this work, we have shown that distinct electrical characteristics of TFETs can be exploited, and certain differences with MOSFETs can be tolerated for useful applications. Though low ON-state current of TFETs remains a primary concern for researchers, novel circuit applications are possible using TFETs.

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