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Digital Logic and Asynchronous Datapath With Heterogeneous TFET-MOSFET Structure for Ultralow-Energy Electronics

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ABSTRACT The tunnel field-effect transistor (TFET) is a promising solution for high energy-efficient circuits. Based on the band-to-band tunneling (BTBT) condition, fast switching characteristic with a steep subthreshold swing (SS) in the ultralow-voltage operation is feasible. Our prior work has demonstrated that the SS and ON-state current can be improved without leakage current penalty through the usage of SiGe low-bandgap material in the epitaxial tunnel layer (ETL). ETL-TFET is highly compatible with the CMOS process, enabling heterogeneous integration of TFET and MOSFET in the same technology. In this work, the circuit performance of ETL-TFET and fully depleted SOI (FDSOI) MOSFET is evaluated and compared in terms of energy and delay metrics. By combining the advantages of TFET and MOSFET, heterogeneous pMOS-NTFET dynamic logic gates are proposed. The pMOS-NTFET-based logic gates demonstrate the lowest energy consumption than other realizations. Asynchronous datapath is leveraged to combat the timing variations in the ultralow-voltage region. A 20.9%–33.9% energy reduction is achieved compared with the conventional MOSFET counterpart.

INDEX TERMS Band-to-band (BTBT) tunneling, epitaxial tunnel layer (ETL) tunnel field-effect transistor (TFET), heterogeneous integration, low-energy logic, SiGe low-bandgap material.

I. INTRODUCTION

HIGH energy-efficient circuits have become an important topic over the past years. The battery lifetime, rather than speed performance, has become the main concern in numerous applications, especially for implantable and wearable devices. Circuit energy is divided into dynamic energy and leakage energy. Given a supply voltage V_{DD}, the dynamic energy consumption is proportional to V_{DD}^2. Therefore, scaling of V_{DD} becomes an efficient and commonly used way to significantly reduce energy dissipation. However, the subthreshold swing (SS) of the conventional metal–oxide–semiconductor field-effect transistor (MOSFET) device is limited to 60 mV/decade at room temperature. To maintain circuit performance through supply scaling, the threshold voltage should be scaled down accordingly, which induces a large penalty of leakage energy loss. On the other hand, low-voltage operation slows down the circuit speed. The leakage energy consumption also increases drastically.

Tunnel field-effect transistor (TFET) is a promising solution for ultralow-voltage operation [1]–[3]. Due to the unique band-to-band tunneling (BTBT) conduction mechanism, the steep SS lower than 60 mV/decade can be achieved [4]. However, the BTBT and the gate-to-drain lapping structure [5] result in a low on-state current and limits the TFET-based circuit applications. Furthermore, because of inefficient BTBT, the uni-directional and low on-state current is the main concern of TFET applications [6]. Also, the severe degradation of current is observed from the stacking of TFET devices. Many researchers have been devoted to enhance the BTBT conduction current with low-bandgap materials in the source region or in the whole channel region [7]–[9] or using the hybrid TFET-MOSFET topologies [10]–[12] to have both benefits of MOSFET and TFET. In our previous

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work, an epitaxial tunnel layer (ETL) TFET was proposed with the low-bandgap SiGe/Si heteromaterial used at ETL and the substrate region to further boost the BTBT and maintain the extremely low leakage current [13]. The performance of ETL-NTFET is much better than ETL-PTFET and the large difference between the two devices stems from the band alignment and the TFET operation mechanism [14]. It is also noted that the offset in the valance band can suppress the low-field BTBT and result in a better SS. A device with a better swing by employing the ETL band engineering design can achieve better performance at the low V_{DD} regime (see [14] for details).[1] Due to its compatibility with conventional complementary metal–oxide–semiconductor (CMOS) technology, ETL-TFET allows the heterogeneous integration with MOSFET.

Synchronous circuits are still the mainstream design style in VLSI implementation. However, when V_{DD} scales down to the subtherhold region, the reliability of synchronous circuits will be challenged. Conventional synchronous pipeline structure suffers from high delay sensitivity to the process, voltage, and temperature (PVT) variations in the low-voltage region. Therefore, a large delay margin in a clock cycle should be taken into consideration, which induces large leakage power penalty. To combat the timing variations due to PVT variations, asynchronous circuits are proposed for process-tolerant and energy-efficient subthreshold operation [16].

In this work, based on the characteristics of ETL-TFET device, heterogeneous asynchronous pipeline architecture in the subthreshold operation is proposed to maximize the utilization of the ETL-TFET device. Asynchronous datapath for field-programmable gate array (FPGA) fabric [17] with regular pipelined logic blocks is presented to demonstrate the heterogeneous circuit performance. The asynchronous pipeline stage consists of a precharge transistor, a gating transistor, and an n-type pull-down network. The circuit operation is divided into two phases, precharge and evaluation, which solves the problem from device asymmetry in complementary logic operation. Superior ETL-NTFET can further improve the performance of n-type network computation. Asynchronous circuits with higher delay tolerance can also improve the reliability in the ultralow-voltage region.

The rest of this article is organized as follows. Section II describes the transistor characteristics of the ETL-TFET device. Heterogeneous integration of TFET and MOSFET is presented in Section III. Section IV presents an asynchronous datapath structure with the proposed pMOS-NTFET dynamic logic gates. Finally, Section V concludes this article.

[1] A qualitative discussion on the effect of quantum confinement has been disclosed in [13] and [14]. The main impact of the quantization effect would be the shift of the device onset voltage. This onset voltage shift could be corrected by work function modulation and will not affect the simulated results in this work. The quantization effect becomes stronger as the gate voltage increases so that the SS behavior would degrade. However, due to the lack of elaborate models to take the correlation between the discrete quantized level and BTBT into account in 2-D structure, the effect of quantum confinement is not considered in this work.

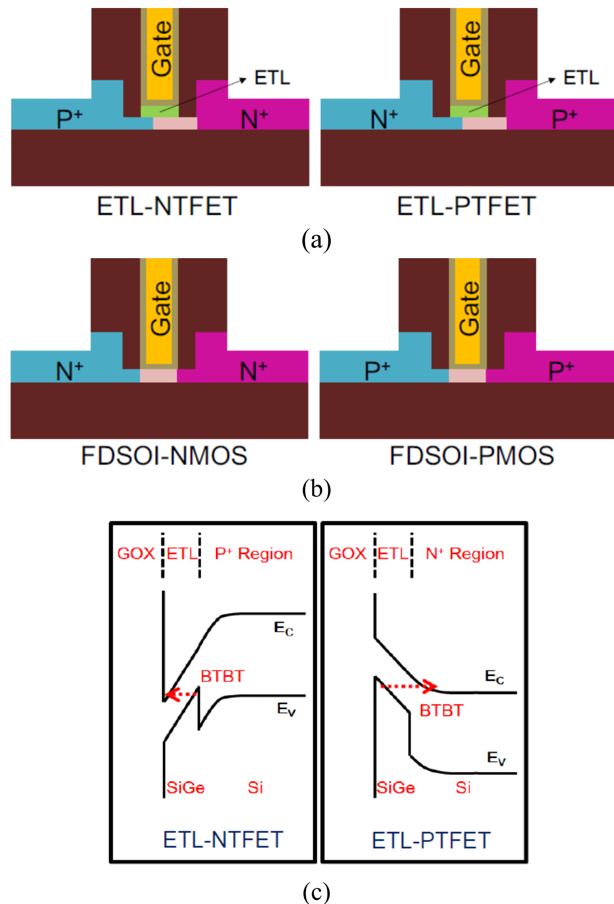

FIGURE 1. **(a) Structure of ETL-TFET. (b) Structure of FDSOI-MOSFET. (c) ON-state band diagrams of ETL-TFET.**

II. CHARACTERISTICS OF ETL-TFET

Fig. 1(a) shows the ETL-TFET structure [13] discussed in this work. The SiGe material is applied to the ETL and Ge content is set at 80%. In order to make a performance comparison with MOSFET technology, the fully depleted SOI (FDSOI) MOSFET [18] is used, as shown in Fig. 1(b). For SiGe epitaxy, it is highly related to the interface quality. Because the ETL is on the channel surface of an FDSOI substrate, it is believed that the epitaxy capability can follow the general critical thickness and Ge percentage trend. Therefore, 80% Ge with very thin ETL layer (<5 nm) is feasible. Fig. 1(c) shows the ON-state band diagrams of the PTFET and NTFET with cross section. The ON-state BTBT is occurred at the gate-to-source and drain overlap region for NTFET and PTFET, respectively. Therefore, the low-bandgap material used in ETL can boost the BTBT efficiency. The important device and simulation parameters of ETL-TFET and FDSOI-MOSFET are listed in Table 1. The physical model of device is constructed by the commercial package TCAD [19]. The recombination SRH model, mobility model, and Fermi–Dirac statics are all included. Conduction current and parasitic capacitance characteristics of device are extracted through TCAD mixed-mode simulation [15]. Device module is created by Verilog-A [20], [21] with 2-D tables, including

TABLE 1. Structure parameters of ETL-TFET and FDSOI-MOSFET.

	NTFET	PTFET	NMOS	PMOS
Gate Length (nm)	30	30	30	30
Channel Thickness (nm)	10	10	10	10
Channel Doping Concentration (cm^{-3})	1E16	1E16	1E17	1E17
ETL-Layer Thickness	4nm SiGe + 1nm Si	4nm SiGe	NA	NA
EOT (nm)	1	1	1	1
Source/Drain Overlap (nm, nm)	15, 0	15, 0	0, 0	0, 0

I_{DS} (V_{DS} and V_{GS}), C_{GS} (V_{GS} and V_{DS}), and C_{GD} (V_{GS} and V_{DS}) [22]. The symbols referred here are drain-to-source current (I_{DS}), gate/drain-to-source bias (V_{GS} and V_{DS}), and parasitic gate-to-drain/source capacitance (C_{GD} and C_{GS}). The Verilog-A models are then integrated into the analog design environment to perform complex circuit simulations.

Based on the International Technology Roadmap for Semiconductors (ITRS) [23], the low operating power (LOP) and the low standby power (LSTP) applications for 30-nm ETL-TFET and 30-nm FDSOI-MOSFET are evaluated with drain-to-source current (I_{DS}) versus gate-to-source (V_{GS}) transfer characteristics, as shown in Fig. 2. Under the LOP constraint, the TFET device does not show the superiority of SS but has a relatively weak ON-state current. The advantageous operation range of TFET is limited between 0 and 0.15 V. On the contrary, under the LSTP constraint, the maximum ON-state current of the TFET can be 180× and 20× higher than that of FDSOI-MOSFET for n-type and p-type devices, respectively. The advantageous operation range of TFET can be extended to 0.5 V. In this work, the circuit performance is discussed for the LSTP applications. The turn-off current (I_{OFF}) in both TFET and MOSFET is set to 10 pA/μm through the gate work function modulation. The steep SS is distinctly observed in the ETL-TFETs as the gate-to-source voltage is below 0.2 V. The average (in the range of 10 pA–0.1 μA) SSs of the NTFET and the PTFET are 36 and 58 mV/decade, respectively. The improved average SS of the NTFET is attributed to the ETL band engineering. Regarding the operation of the ETL-NTFET, the low electric field BTBT from the valence band of the P+ region to the conduction band of the ETL is suppressed due to the valence band offset from the SiGe/Si heteromaterial system. As the high electric field BTBT occurred in the ETL is maintained, the average SS is further improved through the suppression of the low-electric-field BTBT.

C_{GD} of the device plays an important role when considering energy dissipation and circuit delay. The impact of the capacitance in the ETL-TFET is magnified due to the C_{GD}-dominated Miller effect [24]. In this work, C_{GD} of ETL-TFET and MOSFET is included in the gate capacitance shown in Fig. 3. Fig. 3(a) shows the capacitance characteristics of the devices. As can be seen, the ETL-TFETs have larger gate capacitance than MOSFETs. It is because a sufficient gate-to-source overlap length is necessary for the ETL-TFET to boost the BTBT current. In addition, the ON-state BTBT current of the TFET occurs in the inversion region, but the

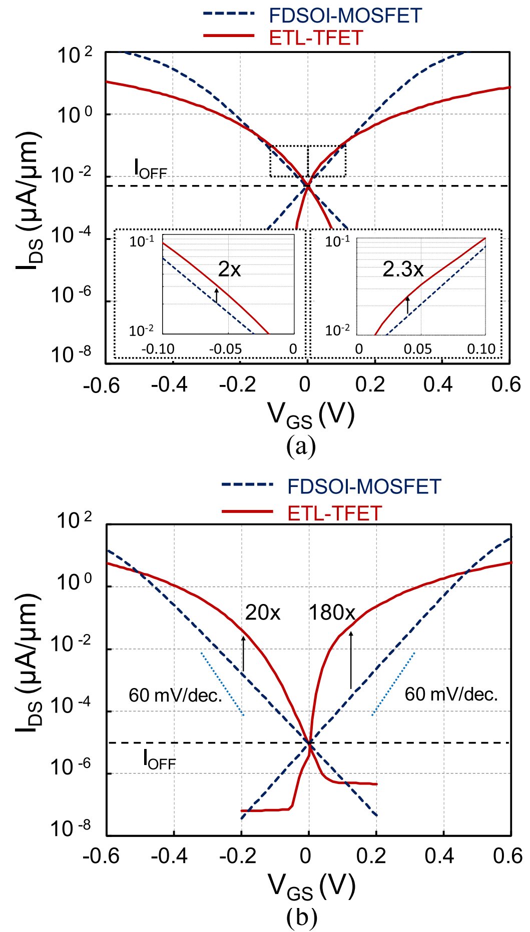

FIGURE 2. I_{DS}–V_{GS} **characteristics at** V_{DS} **= 0.5 V for ETL-TFET and FDSOI-MOSFET with the different** I_{OFF}**. (a) LOP (**I_{OFF} **= 5 nA/**μ**m). (b) LSTP (**I_{OFF} **= 10 pA/**μ**m).**

MOSFET is operated in the subthreshold region and the channel is in the depletion region. A strong, negative V_{DS} dependence of the gate capacitance is also observed. This causes significant speed degradation, which characterized by an RC delay when the circuit is operated in an ultralow-voltage region.

As the complementary logic is the mainstream digital logic, the impact of the gate/drain capacitance is evaluated using a fan-out-1 (FO1) inverter. Fig. 3(b) shows the effective input capacitance of an FO1 inverter for both TFET and MOSFET devices. Due to the larger parasitic capacitance of device, the TFET inverter has a 1.7× to 3× larger input capacitance than MOSFET. The input capacitance of the TFET inverter also has a relatively larger variation when $V_{DD} < 0.25$ V. At $V_{DD} = 0.15$ V, the input capacitance of the TFET is 3× larger than that of the MOSFET counterpart.

III. HETEROGENEOUS TFET-MOSFET LOGIC STRUCTURE

To combat the increased capacitance of TFET, dynamic logic is explored to improve the speed performance. The aforementioned ETL-TFET is fully compatible with the

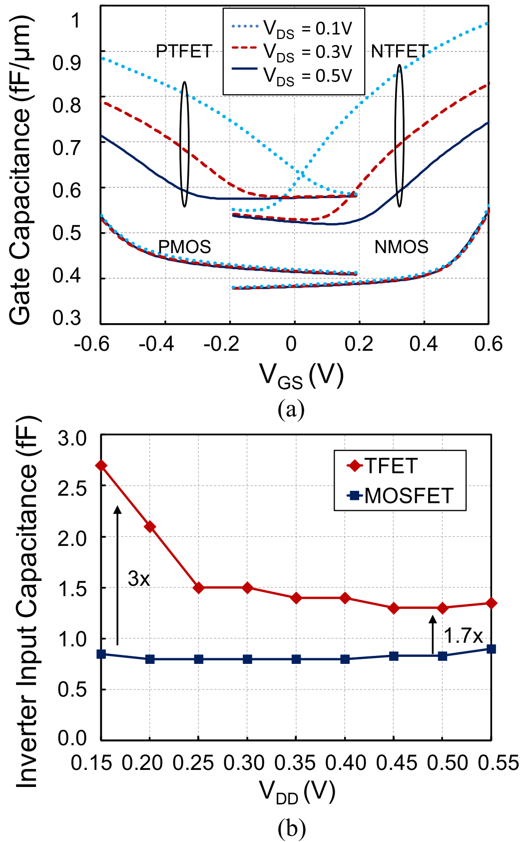

FIGURE 3. (a) Gate capacitance versus supply voltage for ETL-TFET and FDSOI-MOSFET with different V_{DS}s. (b) Input capacitance of an FO1 inverter with varying supply voltages.

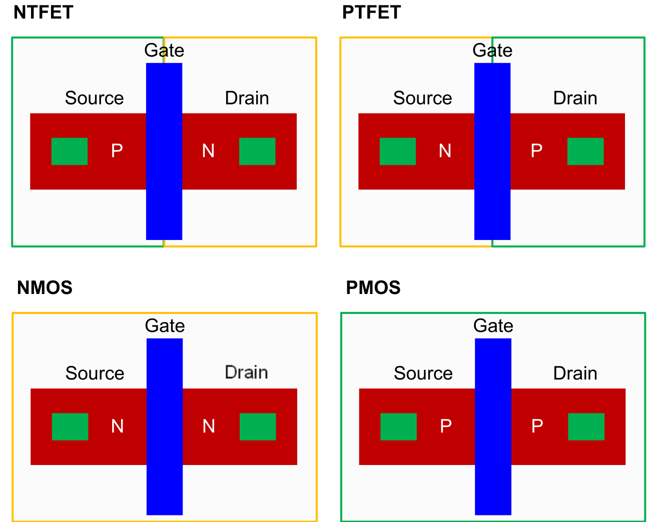

FIGURE 4. Layout of nMOS, pMOS, NTFET, and PTFET devices.

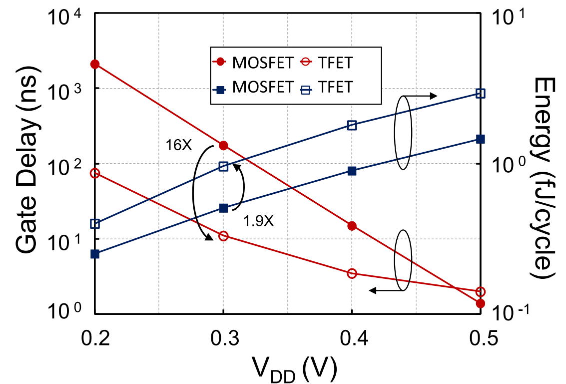

FIGURE 5. Delay and transition energy of FO4 inverter realized by both TFET and MOSFET devices.

MOSFET process (see Fig. 1) [2], which is leveraged for heterogeneous TFET-MOSFET logic design [15]. From the circuit design perspective, the layouts of ETL-TFET and MOSFET, as shown in Fig. 4, are identical, enabling integration of TFET and MOSFET devices. An NTFET sleep transistor is also embedded for power gating to further reduce the leakage power.

A. SPEED ENHANCEMENT

A fan-out-of-4 (FO4) complementary inverter is chosen to evaluate the circuit delay and transition energy. The FO4 inverter delay and transition energy with respect to supply voltage are shown in Fig. 5. Given $V_{DD} = 0.3$ V, ETL-TFET inverter exhibits 16× shorter delay and 1.9× larger transition energy. The impact of the higher parasitic capacitance in the ETL-TFET causes the higher energy consumption. However, the tremendous speed gain allows the TFET-based circuit to operate at lower V_{DD} to save energy consumption without delay penalty.

To explore the advantages of the dynamic logic, we performed an energy–delay analysis [25], in which INV, NAND, and NOR gates are weighted by the ratio 50%, 25%, and 25%, respectively. Fig. 6(a) shows that the TFET dynamic structure has the lowest energy dissipation compared with MOSFET-based dynamic logic and complementary logic gates realized by MOSFET or TFET. For TFET devices, a 74% energy reduction is achieved through dynamic structure compared with the complementary counterpart. Considering the dynamic logic, distinct heterogeneous structures are evaluated, as shown in Fig. 6(b). Due to the lower capacitance of MOSFET and higher current conduction of TFET, the pMOS-NTFET structure demonstrates the lowest energy consumption when delay <10 ns.

B. LEAKAGE SUPPRESSION

The NTFET device has a high ON-state/turn-off current ratio I_{ON}/I_{OFF} in low V_{DD}, which can be leveraged for power gating. An analysis method presented in [26], in which a nine-stage ring oscillator connected through a power gating transistor, is adopted. The delay and virtual ground voltage (V_{VG}) are shown in Fig. 7. For nMOS, when the supply voltage is reduced below the threshold voltage V_{TH}, V_{VG} cannot be reduced simultaneously due to the dramatic increase of ON-state resistance of the gating transistor. This yields less voltage headroom for circuit operation, degrading the circuit performance. In contrast, V_{VG} decreases for NTFET due to the higher current conduction. At $V_{DD} = 0.3$ V, the ring

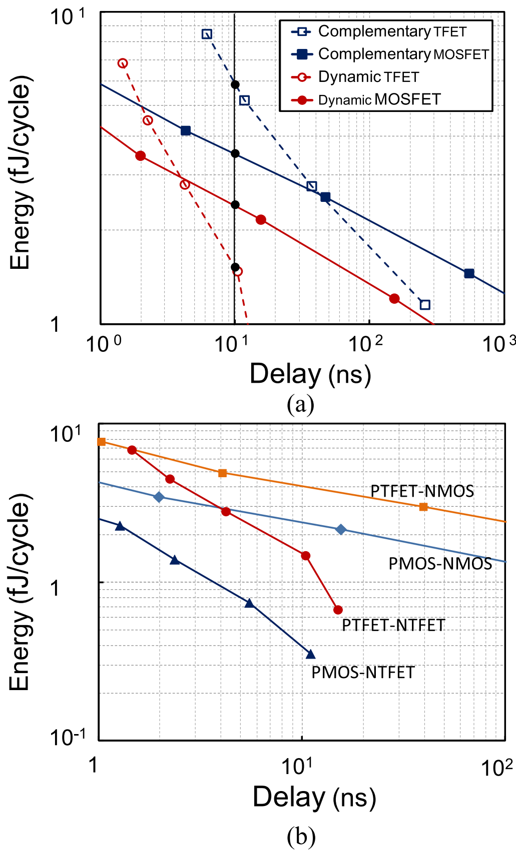

FIGURE 6. Energy–delay analysis with INV/NAND/NOR combined by 50%/25%/25%. (a) Complementary versus dynamic logic with different devices. (b) Dynamic logic with heterogeneous structures.

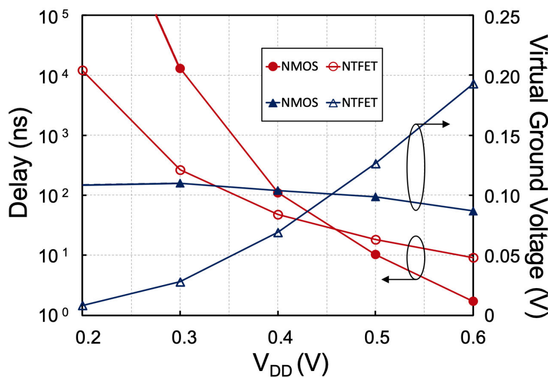

FIGURE 7. Ring oscillator delay and virtual ground voltage versus power supply voltage.

oscillator with NTFET power gating has a 50× shorter delay compared with the nMOS-based counterpart.

V_{VG} can be regarded as an indicator of circuit performance. A lower V_{VG} indicates a shorter delay. As the width of the power-gating transistor increases, the effective current conduction increases, thereby reducing V_{VG}. The increased device width, however, introduces a larger leakage

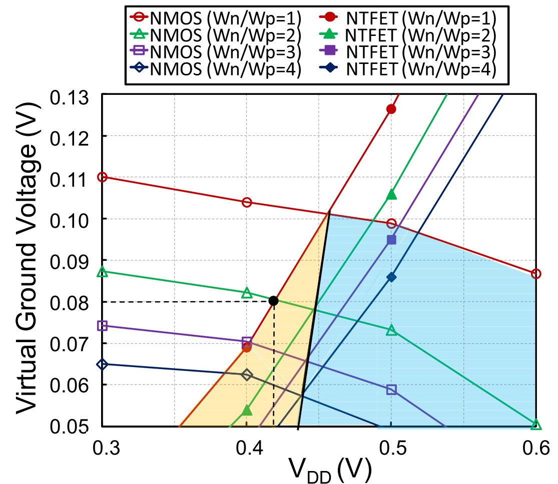

FIGURE 8. Virtual ground voltage for distinct supply voltages and power gating transistor sizes. W_n: width of n-type device. W_p: width of p-type device.

TABLE 2. Truth table for 1-bit full adder by function unit.

A	B	F	Cin	XOR output (X)	AND output	MUX output (Cout)
1	1	0	1/0	1/0	1	1/1
1	0	1	1/0	0/1	0	1/0
0	1	1	1/0	0/1	0	1/0
0	0	0	1/0	1/0	0	0/0

current in the sleep mode. Hence, there is a tradeoff between performance and leakage. Given that MOSFET and TFET have the same leakage current given the same device width, the design options with V_{DD}, V_{VG}, and power gating transistor size are shown in Fig. 8. The orange zone indicates that TFET-based power gating can achieve lower leakage power under the same condition. As an example, NTFET demonstrates a 48.9% less leakage power than nMOS when $V_{DD} = 0.42$ V and $V_{VG} = 0.08$ V (shown by the dashed guiding lines in Fig. 8). At a low V_{DD}, a larger nMOS for power gating is needed to meet the same performance as NTFET, resulting in larger leakage power consumption.

IV. ASYNCHRONOUS DATAPATH

Asynchronous datapath is considered here to maximize the utilization of the TFET device. Conventional synchronous pipeline structure suffers from high delay sensitivity to the voltage variation in the low-voltage region. Asynchronous circuits, however, do not need a global clock and data are only exchanged when the computation is completed. The clock-less feature renders asynchronous circuits resilient against PVT variations in the low-voltage region.

A function unit in an asynchronous FPGA [17] is chosen for performance evaluation. Figs. 9 and 10 show the architecture of the function unit and the circuits of the submodules. The asynchronous pipeline stage consists of a gating transistor and an n-type pull-down network, which can be efficiently

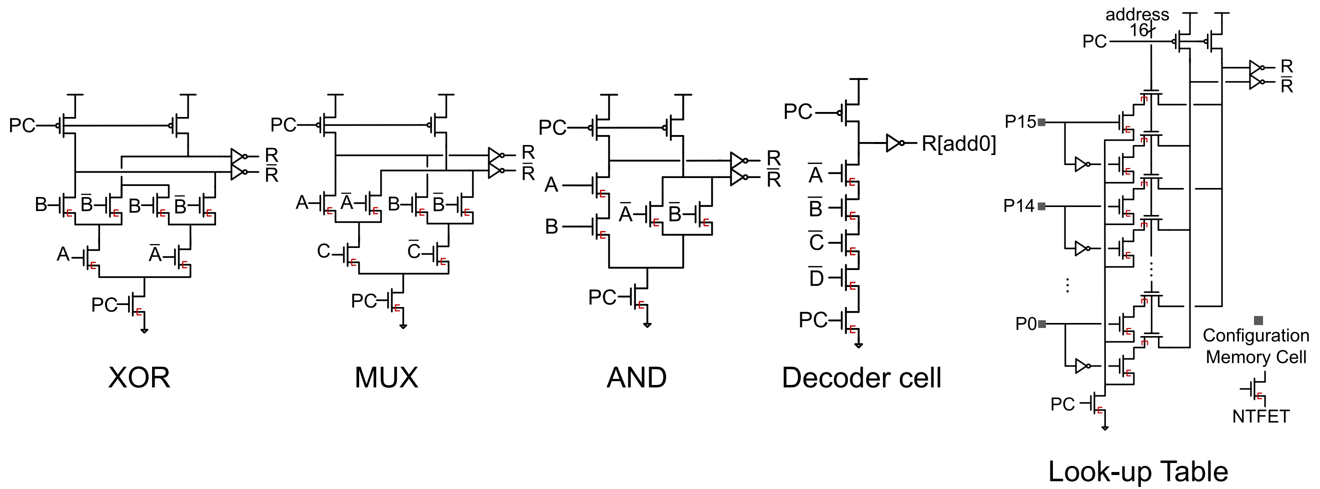

FIGURE 9. Subcircuits of the function unit. pMOS and NTFET are heterogeneously integrated to minimize the power dissipation.

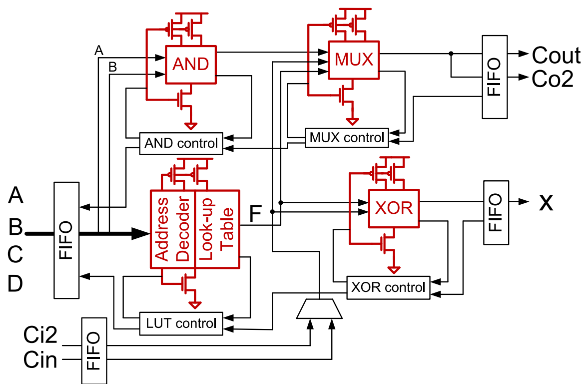

FIGURE 10. Function unit in a pipelined asynchronous FPGA architecture.

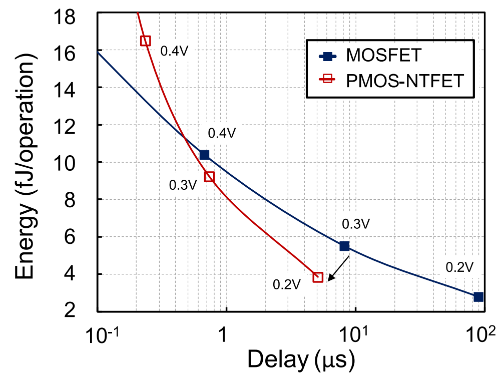

FIGURE 11. Delay–energy performance of the function unit for MOSFET and MOSFET-TFET implementations.

realized by NTFET-based logic and pMOS/NTFET power gating cells controlled by a power control (PC) signal. The function of 1-bit full adder by function unit is demonstrated to show the circuit operation. The truth table of a 1-bit full adder is shown in Table 2, where A and B are the two inputs. Through the address decoder and lookup table (LUT), the sum of a half-adder F with two inputs A and B is calculated. The sum of a full-adder X is the output of an XOR gate with inputs F and carry in (Cin). In addition, the carry-out signal (Cout) can be realized by proper select signals. The carry signals can be cascaded to form a carry-ripple chain for carry propagation [17].

The subcircuits of the function unit are realized with the proposed heterogeneous pMOS-NTFET structure, as shown in Fig. 9. The output nodes R and $\bar{R}$ are set to V_{SS} in the precharge phase before the subcircuits are activated. pMOS devices, which have lower parasitic capacitance, are used as the pull-up transistors to reduce the energy consumption. In the evaluation phase, the computation speed depends on the discharge current of pull-down network. NTFET devices, which have low leakage current and high ON-state current, are adopted for the pull-down network.

The energy–delay curve of the asynchronous function unit is shown in Fig. 11. The unique characteristic of NTFET expands the energy–delay space. The proposed heterogeneous pMOS-NTFET structure is able to achieve lower energy consumption and shorter circuit delay in a low-voltage region. The heterogeneous structure tailored for the asynchronous datapath demonstrates a superior performance for energy-constrained applications. The delay and energy reductions by employing pMOS-NTFET structure for the subcircuits are shown in Fig. 12. By leveraging delay reduction, the pMOS-NTFET circuit can operate at a lower power supply voltage than MOSFET counterpart without a delay penalty. For the decoder cell (Dec), five n-type devices in series increase the delay extremely, but NTFET devices can improve the circuit speed by 1.71×. For LUT, large devices loading connected at output node causes the large delay penalty. The heterogeneous pMOS-NTFET structure achieves a 1.43× speed improvement. Overall, the proposed pMOS-NTFET heterogeneous structure achieves 20.9%–33.9% energy savings compared with the conventional MOSFET realization.

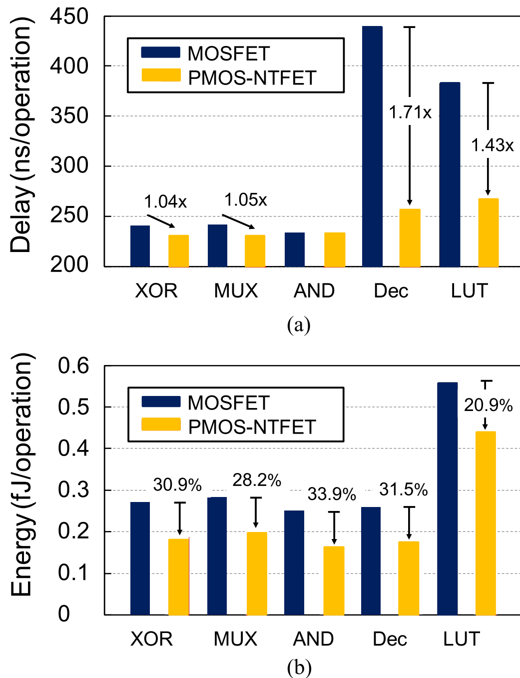

FIGURE 12. Performance evaluation of the subcircuits (Dec: decoder cell and LUT: lookup table) for (a) propagation delay and (b) energy dissipation. Supply voltages for MOSFET and pMOS-NTFET realizations are 0.3 and 0.2 V, respectively.

V. CONCLUSION

The ETL-TFET device with low-bandgap SiGe material in ETL shows a steep SS and a high ON-state current in the ultralow V_{DD} region. However, the increased parasitic capacitance of ETL-TFET also degrades the circuit performance. Compared with the MOSFET-based circuit, speed improvement and energy reduction of the TFET-based circuits are addressed in this work. Given the same delay, TFET-based dynamic logic consumes less energy than both FDSOI-MOSFET-based complementary and dynamic logic gates. Since the ETL-TFET is highly compatible with the MOSFET process, the heterogeneous pMOS-NTFET structure can further improve the performance of ETL-TFET-based dynamic logic in terms of delay and energy. As for power gating, NTFET demonstrates better suppression on the raised virtual ground voltage when V_{DD} scales down to the subthreshold region. Asynchronous datapath is investigated to combat PVT variations in the ultralow-voltage applications. Tailored for the asynchronous function unit, the heterogeneous pMOS-NTFET dynamic logic with power gating structure achieves 20.9%–33.9% energy savings. The concept of ETL-TFET can also be applied to another material system with narrower bandgap, such as GeSn ETL on Ge channel or InAs ETL on InGaAs channel [27]. In these cases, the ON-current would increase due to higher BTBT probability so that the improvement of circuit performance could be expected. This provides a promising solution for future energy-efficient VLSI signal processing in the ultralow-voltage region.

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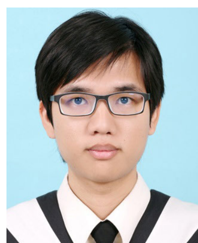

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